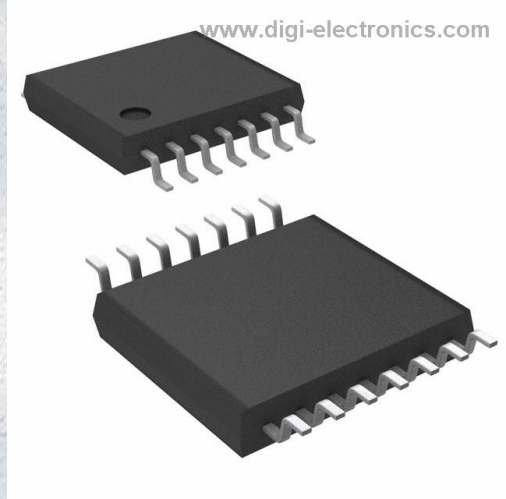
# 74LVX14MTCX Datasheet

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| | |
|---|---|
| DiGi Electronics Part Number | 74LVX14MTCX-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | 74LVX14MTCX |
| Description | IC INVERTER 6CH 1-INP 14TSSOP |
| Detailed Description | Inverter IC 6 Channel Schmitt Trigger 14-TSSOP |

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| 74LVX14MTCX | onsemi |
| Series: | Product Status: |
| 74LVX | Active |
| Logic Type: | Number of Circuits: |
| Inverter | 6 |
| Number of Inputs: | Features: |
| 1 | Schmitt Trigger |
| Voltage - Supply: | Current - Quiescent (Max): |
| 2V ~ 3.6V | 2 µA |
| Current - Output High, Low: | Input Logic Level - Low: |
| 4mA, 4mA | 0.9V |
| Input Logic Level - High: | Max Propagation Delay @ V, Max CL: |
| 2.2V | 14.1ns @ 3.3V, 50pF |
| Operating Temperature: | Mounting Type: |
| -40°C ~ 85°C | Surface Mount |
| Supplier Device Package: | Package / Case: |
| 14-TSSOP | 14-TSSOP (0.173", 4.40mm Width) |
| Base Product Number: | |
| 74LVX14 | |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| ROHS3 Compliant | 1 (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

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**DATA SHEET**
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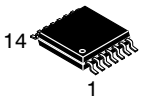
# Low Voltage Hex Inverter with Schmitt Trigger Input

# 74LVX14




**TSSOP−14**
**DT SUFFIX**
**CASE 948G**

## General Description

The LVX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter−free output signals. In addition, they have a greater noise margin than conventional inverters.

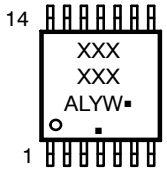
The LVX14 has hysteresis between the positive−going and negative−going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

The inputs tolerate voltages up to 6.5 V allowing the interface of 5 V systems to 3 V systems.

## Features

- Input Voltage Level Translation From 5 V to 3 V
- Ideal For Low Power/Low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- These Devices are Pb−Free and Halide Free

## MARKING DIAGRAM




XXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
Ww, W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

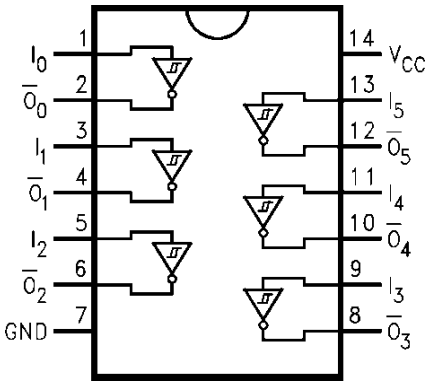



**Figure 1. Connection Diagram**

**PIN DESCRIPTION**

| Pin Names | Description |
|---|---|
| $I_n$ | Inputs |
| $\overline{O}_n$ | Outputs |

**TRUTH TABLE**

| Input | Output |
|---|---|
| **A** | **$\overline{O}$** |
| L | H |
| H | L |

**EEE/IEC**

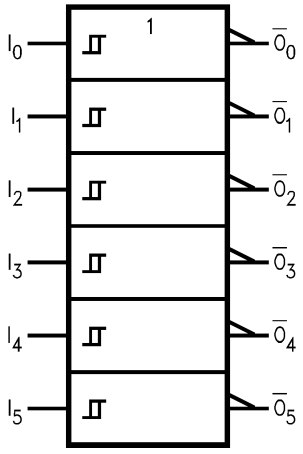



**Figure 2. Logic Symbol**

**ABSOLUTE MAXIMUM RATINGS** (The absolute maximum ratings are stress ratings only.)

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 V to +6.5 V |
| $I_{IK}$ | DC Input Diode Current, $V_I$ = −0.5 V | −20mA |
| $V_I$ | DC Input Voltage | −0.5 V to 6.5 V |
| $I_{OK}$ | DC Output Diode Current<br>$V_O$ = −0.5 V | −20 mA |
| | $V_O$ = $V_{CC}$ + 0.5 V | +20 mA |
| $V_O$ | DC Output Voltage | −0.5 V to $V_{CC}$ + 0.5 V |
| $I_O$ | DC Output Source or Sink Current | ±25 mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ±50 mA |
| $T_{STG}$ | Storage Temperature | −65°C to +150°C |
| $P_D$ | Power Dissipation | 833 mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**RECOMMENDED OPERATING CONDITIONS** (Note 1)

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.0 V to 3.6 V |
| $V_I$ | Input Voltage | 0 V to 5.5 V |
| $V_O$ | Output Voltage | 0 V to $V_{CC}$ |
| $T_A$ | Operating Temperature | −40°C to +85°C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

**DC CHARACTERISTICS**

| Symbol | Parameter | $V_{CC}$ | Conditions | $T_A$ = +25°C | | | $T_A$ = −40°C to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{T+}$ | Positive Threshold | 3.0 | – | – | – | 2.2 | – | 2.2 | V |
| $V_{T−}$ | Negative Threshold | 3.0 | – | 0.9 | – | – | 0.9 | – | V |
| $V_H$ | Hysteresis | 3.0 | – | 0.3 | – | 1.2 | 0.3 | 1.2 | V |
| $V_{OH}$ | HIGH Level Output Voltage | 2.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −50 μA | 1.9 | 2.0 | – | 1.9 | – | V |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −50 μA | 2.9 | 3.0 | – | 2.9 | – | |
| | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −4 mA | 2.58 | – | – | 2.48 | – | |
| $V_{OL}$ | LOW Level Output Voltage | 2.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = 50 μA | – | 0.0 | 0.1 | – | 0.1 | V |
| | | 3.0 | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = 50 μA | – | 0.0 | 0.1 | – | 0.1 | |
| | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = 4 mA | – | – | 0.36 | – | 0.44 | |
| $I_{IN}$ | Input Leakage Current | 3.6 | $V_{IN}$ = 5.5 V or GND | – | – | ±0.1 | – | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | 3.6 | $V_{IN}$ = $V_{CC}$ or GND | – | – | 2.0 | – | 0 | μA |

## NOISE CHARACTERISTICS (Note 2)

| Symbol | Parameter | $V_{CC}$ (V) | $C_L$ (pF) | $T_A$ = 25°C | | Unit |
|---|---|---|---|---|---|---|
| | | | | Typ | Limits | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 50 | 0.3 | 0.5 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | 50 | –0.3 | –0.5 | V |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 3.3 | 50 | – | 2.0 | V |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 3.3 | 50 | – | 0.8 | V |

2. Input $t_r = t_f$ = 3 ns.

## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | $C_L$ (pF) | $T_A$ = +25°C | | | $T_A$ = –40°C to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Time | 2.7 | 15<br>50 | –<br>– | 8.7<br>11.2 | 16.3<br>19.8 | 1.0<br>1.0 | 19.5<br>23.0 | ns |
| | | 3.3 ±0.3 | 15<br>50 | –<br>– | 6.8<br>9.3 | 10.6<br>14.1 | 1.0<br>1.0 | 12.5<br>16.0 | |
| $T_{OSLH}$, $t_{OSHL}$ | Output to Output Skew (Note 3) | 2.7 | 50 | – | – | 1.5 | – | 1.5 | ns |
| | | 3.3 | | – | – | 1.5 | – | 1.5 | |

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

## CAPACITANCE

| Symbol | Parameter | $T_A$ = +25°C | | | $T_A$ = –40°C to 85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $C_{IN}$ | Input Capacitance | – | 4 | 10 | – | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 4) | – | 21 | – | – | – | pF |

4. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

(eq. 1) $$I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{6 \text{ (per Gate)}}$$

## ORDERING INFORMATION

| Part Number | Package | Marking | Shipping† |
|---|---|---|---|
| 74LVX14MTCX | TSSOP–14 | LVX<br>14 | 2500 Units / Tape & Reel |

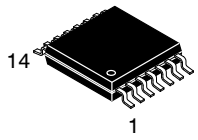
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*–Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

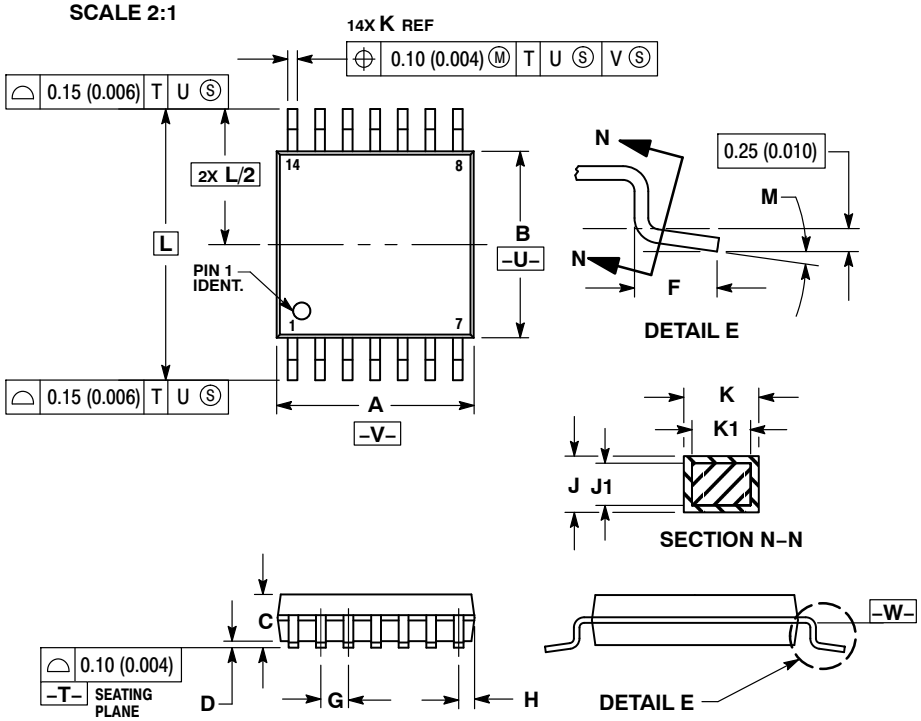
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−14 WB**
CASE 948G
ISSUE C

DATE 17 FEB 2016



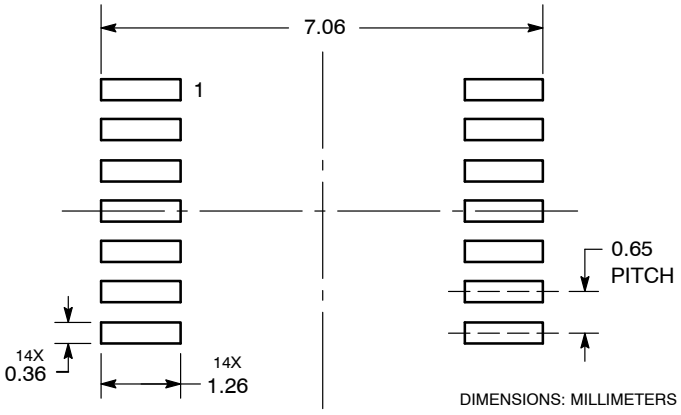

SCALE 2:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

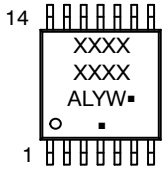
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−14 WB** | **PAGE 1 OF 1** |

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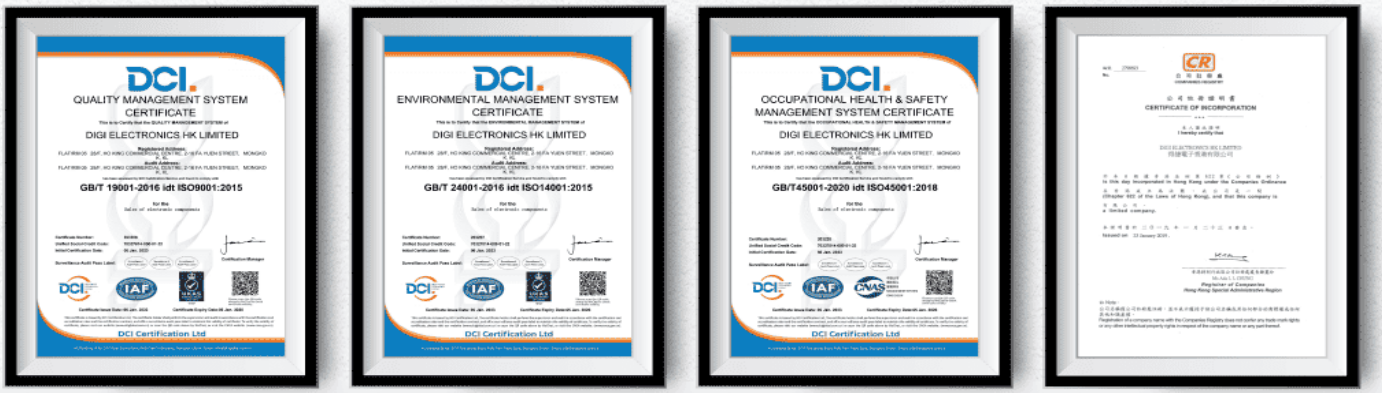



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