74LVX541MX Datasheet

DiGi Electronics Part Number	74LVX541MX-DG
Manufacturer	onsemi
Manufacturer Product Number	74LVX541MX
Description	IC BUF NON-INVERT 3.6V 20SOIC
Detailed Description	Buffer, Non-Inverting 1 Element 8 Bit per Element 3 -State Output 20-SOIC

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74LVX541MX	onsemi
Series:	Product Status:
74LVX	Obsolete
Logic Type:	Number of Elements:
Buffer, Non-Inverting	1
Number of Bits per Element:	Input Type:
8	-
Output Type:	Current - Output High, Low:
3-State	4mA, 4mA
Voltage - Supply:	Operating Temperature:
2V ~ 3.6V	-40°C ~ 85°C (TA)
Mounting Type:	Package / Case:
Surface Mount	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package:	Base Product Number:
20-SOIC	74LVX541

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001

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FAIRCHILD SEMICONDUCTOR®

September 1999
Revised April 2005

74LVX541
Low Voltage Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The LVX541 is an octal non-inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

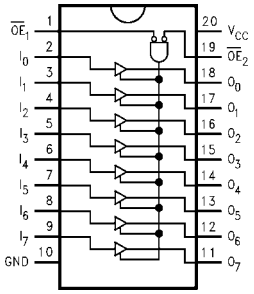
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

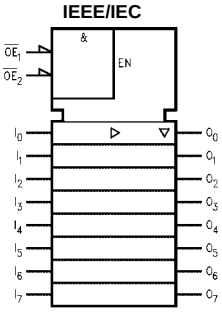
Order Number	Package Number	Package Description
74LVX541M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX541SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0 - I_7	Inputs
O_0 - O_7	3-STATE Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +3.6V
Input Voltage (V_I)	0V to +5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δt/ΔV)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input	2.0	1.5			1.5				
	Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
V_{IL}	LOW Level Input	2.0			0.5		0.5			
	Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V_{OH}	HIGH Level Output	2.0	1.9	2.0		1.9				I_{OH} = −50 μA
	Voltage	3.0	2.9	3.0		2.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	LOW Level Output	2.0		0.0	0.1		0.1			I_{OL} = 50 μA
	Voltage	3.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{OZ}	3-STATE Output OFF-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	C_L = 50 pF
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	C_L = 50 pF
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	C_L = 50 pF
V_{ILD}	Maximum HIGH Level Dynamic Input Voltage	3.3		0.8	V	C_L = 50 pF

Note 3: Input t_r = t_f = 3 ns.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	2.7		6.1	11.3	1.0	13.5	ns	$C_L = 15$ pF
t_{PHL}	Time			8.6	14.9	1.0	17.0		$C_L = 50$ pF
		3.3 ± 0.3		4.7	7.0	1.0	8.5		$C_L = 15$ pF
				7.2	10.5	1.0	12.0		$C_L = 50$ pF
t_{PZL}	3-STATE Output	2.7		7.1	13.8	1.0	16.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
t_{PZH}	Enable Time			9.6	17.3	1.0	20.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ± 0.3		6.8	10.5	1.0	12.5		$C_L = 15$ pF, $R_L = 1$ kΩ
				9.3	14.0	1.0	16.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ}	3-STATE Output	2.7		11.6	17.9	1.0	20.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PHZ}	Disable Time	3.3 ± 0.3		10.7	15.4	1.0	17.5		
t_{OSLH}	Output to Output	2.7			1.5		1.5	ns	$C_L = 50$ pF
t_{OSHL}	Skew (Note 4)	3.3			1.5		1.5		

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$; $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

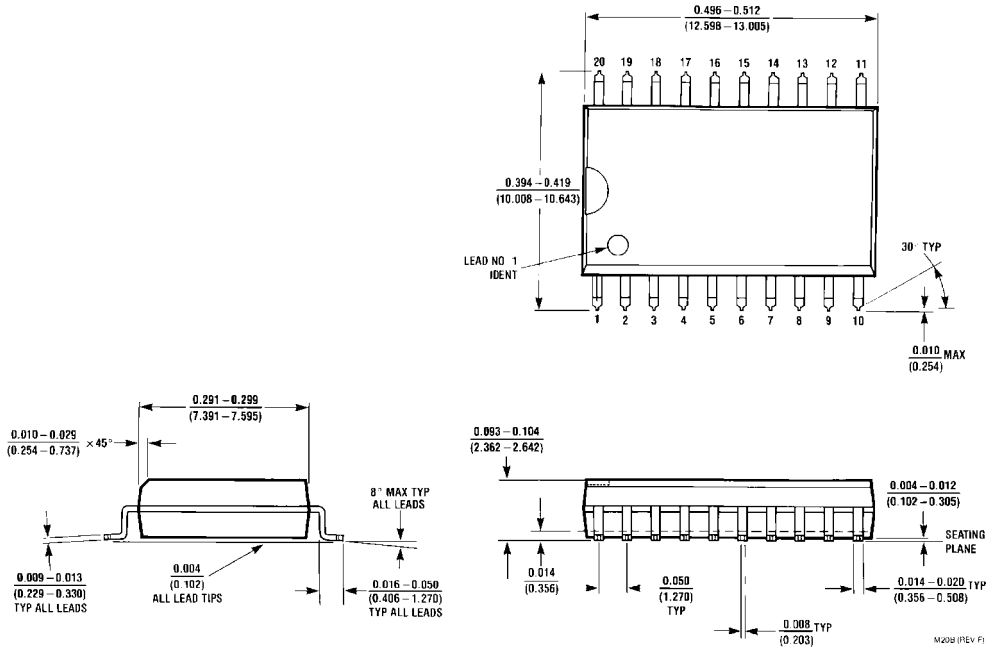
Capacitance

Symbol	Parameter	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 5)		19				pF

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

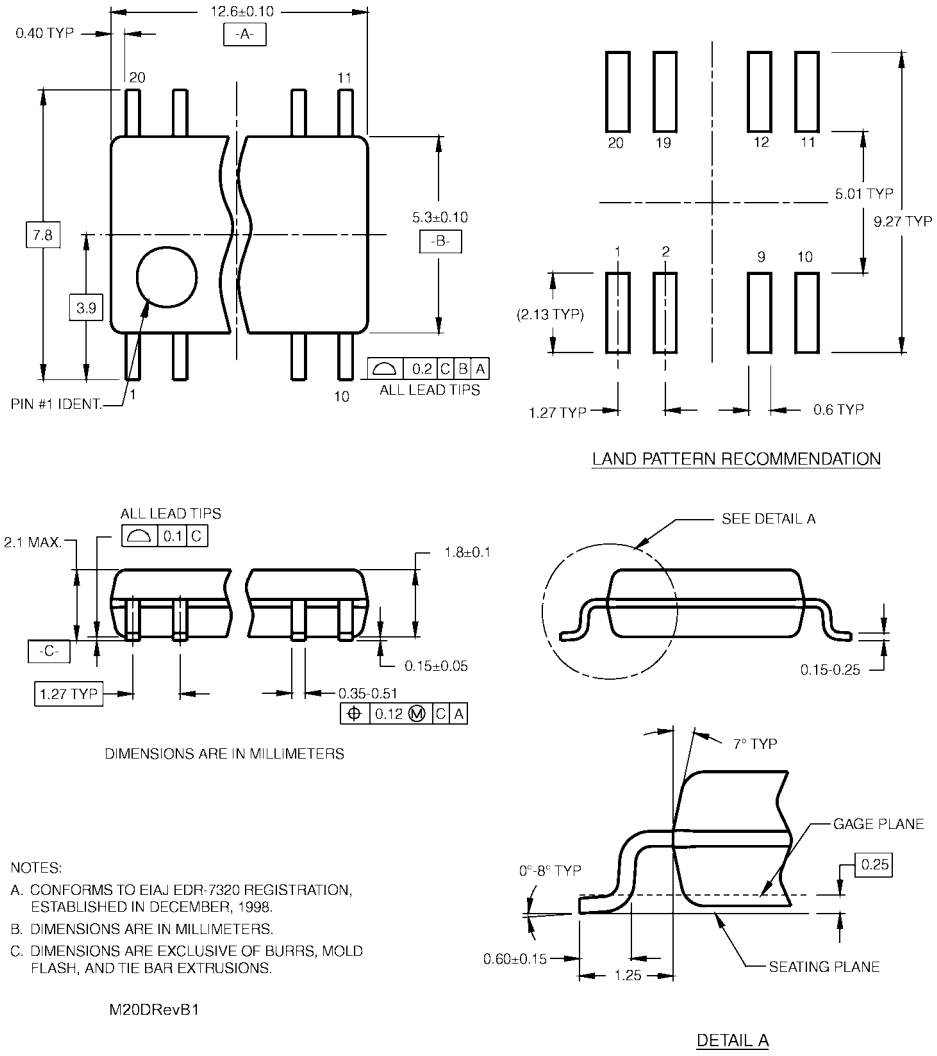
Average operating current can be obtained by the equation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per bit)}}$

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

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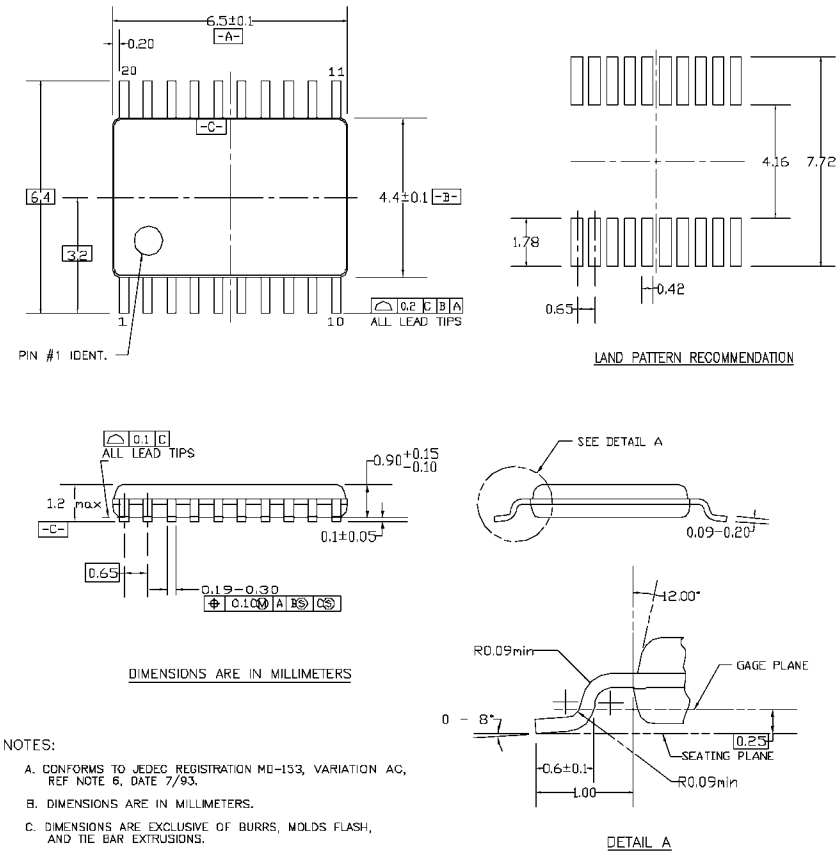
M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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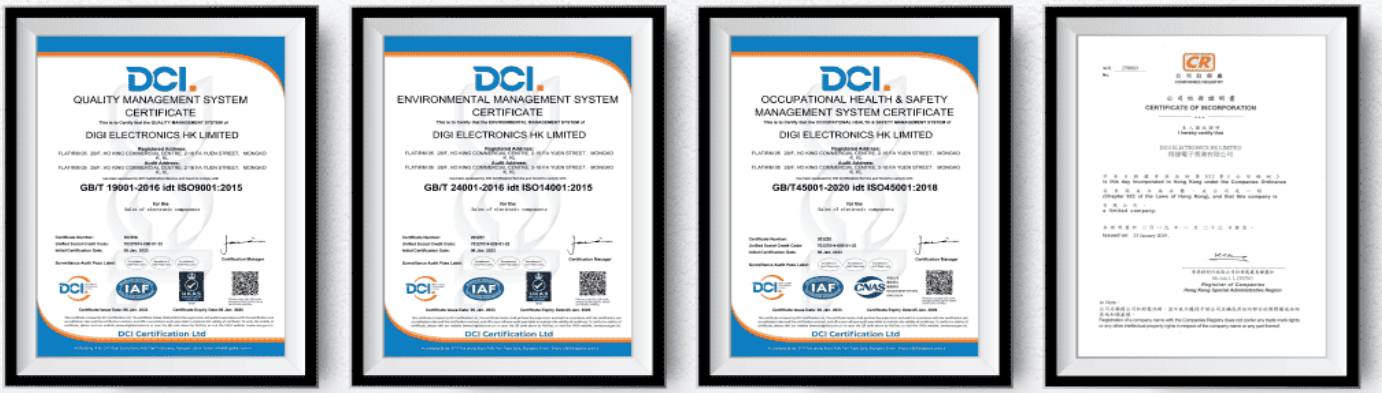

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