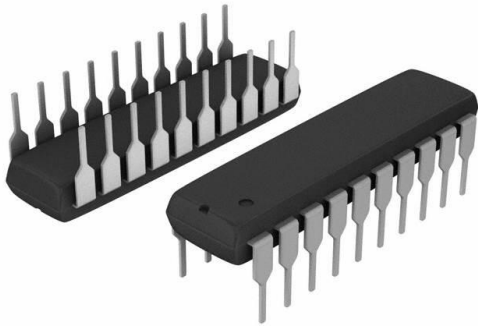


74VHC373N Datasheet

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DiGi Electronics Part Number	74VHC373N-DG
Manufacturer	onsemi
Manufacturer Product Number	74VHC373N
Description	IC D-TYPE TRANSP SGL 8:8 20DIP
Detailed Description	D-Type Transparent Latch 1 Channel 8:8 IC Tri-State 20-PDIP



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

74VHC373N

Series:

74VHC

Logic Type:

D-Type Transparent Latch

Output Type:

Tri-State

Independent Circuits:

1

Current - Output High, Low:

8mA, 8mA

Mounting Type:

Through Hole

Supplier Device Package:

20-PDIP

Manufacturer:

onsemi

Product Status:

Obsolete

Circuit:

8:8

Voltage - Supply:

2V ~ 5.5V

Delay Time - Propagation:

5ns

Operating Temperature:

-40°C ~ 85°C

Package / Case:

20-DIP (0.300", 7.62mm)

Base Product Number:

74VHC373

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

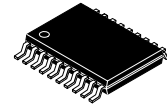
REACH Unaffected

HTSUS:

8542.39.0001

Octal D-Type Latch with 3-STATE Outputs

74VHC373


**TSSOP20, 4.4x6.5
CASE 948AQ**

General Description

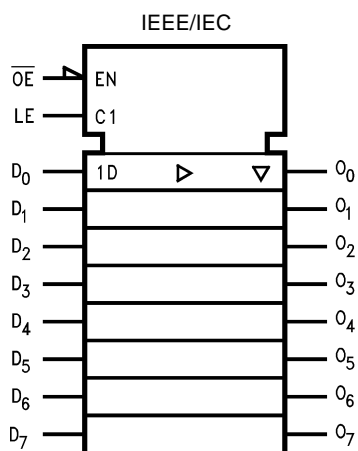
The VHC373 is an advanced high speed CMOS octal D-type latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}). The latches appear transparent to data when latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is LATCHED. When the \overline{OE} input is HIGH, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

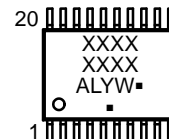
Features

- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5$ V
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min)
- Power Down Protection is Provided on All Inputs
- Low Noise: $V_{OLP} = 0.6$ V (Typ)
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) @ $T_A = 25$ °C
- Pin and Function Compatible with 74HC373
- This is a Pb-Free Device

Logic Symbol


Figure 1. Logic Symbol

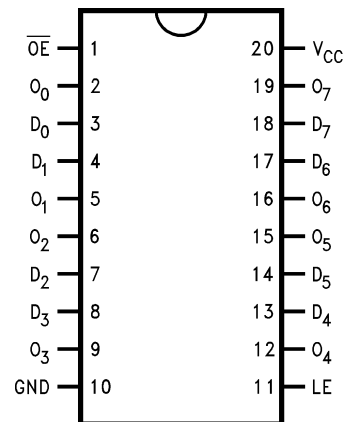
MARKING DIAGRAM



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O ₀ -O ₇	3-STATE Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

74VHC373**TRUTH TABLE**

Inputs			Outputs
LE	\overline{OE}	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level

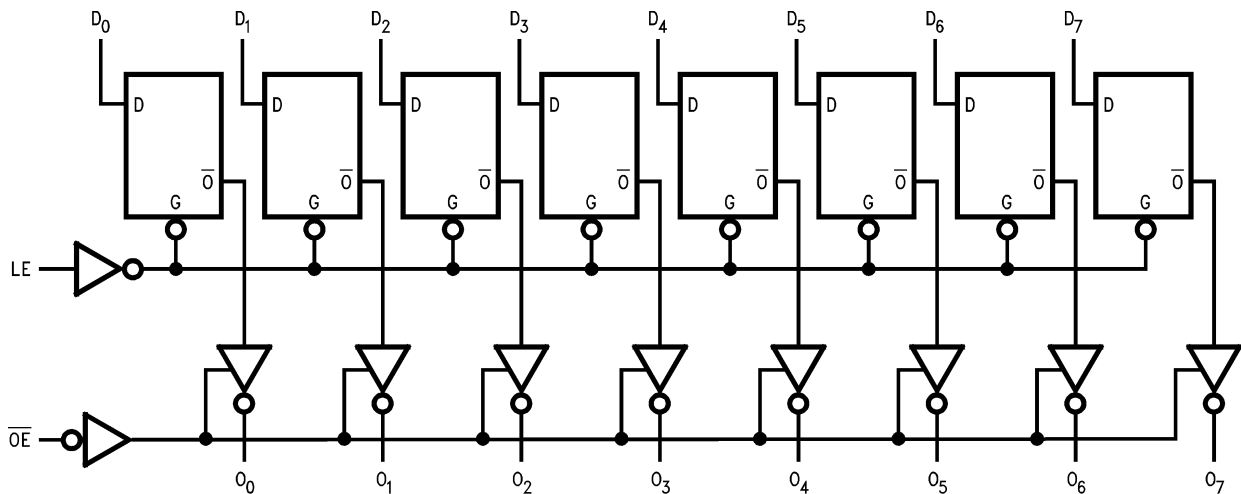
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

 O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable**Functional Description**

The VHC373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

74VHC373**MAXIMUM RATINGS**

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
V _{IN}	DC Input Voltage		-0.5 to +6.5	V
V _{OUT}	DC Output Voltage		-0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current		±20	mA
I _{OUT}	DC Output Current		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±75	mA
I _{IK}	Input Clamp Current		-20	mA
I _{OK}	Output Clamp Current		±20	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T _J	Junction Temperature under Bias		+150	°C
θ _{JA}	Thermal Resistance (Note 2)		150	°C/W
P _D	Power Dissipation in Still Air at 25 °C		833	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.373 in	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage		2.0	5.5	V
V _{IN}	DC Input Voltage (Note 4)		0	5.5	V
V _{OUT}	DC Output Voltage (Note 4)		0	V _{CC}	V
T _A	Operating Temperature		-40	+85	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	0	20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

74VHC373

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit	
				Min	Typ	Max	Min	Max		
V _{IH}	HIGH Level Input Voltage		2.0	1.50	-	-	1.50	-	V	
			3.0-5.5	0.7 x V _{CC}	-	-	0.7 x V _{CC}	-		
V _{IL}	LOW Level Input Voltage		2.0	-	-	0.50	-	0.50	V	
			3.0-5.5	-	-	0.3 x V _{CC}	-	0.3 x V _{CC}		
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	-	1.9	-	V
				3.0	2.9	3.0	-	2.9	-	
				4.5	4.4	4.5	-	4.4	-	
			I _{OH} = -4 mA	3.0	2.58	-	-	2.48	-	
				4.5	3.94	-	-	3.80	-	
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	-	0.0	0.1	-	0.1	V
				3.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
			I _{OL} = 4 mA	3.0	-	-	0.36	-	0.44	
				4.5	-	-	0.36	-	0.44	
I _{OZ}	3-STATE Output Off-State Current	V _{IN} = V _{IH} or V _{IL} ; V _{OUT} = V _{CC} or GND	5.5	-	-	±0.25	-	±2.5	μA	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0-5.5	-	-	±0.1	-	±1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	4.0	-	40.0	μA	

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C		Unit
				Typ	Limits	
V _{OLP} (Note 5)	Quiet Output Maximum Dynamic V _{OL}	C _L = 50 pF	5.0	0.6	0.9	V
V _{OLV} (Note 5)	Quiet Output Minimum Dynamic V _{OL}	C _L = 50 pF	5.0	-0.6	-0.9	V
V _{IHD} (Note 5)	Minimum HIGH Level Dynamic Input Voltage	C _L = 50 pF	5.0	-	3.5	V
V _{ILD} (Note 5)	Maximum LOW Level Dynamic Input Voltage	C _L = 50 pF	5.0	-	1.5	V

5. Parameter guaranteed by design.

74VHC373

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit	
				Min	Typ	Max	Min	Max		
t _{PLH} , t _{PHL}	Propagation Delay Time (LE to O _n)		C _L = 15 pF	3.3 ±0.3	-	7.0	11.0	1.0	13.0	ns
			C _L = 50 pF		-	9.5	14.5	1.0	16.5	
			C _L = 15 pF	5.0 ±0.5	-	4.9	7.2	1.0	8.5	ns
			C _L = 50 pF		-	6.4	9.2	1.0	10.5	
t _{PLH} , t _{PHL}	Propagation Delay Time (D to O _n)		C _L = 15 pF	3.3 ±0.3	-	7.3	11.4	1.0	13.5	ns
			C _L = 50 pF		-	9.8	14.9	1.0	17.0	
			C _L = 15 pF	5.0 ±0.5	-	5.0	7.2	1.0	8.5	ns
			C _L = 50 pF		-	6.5	9.2	1.0	10.5	
t _{PZL} , t _{PZH}	3-STATE Output Enable Time	R _L = 1 kΩ	C _L = 15 pF	3.3 ±0.3	-	7.3	11.4	1.0	13.5	ns
			C _L = 50 pF		-	9.8	14.9	1.0	17.0	
			C _L = 15 pF	5.0 ±0.5	-	5.5	8.1	1.0	9.5	ns
			C _L = 50 pF		-	7.0	10.1	1.0	11.5	
t _{PLZ} , t _{PHZ}	3-STATE Output Disable Time	R _L = 1 kΩ	C _L = 50 pF	3.3 ±0.3	-	9.5	13.2	1.0	15.0	ns
			C _L = 50 pF	5.0 ±0.5	-	6.5	9.2	1.0	10.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew	(Note 6)	C _L = 50 pF	3.3 ±0.3	-	-	1.5	-	1.5	ns
			C _L = 50 pF	5.0 ±0.5	-	-	1.0	-	1.0	
C _{IN}	Input Capacitance	V _{CC} = Open		-	4	10	-	10	pF	
C _{OUT}	Output Capacitance	V _{CC} = 5.0 V		-	6	-	-	-	pF	
C _{PD}	Power Dissipation Capacitance	(Note 7)		-	27	-	-	-	pF	

6. Parameter guaranteed by design. t_{OSLH} = |t_{PLH} max - t_{PLH} min|; t_{OSHL} = |t_{PHL} max - t_{PHL} min|

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} · V_{CC} · f_{IN} + I_{CC}/8 (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD} (total) = 14 + 13n.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} (V)	T _A = 25 °C			T _A = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t _{V(H)}	Minimum Pulse Width (LE)	3.3 ±0.3	5.0	-	-	5.0	-	ns
		5.0 ±0.5	5.0	-	-	5.0	-	
t _S	Minimum Set-Up Time	3.3 ±0.3	4.0	-	-	4.0	-	ns
		5.0 ±0.5	4.0	-	-	4.0	-	
t _H	Minimum Hold Time	3.3 ±0.3	1.0	-	-	1.0	-	ns
		5.0 ±0.5	1.0	-	-	1.0	-	

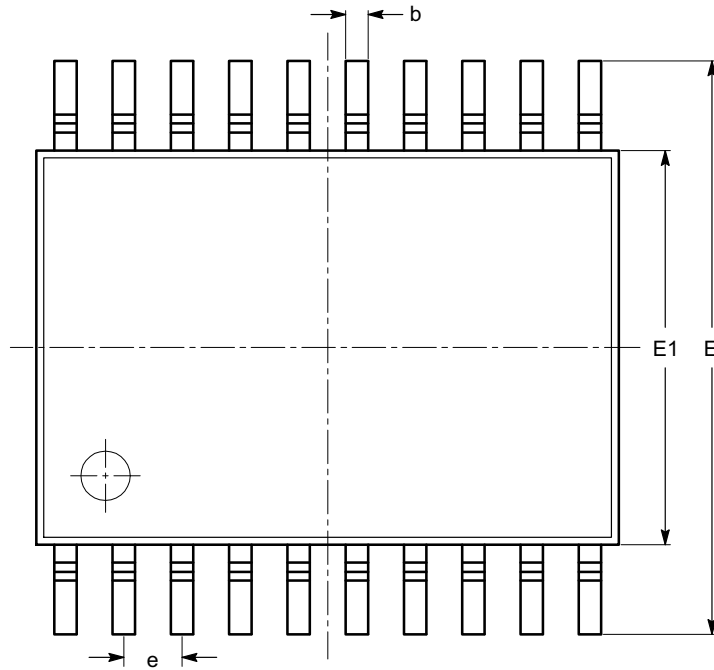
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74VHC373MTCX	VHC 373	TSSOP20 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

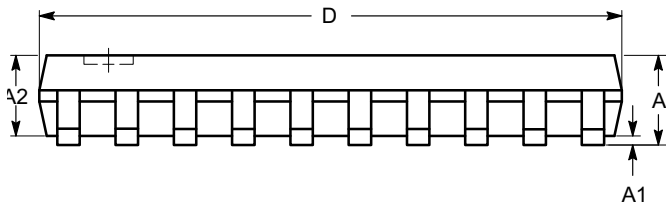
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

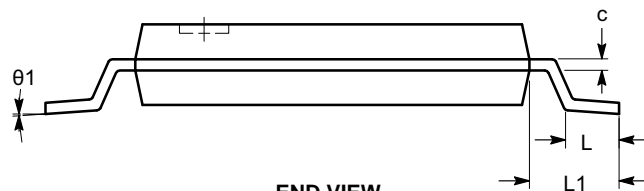


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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DESCRIPTION:	TSSOP20, 4.4X6.5	PAGE 1 OF 1

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