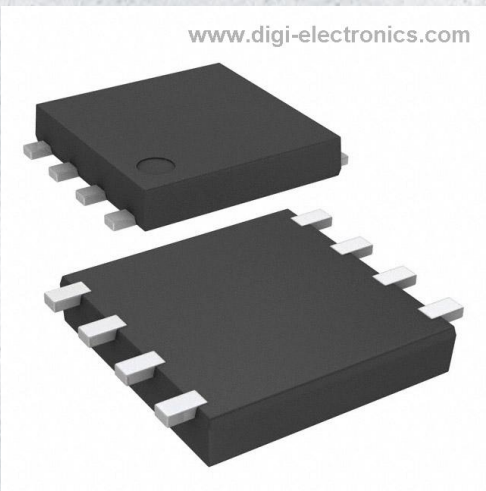
ECH8652-TL-H Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	ECH8652-TL-H-DG
Manufacturer	onsemi
Manufacturer Product Number	ECH8652-TL-H
Description	MOSFET 2P-CH 12V 6A 8ECH
Detailed Description	Mosfet Array 12V 6A 1.5W Surface Mount 8-ECH

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
ECH8652-TL-H	onsemi
Series:	Product Status:
-	Obsolete
Technology:	Configuration:
MOSFET (Metal Oxide)	2 P-Channel (Dual)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	12V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
6A	28mOhm @ 3A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
-	11nC @ 4.5V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
1000pF @ 6V	1.5W
Operating Temperature:	Mounting Type:
150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
8-SMD, Flat Lead	8-ECH
Base Product Number:	
ECH8652	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

Ordering number : ENA0935A

ECH8652

P-Channel Power MOSFET
−12V, −6A, 28mΩ, Dual ECH8

ON Semiconductor®
http://onsemi.com

Features

- Low ON-resistance
- 1.8V drive
- Composit type, facilitating high-density mounting
- Halogen free compliance
- Protection diode in

Specifications

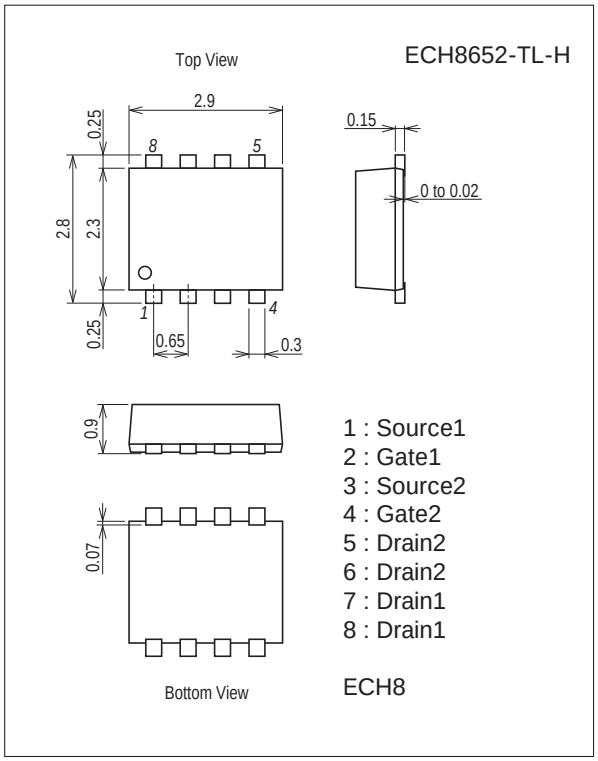
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−12	V
Gate-to-Source Voltage	V_{GSS}		±10	V
Drain Current (DC)	I_D		−6	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−40	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (900mm²×0.8mm) 1unit	1.3	W
Total Power Dissipation	P_T	When mounted on ceramic substrate (900mm²×0.8mm)	1.5	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

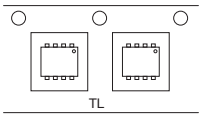
unit : mm (typ)
7011A-001



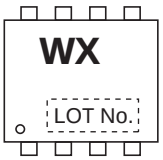
Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

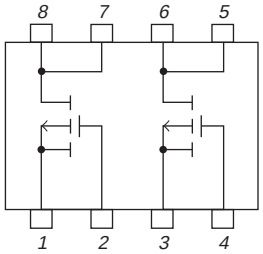
Packing Type : TL



Marking



Electrical Connection

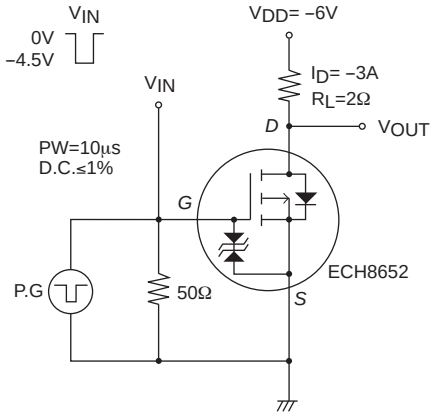


ECH8652

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−12			V
Zero-Gate Voltage Drain Current	$I_{DSS}1$	V_{DS}=−8V, V_{GS}=0V			−1	μA
	$I_{DSS}2$	V_{DS}=−12V, V_{GS}=0V			−10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−6V, I_D=−1mA	−0.4		−1.4	V
Forward Transfer Admittance	| yfs |	V_{DS}=−6V, I_D=−3A	6.6	11		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−3A, V_{GS}=−4.5V		21	28	mΩ
	R_{DS}(on)2	I_D=−1.5A, V_{GS}=−2.5V		31	45	mΩ
	R_{DS}(on)3	I_D=−0.5A, V_{GS}=−1.8V		49	78	mΩ
Input Capacitance	Ciss	V_{DS}=−6V, f=1MHz		1000		pF
Output Capacitance	Coss			320		pF
Reverse Transfer Capacitance	Crss			250		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		11		ns
Rise Time	t_r			72		ns
Turn-OFF Delay Time	t_d(off)			105		ns
Fall Time	t_f			87		ns
Total Gate Charge	Qg	V_{DS}=−6V, V_{GS}=−4.5V, I_D=−6A		11		nC
Gate-to-Source Charge	Qgs			1.5		nC
Gate-to-Drain “Miller” Charge	Qgd			2.9		nC
Diode Forward Voltage	V_{SD}	I_S=−6A, V_{GS}=0V		−0.81	−1.2	V

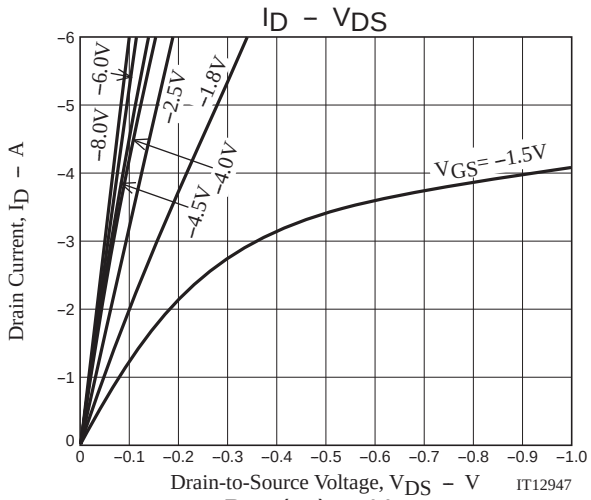
Switching Time Test Circuit

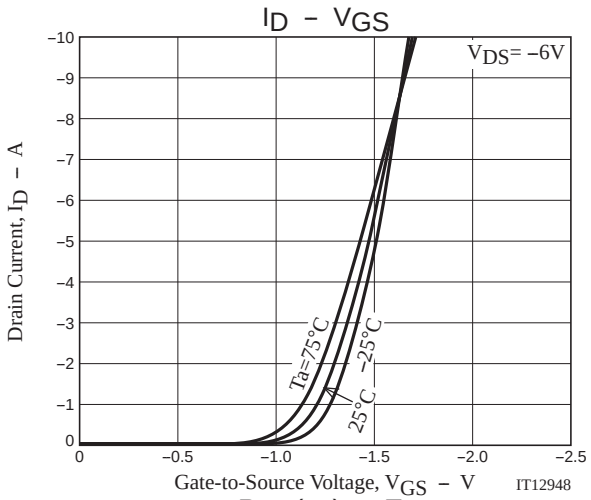


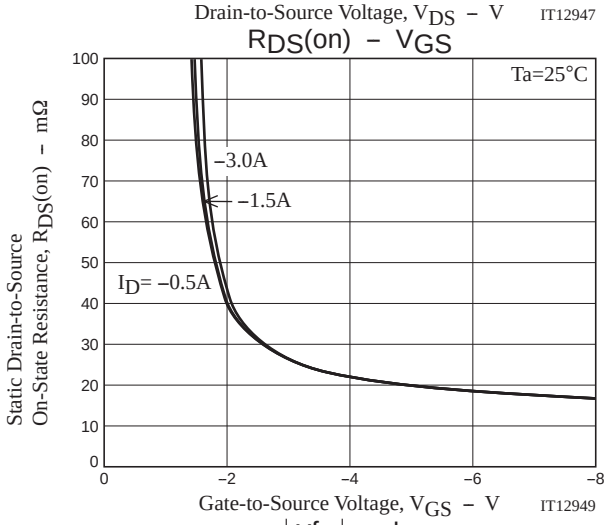
Ordering Information

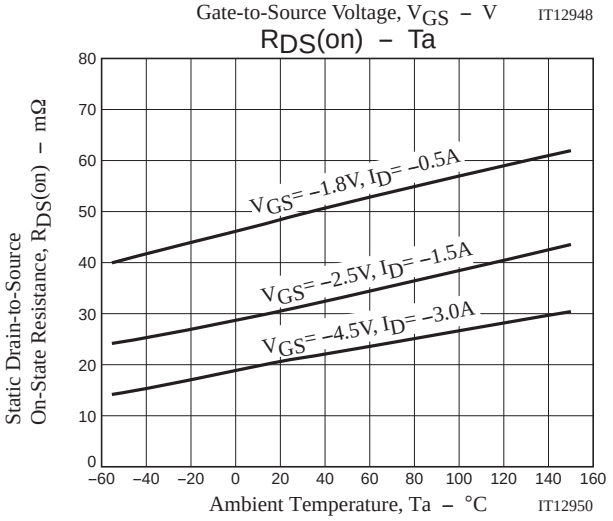
Device	Package	Shipping	memo
ECH8652-TL-H	ECH8	3,000pcs./reel	Pb Free and Halogen Free

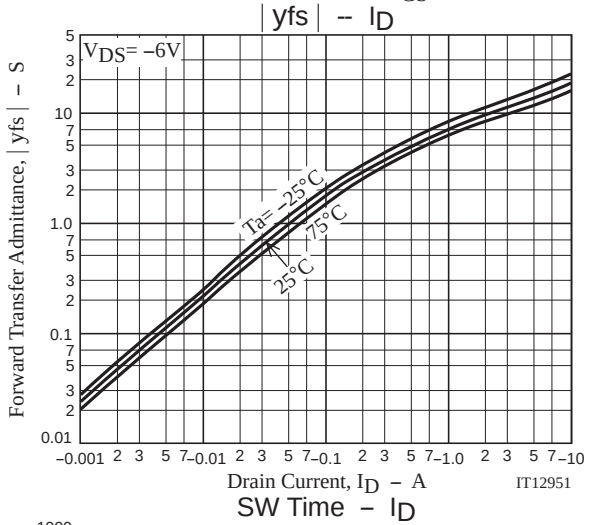
ECH8652

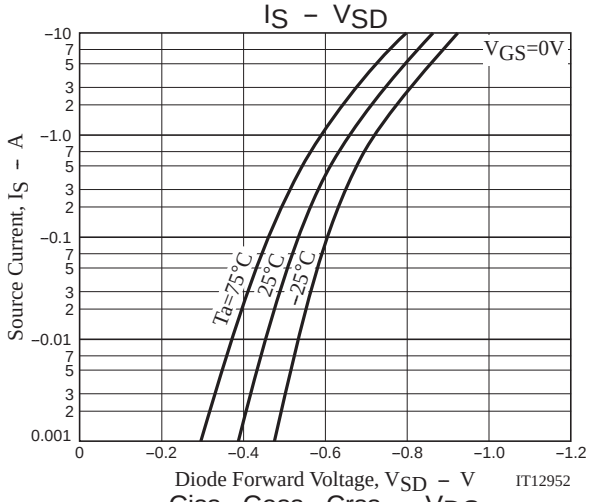

ID – VDS
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT12947
–8.0V
–6.0V
–4.5V
–2.5V
–4.0V
–1.8V
VGS= –1.5V

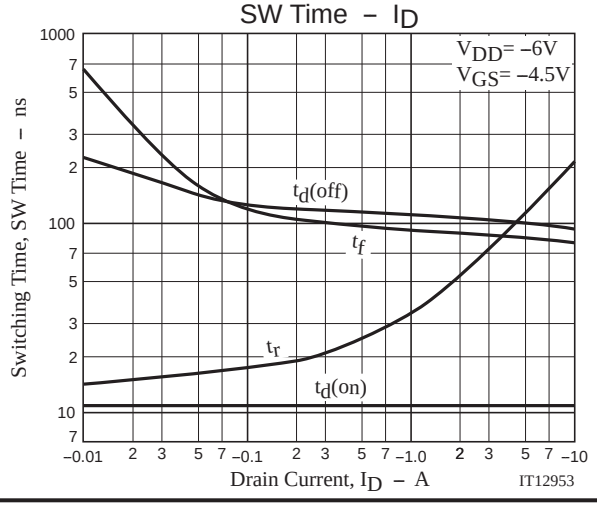

ID – VGS
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT12948
VDS= –6V
Ta=75°C
–25°C
25°C

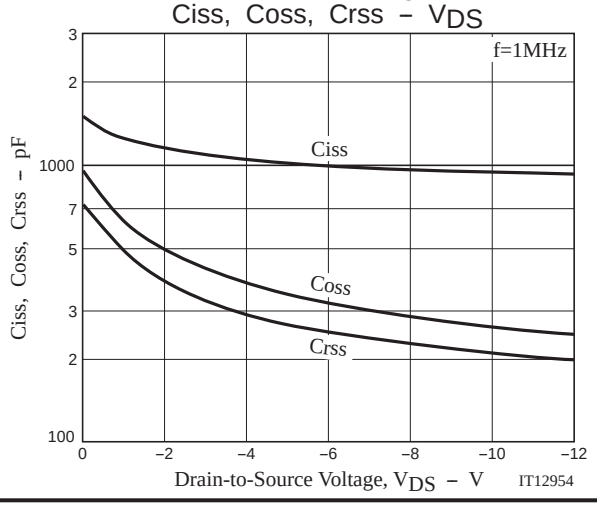

RDS(on) – VGS
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT12949
Ta=25°C
–3.0A
–1.5A
ID= –0.5A

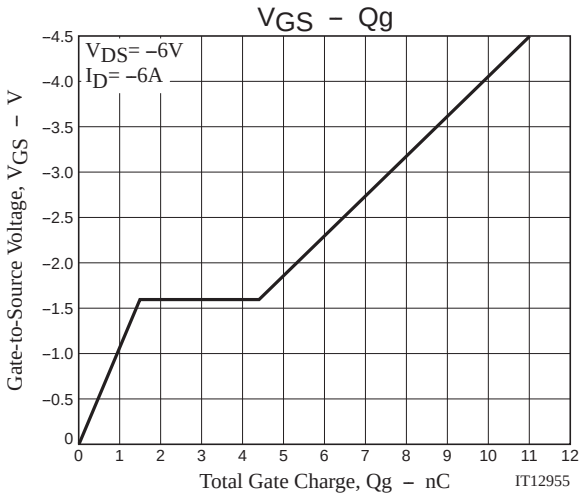

RDS(on) – Ta
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT12950
VGS= –1.8V, ID= –0.5A
VGS= –2.5V, ID= –1.5A
VGS= –4.5V, ID= –3.0A

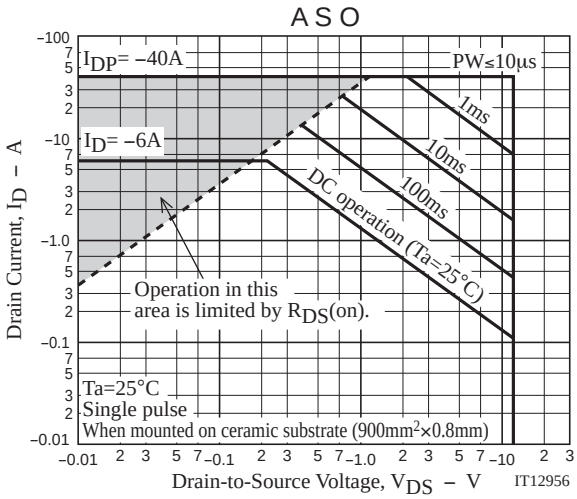

| yfs | – ID
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT12951
VDS= –6V
Ta= –25°C
75°C
25°C

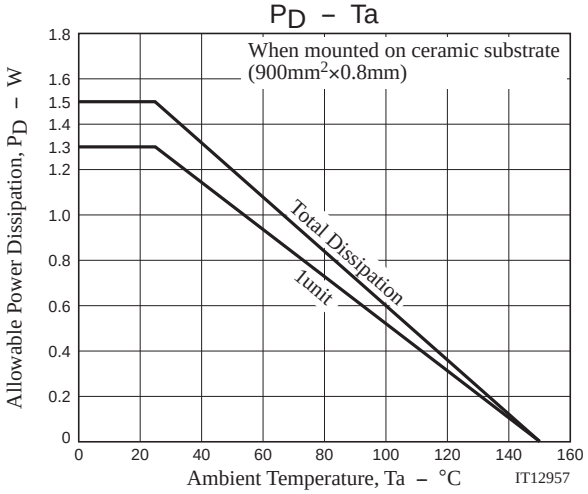

IS – VSD
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT12952
VGS=0V
Ta=75°C
25°C
–25°C


SW Time – ID
Switching Time, SW Time – ns
Drain Current, ID – A
IT12953
VDD= –6V
VGS= –4.5V
td(off)
tf
tr
td(on)


Ciss, Coss, Crss – VDS
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT12954
f=1MHz
Ciss
Coss
Crss


VGS – Qg
VDS= –6V
ID= –6A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT12955


A S O
IDP= –40A
PW≤10μs
ID= –6A
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (900mm2×0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT12956


PD – Ta
When mounted on ceramic substrate
(900mm2×0.8mm)
Total Dissipation
1unit
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT12957

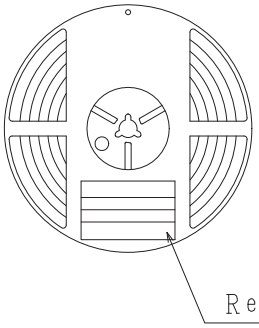
Embossed Taping Specification

ECH8652-TL-H

1. Packing Format

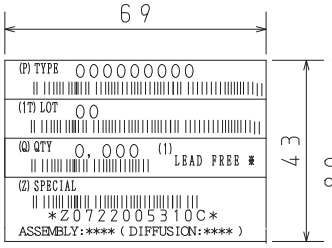
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
ECH8	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm(external) 183×72×185	6 inner boxes contained Dimensions:mm(external) 440×195×210

Packing method



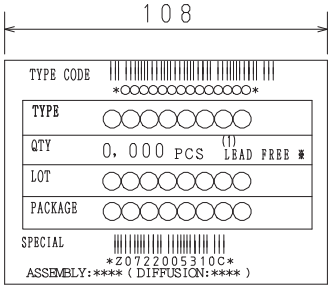
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



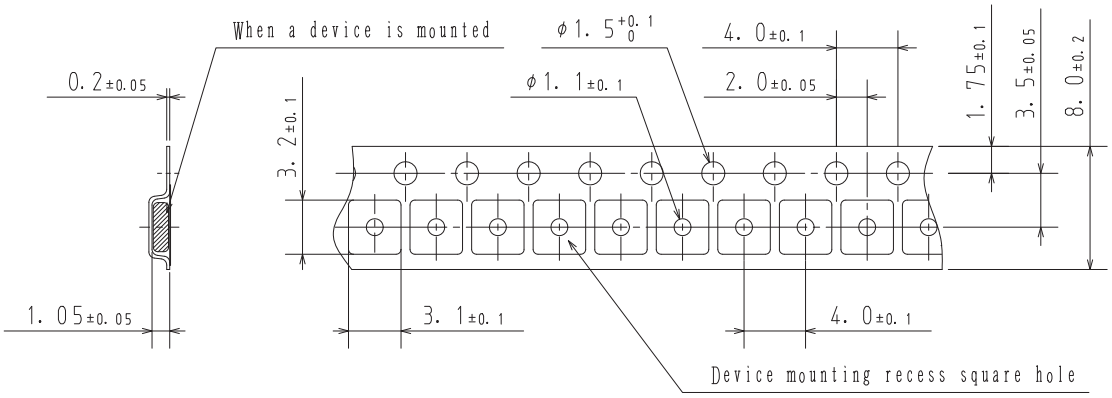
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

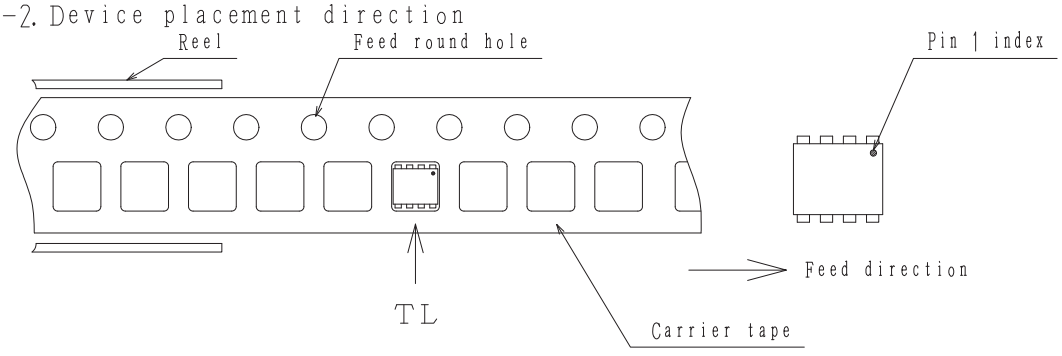
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction

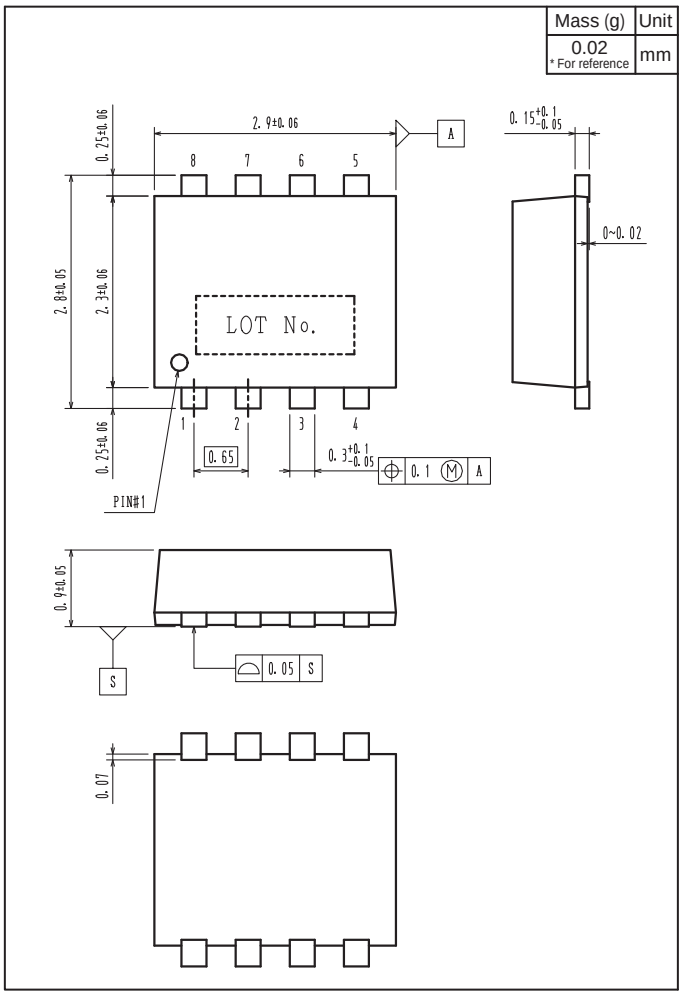


Those with pin 1 index on the feed hole side……TL

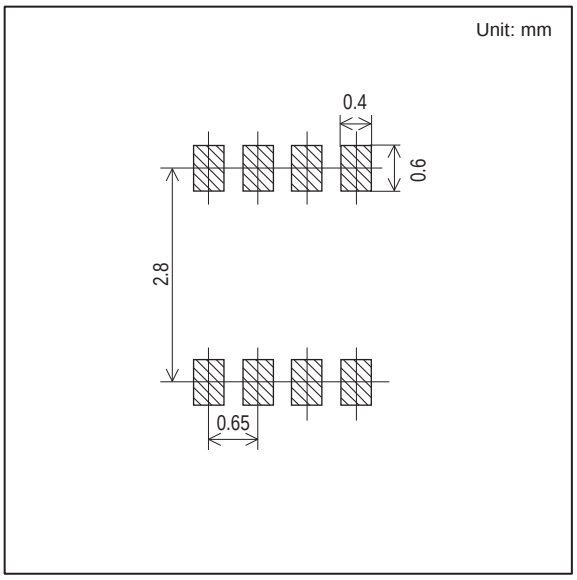
ECH8652

Outline Drawing

ECH8652-TL-H



Land Pattern Example



Note on usage : Since the ECH8652 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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