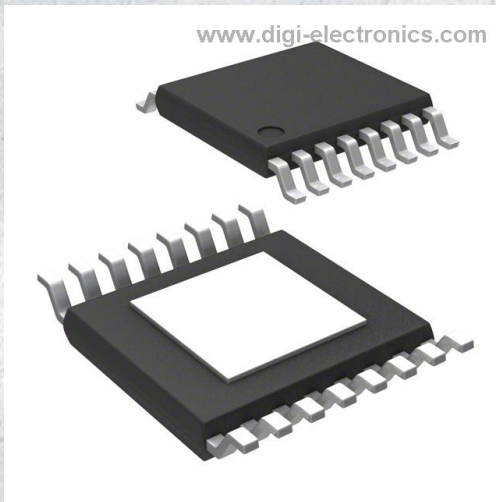


FAN1655MTFX Datasheet



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---|
| DiGi Electronics Part Number | FAN1655MTFX-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | FAN1655MTFX |
| Description | IC REG CTRLR DDR 1OUT 16TSSOP |
| Detailed Description | - Controller, DDR Voltage Regulator IC 1 Output 16-TSSOP-EP |

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Purchase and inquiry

Manufacturer Product Number:

FAN1655MTFX

Series:

-

Applications:

Controller, DDR

Number of Outputs:

1

Operating Temperature:

0°C ~ 125°C

Package / Case:

16-TSSOP (0.173", 4.40mm Width) Exposed Pad

Base Product Number:

FAN1655

Manufacturer:

onsemi

Product Status:

Obsolete

Voltage - Input:

2.3V ~ 3.6V

Voltage - Output:

1.1V ~ 1.8V

Mounting Type:

Surface Mount

Supplier Device Package:

16-TSSOP-EP

Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



January 2006

FAN1655 3A DDR Bus Termination Regulator

Description

The FAN1655 is a low-cost bi-directional LDO specifically designed for terminating DDR memory bus. It can both sink and source up to 2.1A continuous, 3A peak, providing enough current for most DDR applications. Load regulation meets the JEDEC spec, $V_{TT} = V_{REFOUT} \pm 40mV$.

The FAN1655 includes a buffered reference voltage capable of supplying up to 5mA current. On-chip thermal limiting provides protection against a combination of power overload and ambient temperature that would create an excessive junction temperature. A shutdown input puts the FAN1655 into a low power mode.

The FAN1655 regulator is available in a power-enhanced eTSSOP™-16, standard SOIC-14, and an 8-Lead MLP package.

Features

- Sinks and sources 2.1A continuous, 3A peak
- 0 to +125°C operating temperature range
- 5mA Buffered $V_{REFOUT} = V_{DDQ}/2$
- Load regulation: $V_{TT} = V_{REFOUT} \pm 40mV$
- On-chip thermal limiting
- Low Cost SO-14, Power-Enhanced eTSSOP or 8-pin 5x6mm MLP packages
- Low-Current Shutdown Mode
- Output Short Circuit Protection

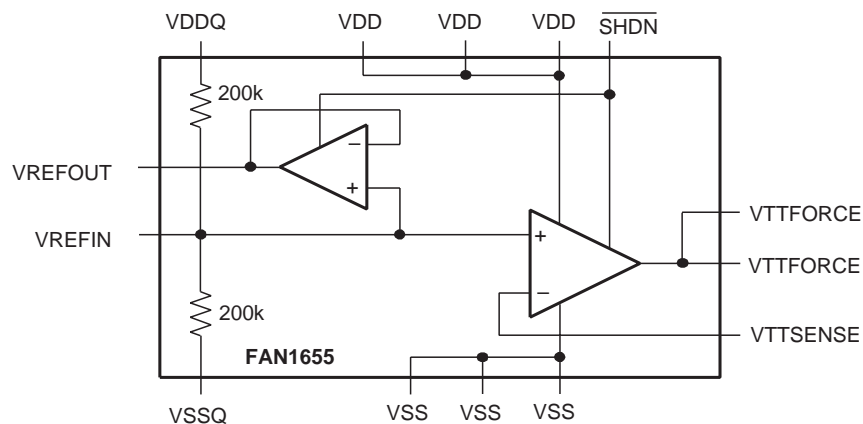
Applications

- DDR Terminator V_{TT} supply

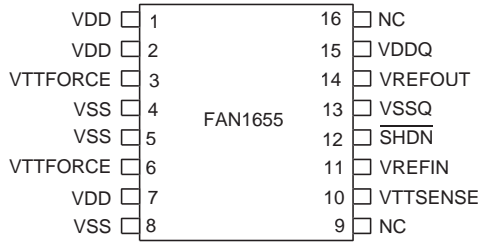
Ordering Information

| Part Number | Temperature Range | Package | Packing |
|-------------|-------------------|-----------|---------------|
| FAN1655M | 0°C to 125°C | SOIC-14 | Rails |
| FAN1655MX | 0°C to 125°C | SOIC-14 | Tape and Reel |
| FAN1655MTF | 0°C to 125°C | eTSSOP-16 | Rails |
| FAN1655MTFX | 0°C to 125°C | eTSSOP-16 | Tape and Reel |
| FAN1655MPX | 0°C to 125°C | MLP-8 | Tape and Reel |

Block Diagram

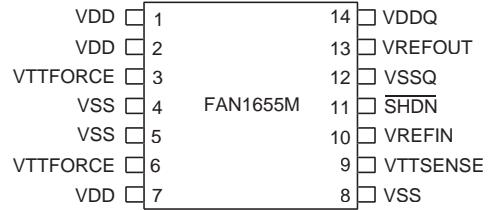


Pin Assignments

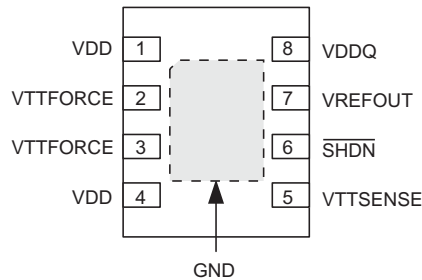


16-Lead Plastic eTSSOP-16
 $\theta_{JC} = 4^{\circ}\text{C/W}^*$

*Thermal impedance is measured with the power pad soldered to a 0.5 square inch copper area. The copper area should be connected to Vss (ground) and positioned over an internal power or ground plane to assist in heat dissipation.



14-Lead Plastic SOIC
 $\theta_{JC} = 37^{\circ}\text{C/W}, \theta_{JA} = 88^{\circ}\text{C/W}$



8-Lead MLP Package (5x6mm)
 $\theta_{JC} = 4^{\circ}\text{C/W}, \theta_{JA} = 34^{\circ}\text{C/W}$
 as measured on FAN1655MP Eval Board

Pin Definitions

| Pin | | | Pin Name | Pin Function |
|------|---------|---------|----------|--|
| MLP | eTSSOP | SOIC-14 | | |
| 1, 4 | 1, 2, 7 | 1, 2, 7 | VDD | Input power for the LDO. |
| 2, 3 | 3, 6 | 3, 6 | VTTFORCE | The VTT output voltage. |
| PAD | 4, 5, 8 | 4, 5, 8 | VSS | IC Ground. |
| 5 | 10 | 9 | VTTSENSE | Feedback for remote sense of the VTT voltage. |
| | 11 | 10 | VREFIN | Alternative input for direct control of VTTOUT and VREFOUT. |
| 6 | 12 | 11 | SHDN | Shutdown. This active low shutdown turns off both VTT and VREFOUT. This pin has an internal pull-down, and must be externally driven high for the IC to be on. |
| | 13 | 12 | VSSQ | Signal Ground. |
| 7 | 14 | 13 | VREFOUT | Buffered Voltage Reference Output. |
| 8 | 15 | 14 | VDDQ | VDDQ Input. Attach this pin to the VDDQ supply to generate VTT and VREFOUT. |
| | 9, 16 | | NC | No Internal Connection |
| PAD | PAD | | | Connect PAD to Vss Ground Plane |

Typical Application

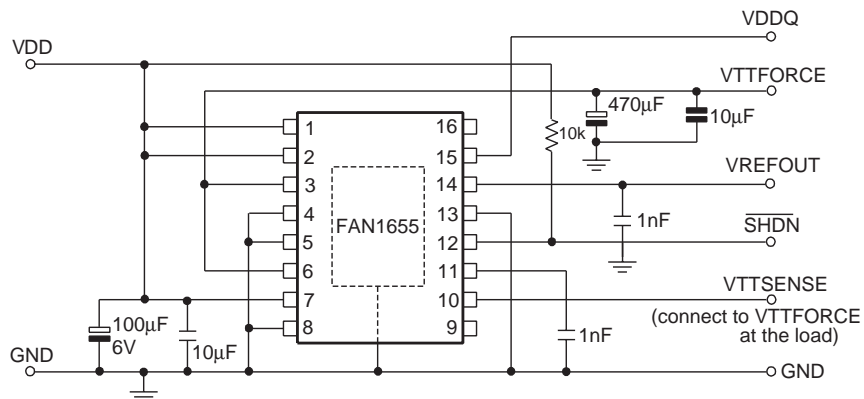


Figure 1. (eTSSOP pinout shown)

Typical Performance Characteristics

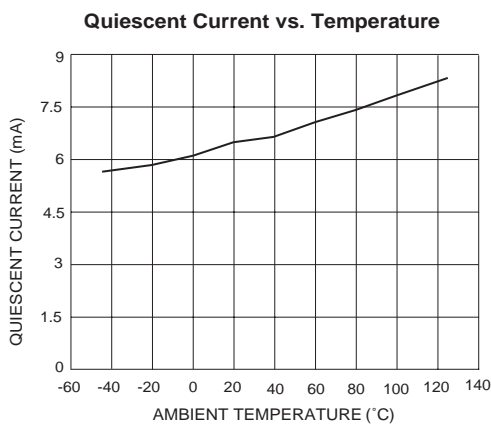


Figure 2. Quiescent Current vs. Ambient Temperature

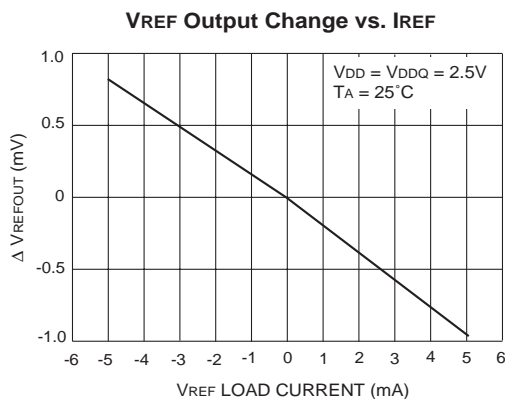


Figure 3. Reference Output Load Regulation

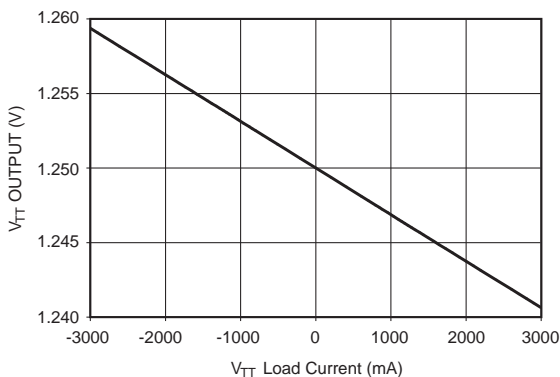


Figure 4. VTT Load Regulation

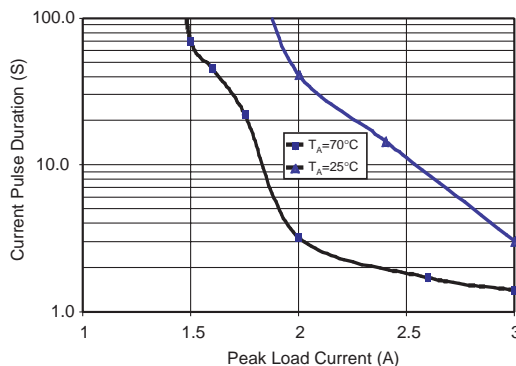


Figure 5. Maximum Non-Repetitive Output Current vs. Pulse Width (FAN1655M SO-14 Package)

Absolute Maximum Ratings

| | | |
|--|----------------------|--------------------------------------|
| Supply Voltage VDD, VDDQ | | 6V |
| Junction Temperature, T _J | | 150°C |
| Storage Temperature | | -65 to 150°C |
| Lead Soldering Temperature, 10 seconds | | 300°C |
| Power Dissipation, P _D | FAN1655M (SOIC-14) | 1.4W |
| | FAN1655MTF (e-TSSOP) | See "Power Dissipation and Derating" |
| | FAN1655MP (MLP) | |

Recommended Operating Conditions

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------|------------|------|------|------|-------|
| Supply Voltage VDD | | 2.3 | 2.5 | 3.6 | V |
| Supply Voltage VDDQ | | 2.2 | 2.5 | 3.0 | V |
| Ambient Operating Temperature | | 0 | | 125 | °C |
| VREFIN | | 1.1 | 1.25 | 1.5 | V |

Electrical Characteristics

(VDD = VDDQ = 2.5V ± 0.2V, and T_A = 25°C using circuit in Figure 1, unless otherwise noted.)

The • denotes specifications which apply over the specified operating temperature range.

| Parameter | Conditions | Min. | Typ. | Max. | Units | |
|--|--|-------------------|-------|-------|-------|---|
| VTT Output Voltage | I _{OUT} = 0A, VREFIN = open | VDDQ = 2.3V • | 1.135 | 1.150 | 1.165 | V |
| | | VDDQ = 2.5V • | 1.235 | 1.250 | 1.265 | V |
| | | VDDQ = 2.7V • | 1.335 | 1.350 | 1.365 | V |
| | I _{OUT} = ±2.1A, VREFIN = open | VDDQ = 2.3V | 1.110 | 1.150 | 1.190 | V |
| | | VDDQ = 2.5V | 1.210 | 1.250 | 1.290 | V |
| | | VDDQ = 2.7V | 1.310 | 1.350 | 1.390 | V |
| VTT Output Slew Rate | C _{load} = 10μF | | 0.3 | | V/μS | |
| VTT Leakage Current | $\overline{\text{SHDN}}$ = 0V | • | -50 | 50 | μA | |
| VTT Current Limit | | | ±3.1 | | A | |
| VREFIN Input Impedance | | | 100 | | KΩ | |
| VREFOUT Output Voltage | No load | VREFIN = 1.150V • | 1.145 | 1.150 | 1.155 | V |
| | | VREFIN = 1.250V • | 1.245 | 1.250 | 1.255 | V |
| | | VREFIN = 1.350V • | 1.345 | 1.350 | 1.355 | V |
| VREFOUT Output Current | VDDQ = 2.3V | • | -5 | 5 | mA | |
| VREFOUT Leakage Current | $\overline{\text{SHDN}}$ = 0V | • | -10 | 10 | μA | |
| $\overline{\text{SHDN}}$ Logic High | | • | 1.667 | | V | |
| $\overline{\text{SHDN}}$ Logic Low | | • | | 0.800 | V | |
| IDD Supply Current | No load, $\overline{\text{SHDN}}$ = 2.7V | • | 7.5 | 20 | mA | |
| VDDQ Leakage Current | $\overline{\text{SHDN}}$ = 0V | • | 6 | 10 | μA | |
| VDD Leakage Current | $\overline{\text{SHDN}}$ = 0V | • | 3 | 50 | μA | |
| $\overline{\text{SHDN}}$ Input Current | $\overline{\text{SHDN}}$ = 2.7V | • | 50 | 75 | μA | |
| Over-Temperature Shutdown | | | 155 | | °C | |
| Over-Temperature Hysteresis | | | 30 | | °C | |

Applications Information

Output Capacitor selection

The JEDEC specification for DDR termination requires that VTT stay within $\pm 40\text{mV}$ of VREF, which must track VDDQ/2 within 1%. During the initial load transient, the output capacitor keeps the output within spec. To stay within the 40mV window, the “load step” due to the load transient current dropping across the output capacitor’s ESR should be kept to around 25mV: where $\text{ESR} <$

$\frac{25}{\Delta I}$ is given in $\text{m}\Omega$, and ΔI is the maximum load current.

For example, to handle a 3A maximum load transient, the ESR should be no greater than $8\text{m}\Omega$. Furthermore, the output capacitor must be able to hold the load in spec while the regulator recovers (about $15\mu\text{S}$). A minimum value of $470\mu\text{F}$ is recommended.

The FAN1655 requires a minimum of $100\mu\text{F}$ of input capacitance with a maximum ESR value of $100\text{m}\Omega$ to insure stability.

Power Dissipation and Derating

The maximum output current (sink or source) for a 1.25V output is:

$$I_{\text{OUT(MAX)}} = \frac{P_{\text{D(MAX)}}}{1.25}$$

where $P_{\text{D(MAX)}}$ is the maximum power dissipation which is:

$$P_{\text{D(MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{\theta_{\text{JA}}}$$

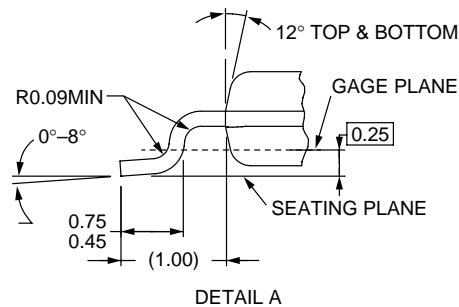
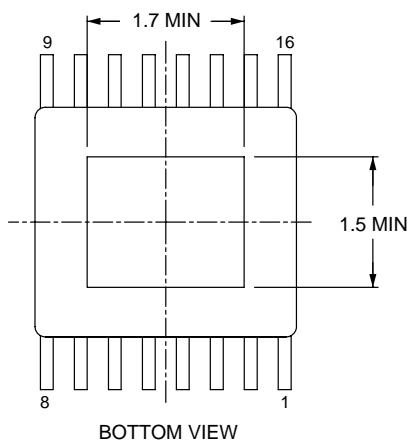
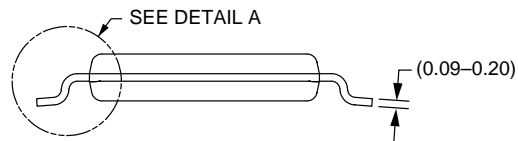
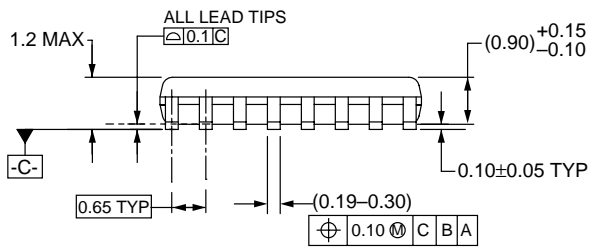
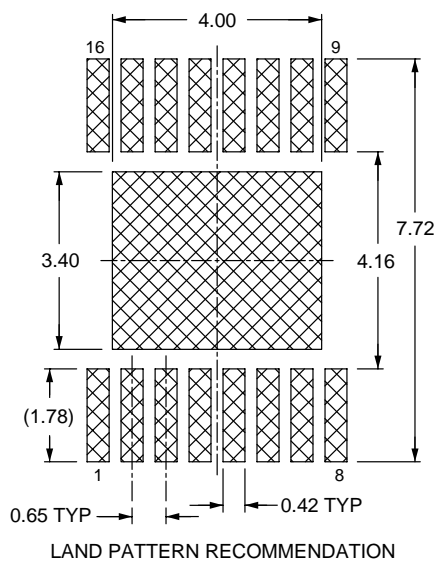
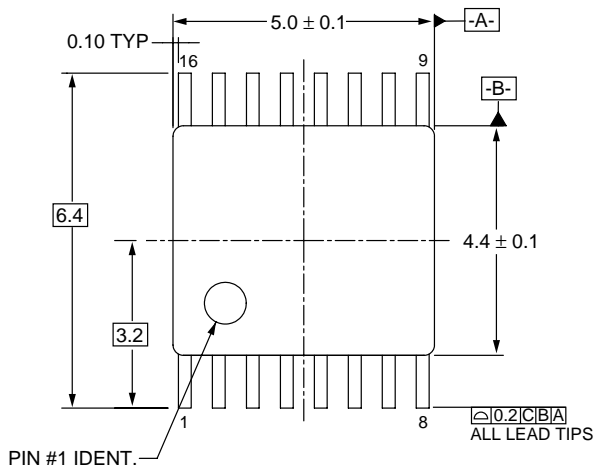
where $T_{\text{J(MAX)}}$ is the maximum die temperature of the IC and T_{A} is the operating ambient temperature.

FAN1655 has an internal thermal limit at 150°C , which defines $T_{\text{J(MAX)}}$. For the SOIC-14 package, θ_{JA} is given at 88°C/W . Using equation 2, the maximum dissipation at $T_{\text{A}} = 25^{\circ}\text{C}$ is 1.4W , which is its rated maximum dissipation.

The e-TSSOP or MLP package, however, use the PCB copper to cool the IC through the thermal pad on the package bottom. For maximum dissipation, this pad should be soldered to the PCB copper, with as much copper area as possible surrounding it to cool the package. Thermal vias should be placed as close to the thermal pad as possible to transfer heat to other layers of copper on the PCB. With large areas of PCB copper for heat sinking, a θ_{JA} of under 40°C/W can easily be achieved.

Mechanical Dimensions

16-Lead eTSSOP

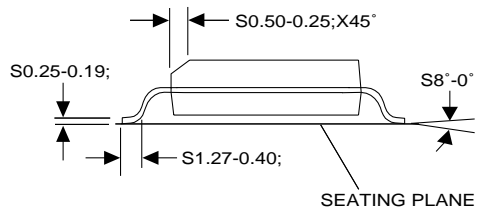
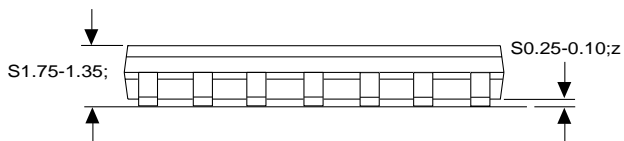
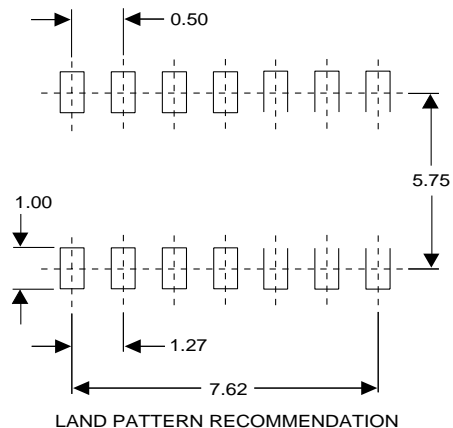
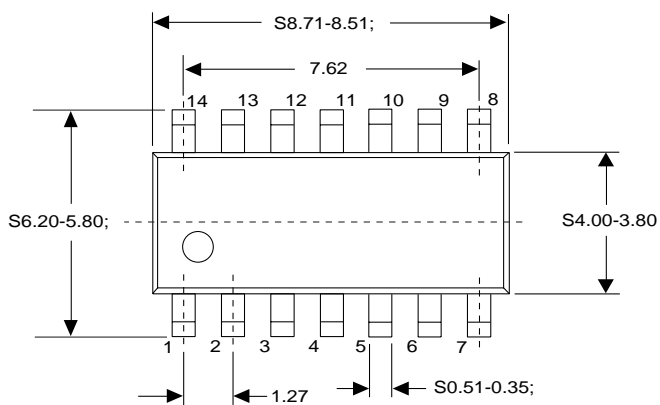


NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABT, DATED 10/97.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND THE BAR EXTENSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

Mechanical Dimensions

14-Lead SOIC

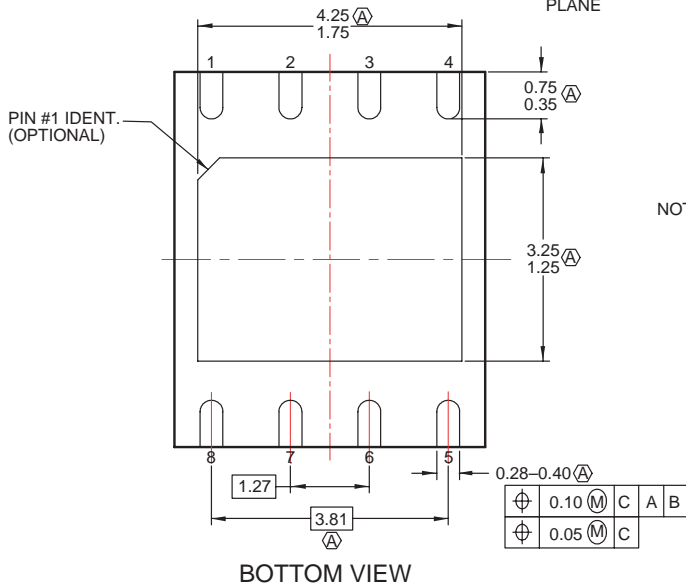
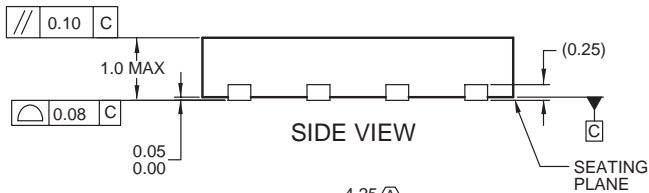
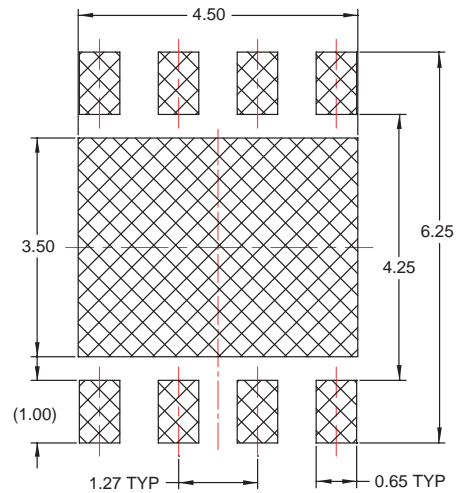
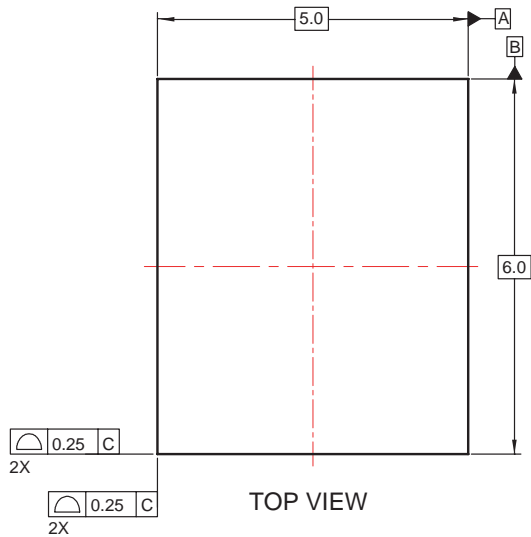


Notes:

1. This package conforms to JEDEC MS-012, variation AB, ISSUEC dated May, 1990.
2. All dimensions are in millimeters
3. Standard lead finished
200 microinches / 5.08 microns min.
Lead/Tin (solder) oncopper

Mechanical Dimensions

5mm x 6mm 8-Lead MLP



- NOTES:
- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229, DATED 11/2001.
 - B) DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCES PER ASME Y14.5-1994.

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Rev. 117

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