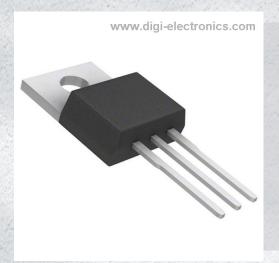


## FCP110N65F Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number FCP110N65F-DG

Manufacturer onsemi

Manufacturer Product Number FCP110N65F

Description MOSFET N-CH 650V 35A TO220-3

Detailed Description N-Channel 650 V 35A (Tc) 357W (Tc) Through Hole

TO-220-3



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RFQ Email: Info@DiGi-Electronics.com

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## **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:
FCP110N65F	onsemi
Series:	Product Status:
FRFET®, SuperFET® II	Not For New Designs
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
650 V	35A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ ld, Vgs:
10V	110mOhm @ 17.5A, 10V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
5V @ 3.5mA	145 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	4895 pF @ 100 V
FET Feature:	Power Dissipation (Max):
	357W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Supplier Device Package:	Package / Case:
TO-220-3	TO-220-3
Base Product Number:	
FCP110	

## **Environmental & Export classification**

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	Not Applicable
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	



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December 2014

## **FCP110N65F**

# N-Channel SuperFET<sup>®</sup> II FRFET<sup>®</sup> MOSFET 650 V, 35 A, 110 m $\Omega$

### **Features**

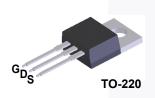
- 700 V @ T<sub>J</sub> = 150°C
- Typ.  $R_{DS(on)}$  = 96 m $\Omega$  (Typ.)
- Ultra Low Gate Charge (Typ. Q<sub>q</sub> = 98 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 464 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

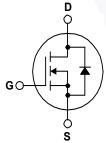
## **Applications**

- LCD / LED / PDP TV Telecom / Server Power Supplies
- · Solar Inverter
- AC DC Power Supply

## **Description**

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FCP110N65F	Unit
V <sub>DSS</sub>	Drain to Source Voltage			650	V
V	Cata to Course Valtage	- DC		±20	V
$V_{GSS}$	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	V
	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		35	А
'D	Diam Current	- Continuous (T <sub>C</sub> = 100°C)		24	A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	105	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (No		(Note 2)	809	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	8	Α
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	3.57	mJ
dv/dt	MOSFET dv/dt			100	V/ns
uv/ut	Peak Diode Recovery dv/dt		(Note 3)	50	V/IIS
D	Payer Dissination	(T <sub>C</sub> = 25°C)		357	W
$P_{D}$	Power Dissipation	- Derate Above 25°C		2.86	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperat	ure Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for 1/8" from Case for 5 Seconds	Soldering,		300	°C

### **Thermal Characteristics**

Symbol	Parameter	FCP110N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	*C/W

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP110N65F	FCP110N65F	TO-220	Tube	N/A	N/A	50 units

**Test Conditions** 

Min.

Тур.

Max. Unit

## **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted. Parameter

Off Chara	acteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	650	-	-	W
BV <sub>DSS</sub> Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	v	
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μА
I <sub>DSS</sub> Zero Gate Voltage Drain Current	$V_{DS} = 520 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	110	-	μΑ	
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

#### **On Characteristics**

Symbol

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 3.5 \text{ mA}$	3	-	5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 17.5 \text{ A}$	-	96	110	mΩ
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 17.5 A	-	30	1	S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 400 V V - 0 V	\ -	3680	4895	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz	-	110	145	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12	-	0.65	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 380 V, V <sub>GS</sub> = 0 V, f = 1 MHz	- \	65	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	464	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	$V_{DS} = 380 \text{ V}, I_{D} = 17.5 \text{ A},$	-	98	145	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V	-	20	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note 4)	-	43	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.7	-	Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	31	72	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_{D} = 17.5 \text{ A},$	- /	21	52	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_g$ = 4.7 $\Omega$	-	89	188	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	5.7	21	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	35	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	105	Α
$V_{SD}$	Drain to Source Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A		-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A,	-	133	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	0.67	-	μС

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I<sub>AS</sub> = 8 A, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- 3. I  $_{SD} \leq$  17.5 A, di/dt  $\leq$  200 A/µs, V  $_{DD} \leq$  380 V, starting T  $_{J}$  = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

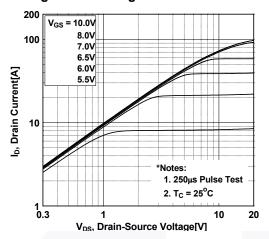


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

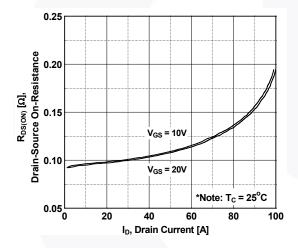


Figure 5. Capacitance Characteristics

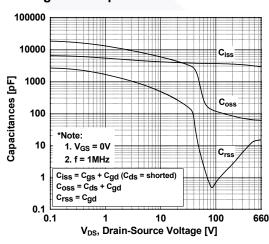


Figure 2. Transfer Characteristics

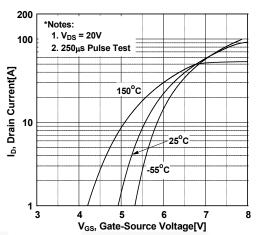


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

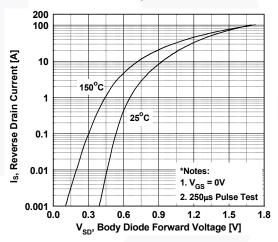
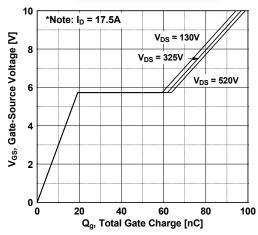


Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

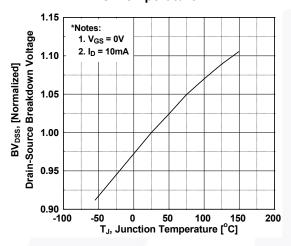


Figure 9. Maximum Safe Operating Area

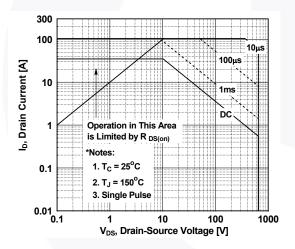


Figure 11. Eoss vs. Drain to Source Voltage

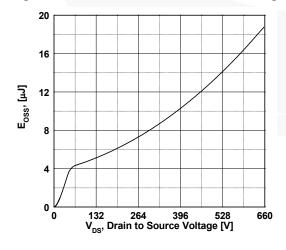


Figure 8. On-Resistance Variation vs. Temperature

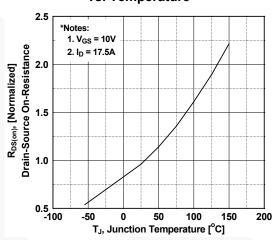
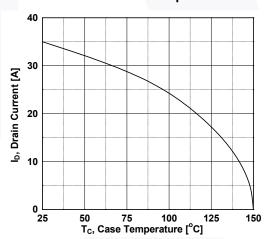
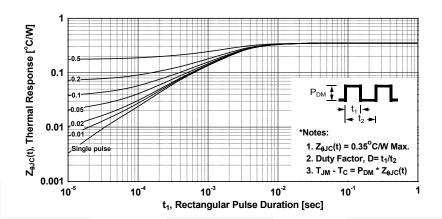


Figure 10. Maximum Drain Current vs. Case Temperature



## **Typical Performance Characteristics** (Continued)

Figure 12. Transient Thermal Response Curve



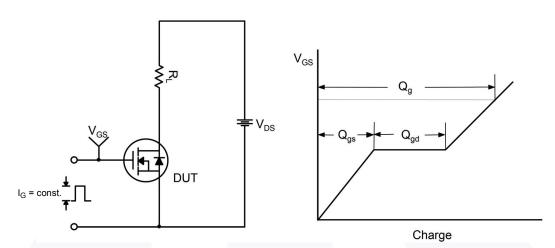


Figure 13. Gate Charge Test Circuit & Waveform

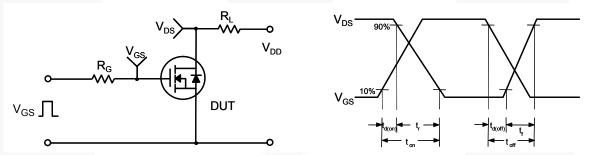


Figure 14. Resistive Switching Test Circuit & Waveforms

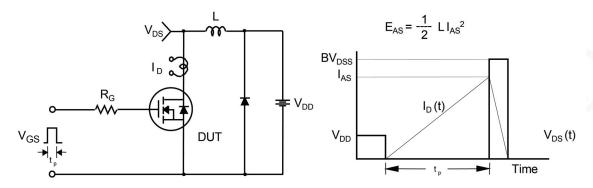


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

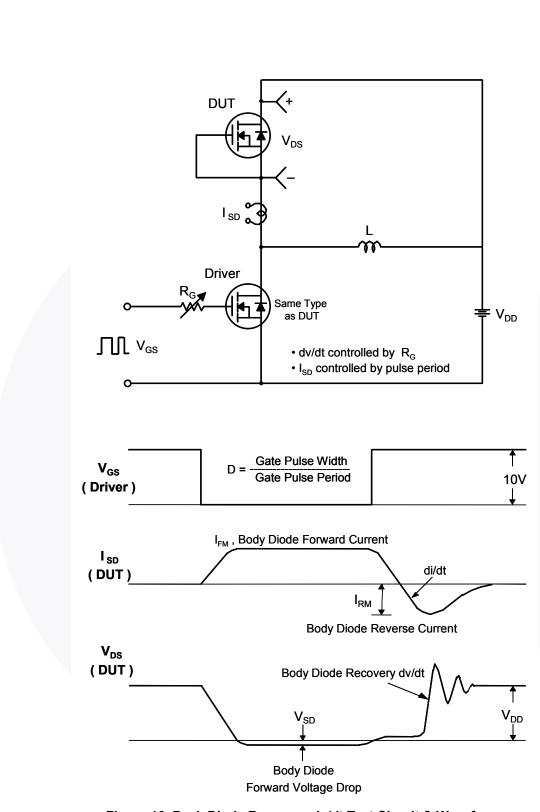
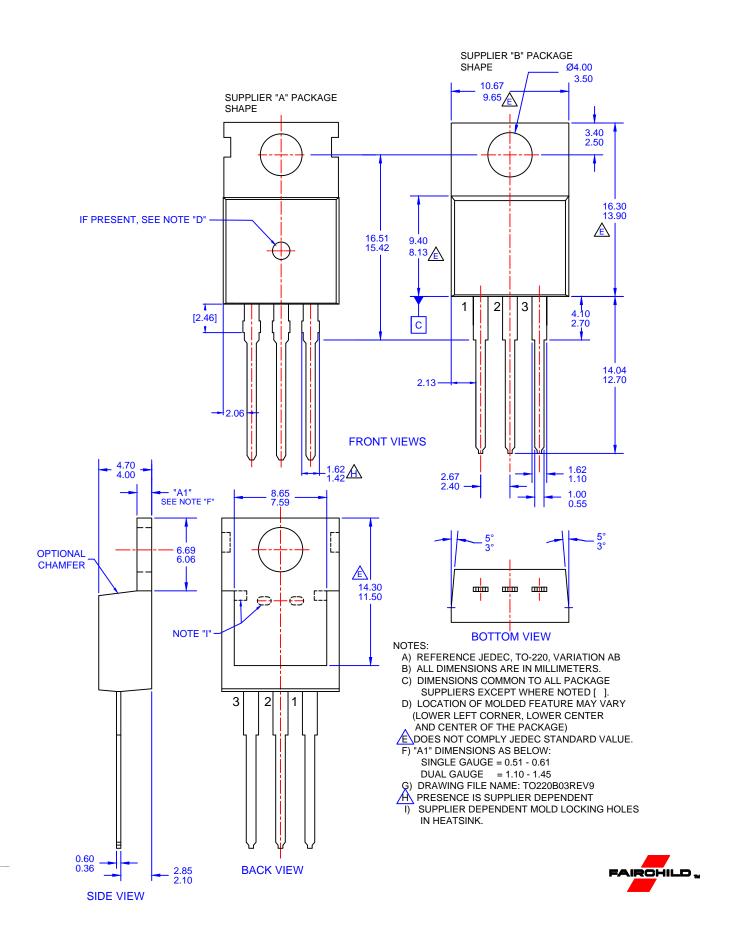


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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