FDC6306P Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	FDC6306P-DG
Manufacturer	onsemi
Manufacturer Product Number	FDC6306P
Description	MOSFET 2P-CH 20V 1.9A SSOT6
Detailed Description	Mosfet Array 20V 1.9A 700mW Surface Mount SuperSOT™-6

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDC6306P	onsemi
Series:	Product Status:
PowerTrench®	Active
Technology:	Configuration:
MOSFET (Metal Oxide)	2 P-Channel (Dual)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	20V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
1.9A	170mOhm @ 1.9A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
1.5V @ 250μA	4.2nC @ 4.5V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
441pF @ 10V	700mW
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
SOT-23-6 Thin, TSOT-23-6	SuperSOT™-6
Base Product Number:	
FDC6306	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.21.0095	

DATA SHEET
www.onsemi.com

MOSFET– Specified, Dual P-Channel, POWERTRENCH®

2.5 V

FDC6306P

General Description

These P−Channel 2.5 V specified MOSFETs are produced using **onsemi**’s advanced PowerTrench process that has been especially tailored to minimize on−state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO−8 and TSSOP−8 packages are impractical.

Features

- −1.9 A, −20 V. $R_{DS(ON)} = 0.170\ \Omega$ @ $V_{GS} = -4.5$ V
  $R_{DS(ON)} = 0.250\ \Omega$ @ $V_{GS} = -2.5$ V
- Low Gate Charge (3 nC Typical)
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SuperSOT™−6 Package: Small Footprint (72% Smaller than Standard SO−8); Low Profile (1 mm Thick).
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Load Switch
- Battery Protection
- Power Management

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

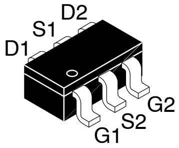
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−Source Voltage	−20	V
V_{GSS}	Gate−Source Voltage	±8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	−1.9 −5	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	 0.96 0.9 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

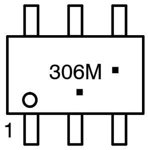
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	60	°C/W

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−20 V	0.170 Ω @ −4.5 V 0.250 Ω @ −2.5 V	−1.9 A



TSOT23 6−Lead
SUPERSOT−6
CASE 419BL

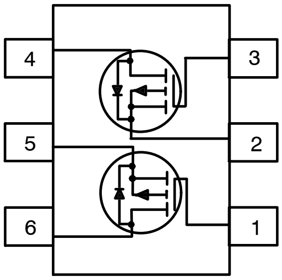
MARKING DIAGRAM



306 = Specific Device Code
M = Assembly Operation Month
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
FDC6306P	TSOT23 6−Lead (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

January, 2024 − Rev. 3

Publication Order Number:
FDC6306P/D

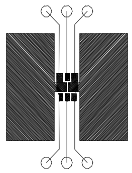
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	–18	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSSF}	Gate to Source Leakage Current, Forward	V_{GS} = 8 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate to Source Leakage Current, Reverse	V_{GS} = –8 V, V_{DS} = 0 V	–	–	–100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.9	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	3	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –1.9 A V_{GS} = –4.5 V, I_D = –1.9 A @ T_J = 125°C V_{GS} = –2.5 V, I_D = –1.7 A	– – –	0.127 0.182 0.194	0.170 0.270 0.250	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–5	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –1.9 A	–	4	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz	–	441	–	pF
C_{oss}	Output Capacitance		–	127	–	pF
C_{rss}	Reverse Transfer Capacitance		–	67	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –10V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω	–	6	12	ns
t_r	Turn-On Rise Time		–	9	18	ns
$t_{d(off)}$	Turn-Off Delay Time		–	14	25	ns
t_f	Turn-Off Fall Time		–	3	9	ns
$Q_{g(Tot)}$	Total Gate Charge	V_{DS} = –10 V, I_D = –1.9 A, V_{GS} = –4.5 V	–	3	4.2	nC
Q_{gs}	Gate–Source Charge		–	0.7	–	nC
Q_{gd}	Gate–Drain Charge		–	0.8	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.8	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.8 A (Note 2)	–	–0.8	–1.2	V

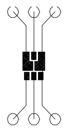
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

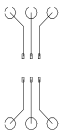
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a. 130°C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b. 140°C/W when mounted on a 0.005 in^2 pad of 2 oz. copper.



c. 180 °C/W when mounted on a 0.0015 in2 pad of 2 oz. copper.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

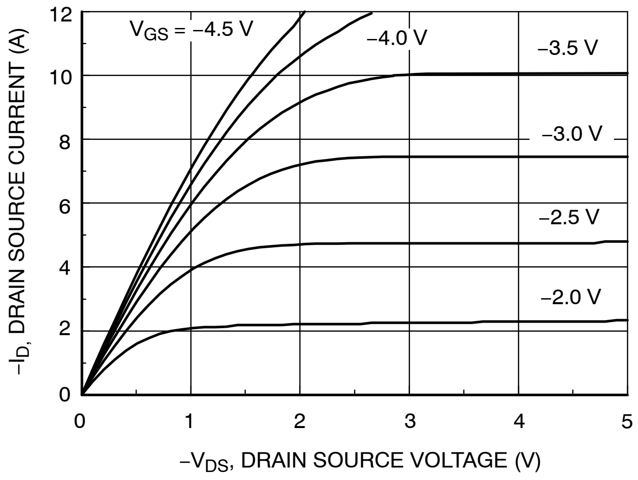


Figure 1. On−Region Characteristics

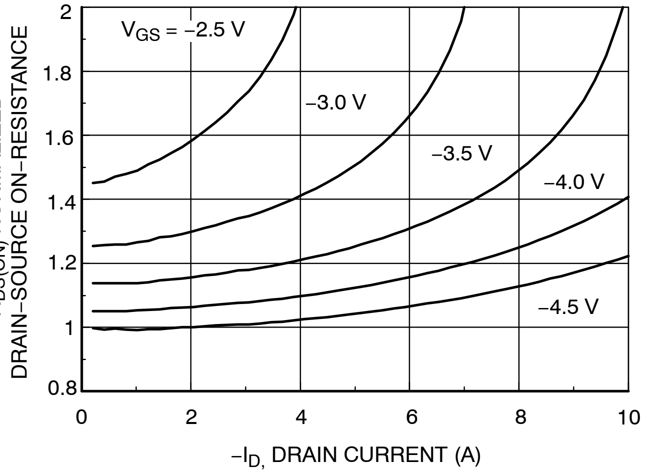


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

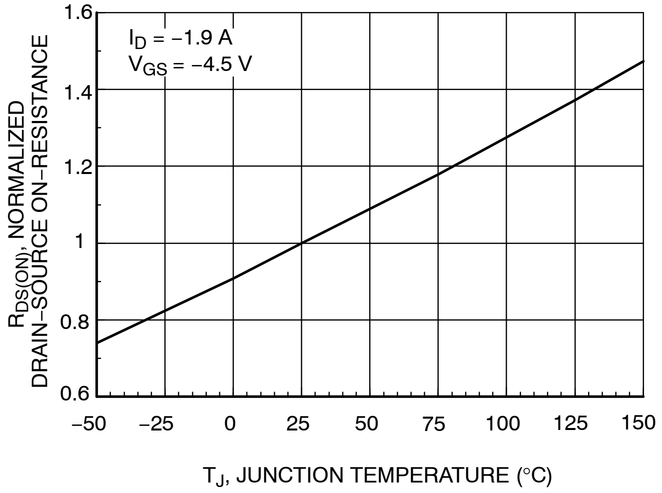


Figure 3. On−Resistance Variation with Temperature

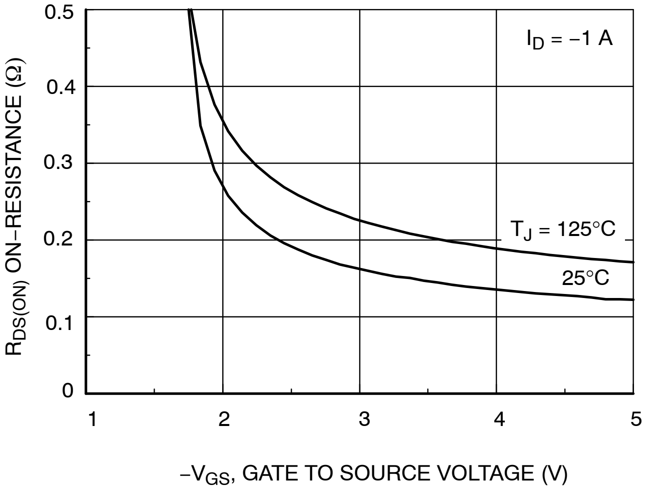


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

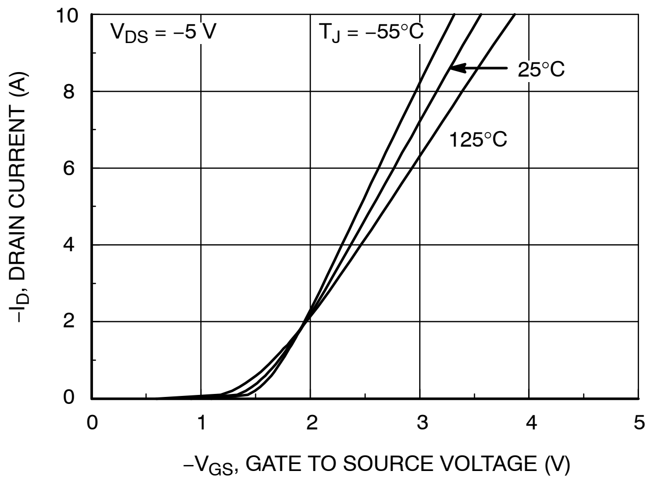


Figure 5. Transfer Characteristics

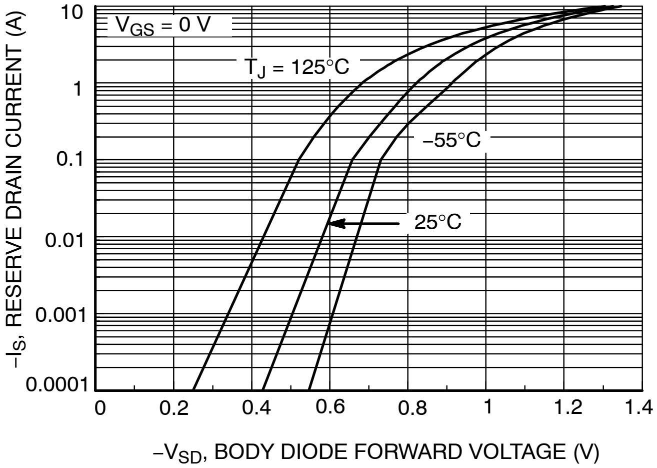


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

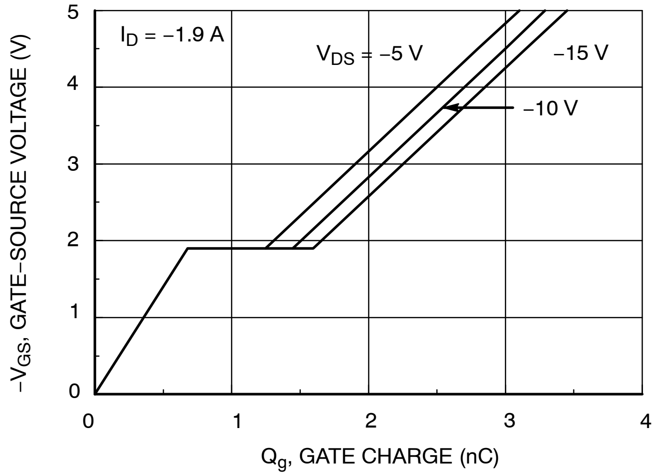


Figure 7. Gate Charge Characteristics

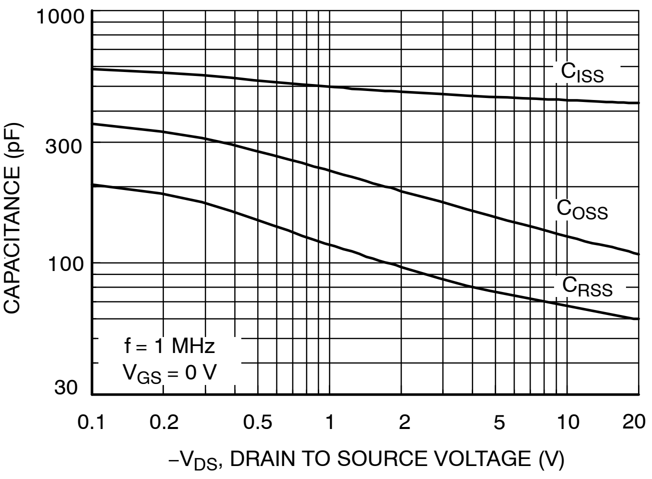


Figure 8. Capacitance Characteristics

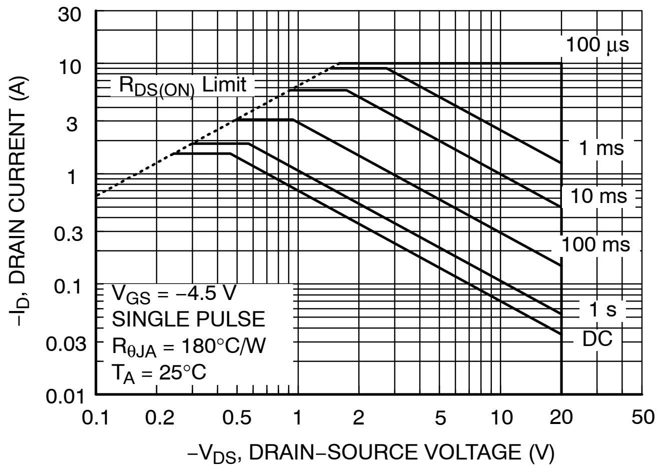


Figure 9. Maximum Safe Operating Area

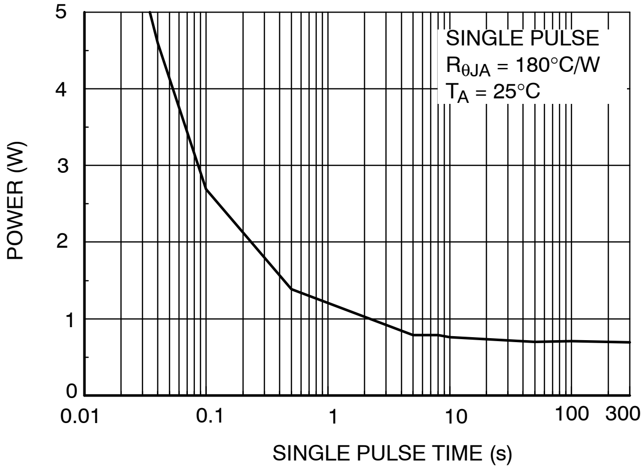


Figure 10. Single Pulse Maximum Power Dissipation

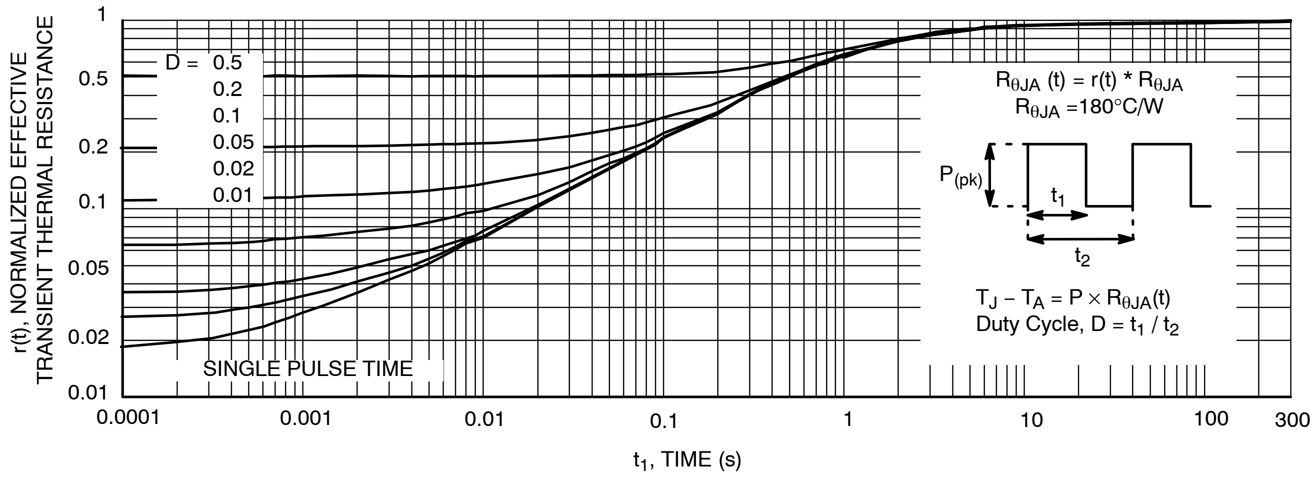


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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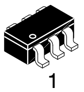
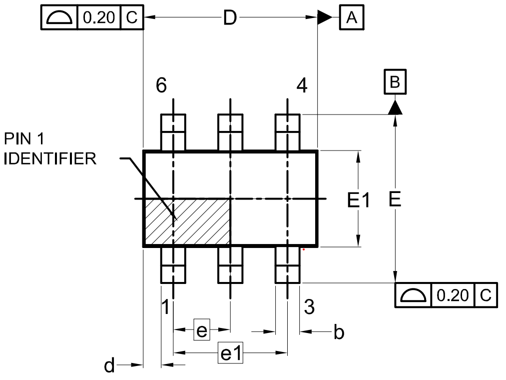
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSOT23 6-Lead
CASE 419BL
ISSUE A

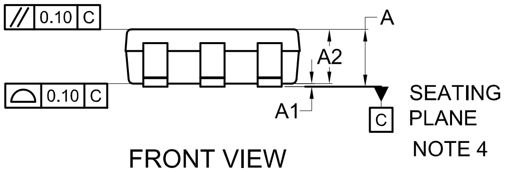
DATE 31 AUG 2020



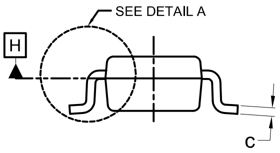
SCALE 2:1



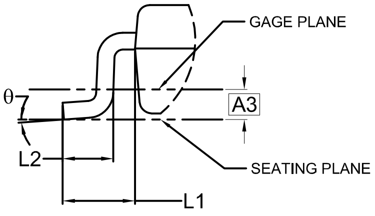
TOP VIEW



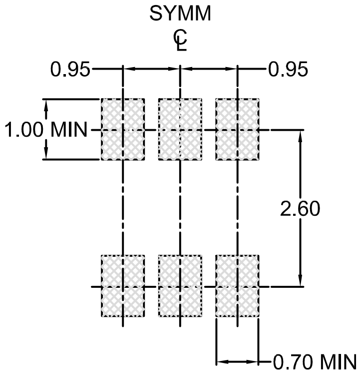
FRONT VIEW



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

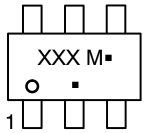
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
ϴ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

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