FDMA1029PZ Datasheet

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DiGi Electronics Part Number	FDMA1029PZ-DG
Manufacturer	onsemi
Manufacturer Product Number	FDMA1029PZ
Description	MOSFET 2P-CH 20V 3.1A 6WDFN
Detailed Description	Mosfet Array 20V 3.1A 700mW Surface Mount 6-WDFN (2x2)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDMA1029PZ	onsemi
Series:	Product Status:
PowerTrench®	Active
Technology:	Configuration:
MOSFET (Metal Oxide)	2 P-Channel (Dual)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	20V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
3.1A	95mOhm @ 3.1A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
1.5V @ 250µA	10nC @ 4.5V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
540pF @ 10V	700mW
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
6-WDFN Exposed Pad	6-WDFN (2x2)
Base Product Number:	
FDMA1029	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.21.0095	

DATA SHEET
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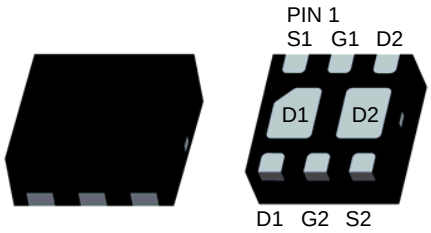
MOSFET – Dual, P-Channel, POWERTRENCH®

-20 V, -3.1 A, 95 Ω

FDMA1029PZ

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
−20 V	95 mΩ @ −4.5 V	−3.1 A
	141 mΩ @ −2.5 V	



WDFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 511DA

General Description

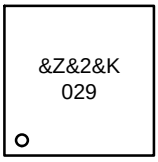
This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra−portable applications. It features two independent P−Channel MOSFETs with low on−state resistance for minimum conduction losses. When connected in the typical common source configuration, bi−directional current flow is possible.

The MicroFET ™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications

Features

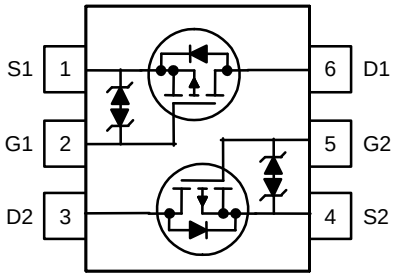
- –3.1 A, –20 V
  - $R_{DS(ON)}$ = 95 mΩ @ V_{GS} = –4.5 V
  - $R_{DS(ON)}$ = 141 mΩ @ V_{GS} = –2.5 V
- Low Profile – 0.8 mm maximum – in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2.5 kV (Note 3)
- Free from halogenated compounds and antimony oxides
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
029 = Specific Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain−Source Voltage	−20	V
V_{GS}	Gate−Source Voltage	±12	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 −3.1 −6	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	 1.4 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	86 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	173 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	69 (Dual Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	151 (Dual Operation)	

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

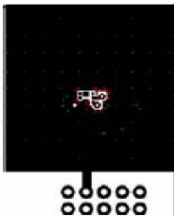
FDMA1029PZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

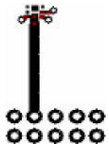
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	–12	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.6	–1.0	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	4	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –3.1 A V_{GS} = –2.5 V, I_D = –2.5 A V_{GS}= –4.5 V, I_D = –3.1 A, T_J = 125°C	– – –	60 88 87	95 141 140	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –3.1 A	–	–11	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz	–	540	–	pF
C_{oss}	Output Capacitance		–	120	–	pF
C_{rss}	Reverse Transfer Capacitance		–	100	–	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω	–	13	24	ns
t_r	Turn–On Rise Time		–	11	20	ns
$t_{d(off)}$	Turn–Off Delay Time		–	37	59	ns
t_f	Turn–Off Fall Time		–	36	58	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –3.1 A, V_{GS} = –4.5 V	–	7.0	10	nC
Q_{gs}	Gate–Source Charge		–	1.1	–	nC
Q_{gd}	Gate–Drain Charge		–	2.4	–	nC
DRAIN−SOURCE CHARACTERISTICS						
I_S	Maximum Continuous Source–Drain Diode Forward Current		–	–	–1.1	A
V_{SD}	Source–Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.1 A (Note 2)	–	–0.8	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –3.1 A, dI_F/dt = 100 A/μs	–	25	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	9	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

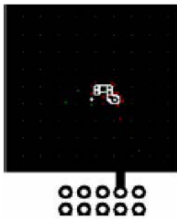
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a) $R_{\theta JA}$ = 86°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
   (b) $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   (c) $R_{\theta JA}$ = 69°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
   (d) $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



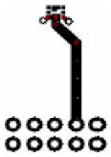
a. 86°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 173°C/W when mounted on a minimum pad of 2 oz copper.



c. 69°C/W when mounted on a 1 in^2 pad of 2 oz copper.



d. 151°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

FDMA1029PZ

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

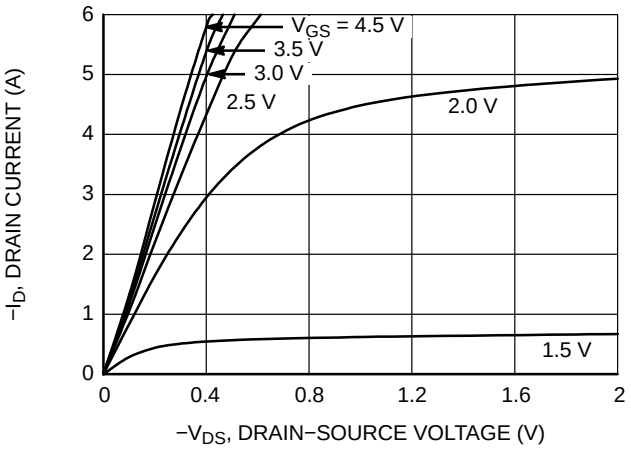


Figure 1. On−Region Characteristics

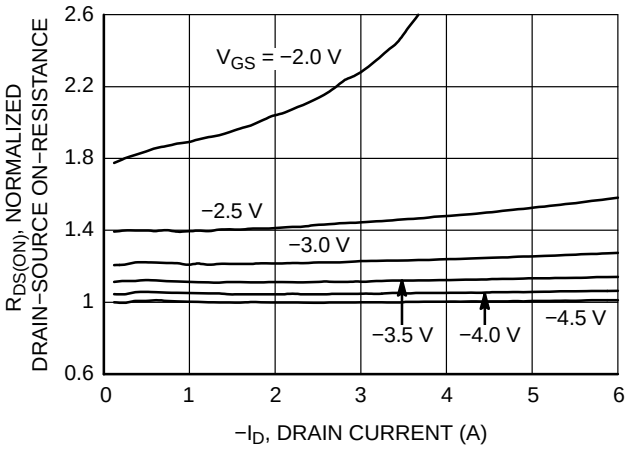


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

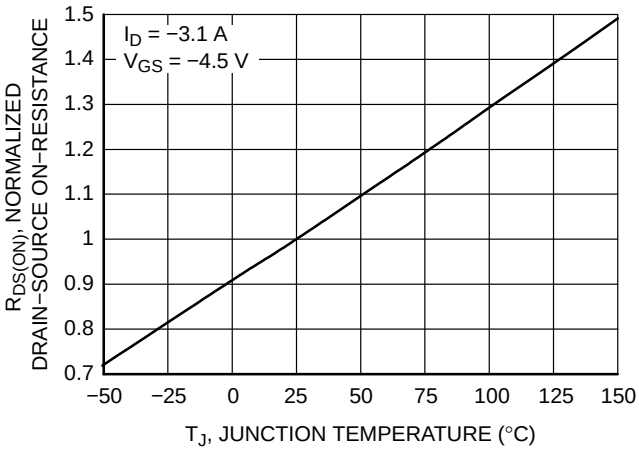


Figure 3. On−Resistance Variation with Temperature

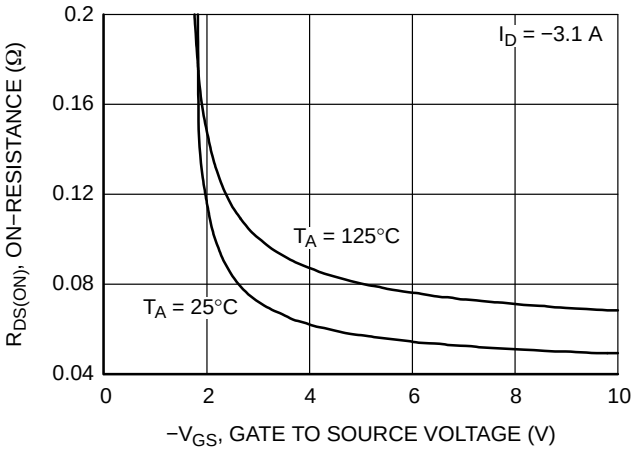


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

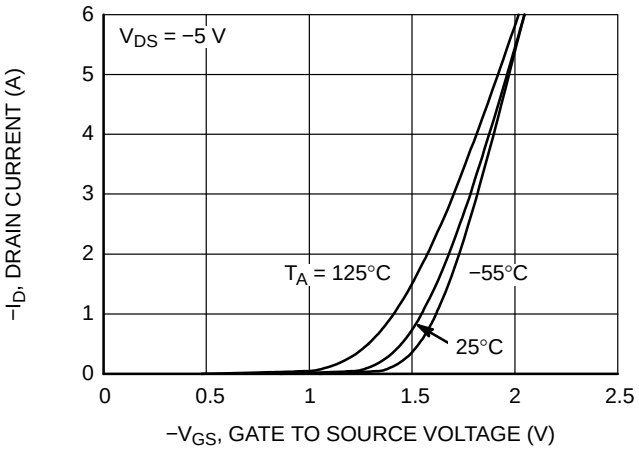


Figure 5. Transfer Characteristics

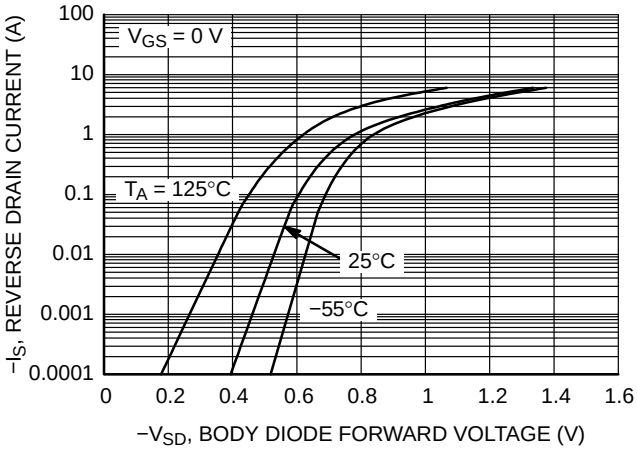


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

FDMA1029PZ

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

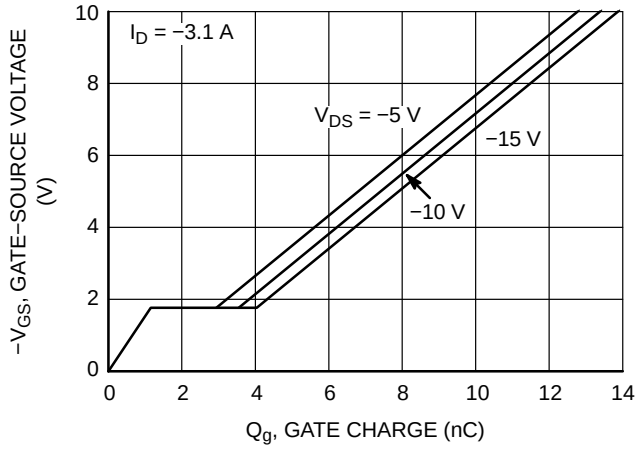


Figure 7. Gate Charge Characteristics

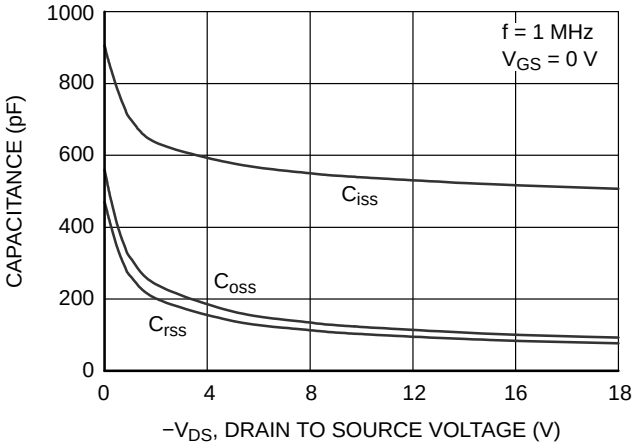


Figure 8. Capacitance Characteristics

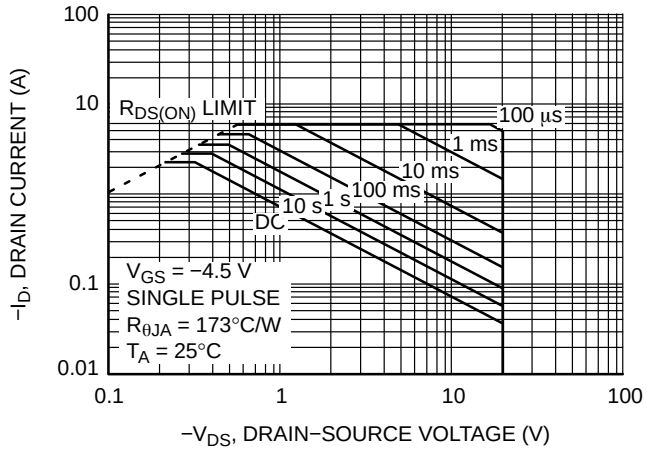


Figure 9. Maximum Safe Operating Area

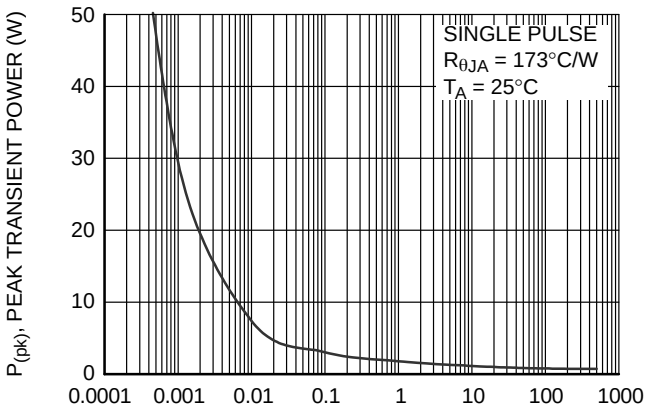


Figure 10. Single Pulse Maximum Power Dissipation

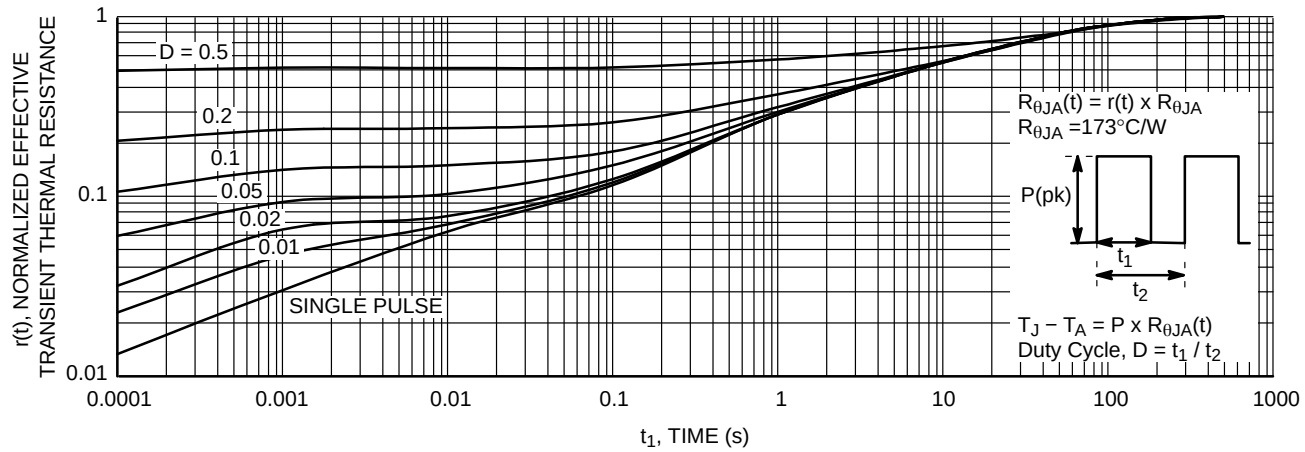


Figure 11. Transient Thermal Response Curve

(Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.)

FDMA1029PZ

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMA1029PZ	029	WDFN6 2x2, 0.65P (MicroFET 2x2) (Pb−Free, Halide Free)	7”	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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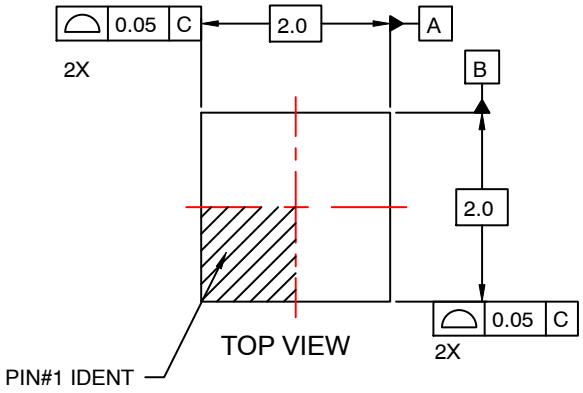
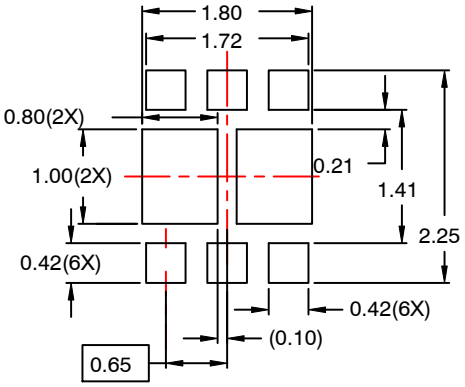
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

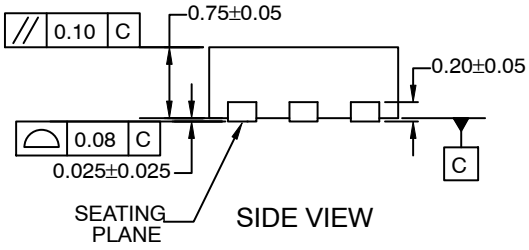
WDFN6 2x2, 0.65P
CASE 511DA
ISSUE O

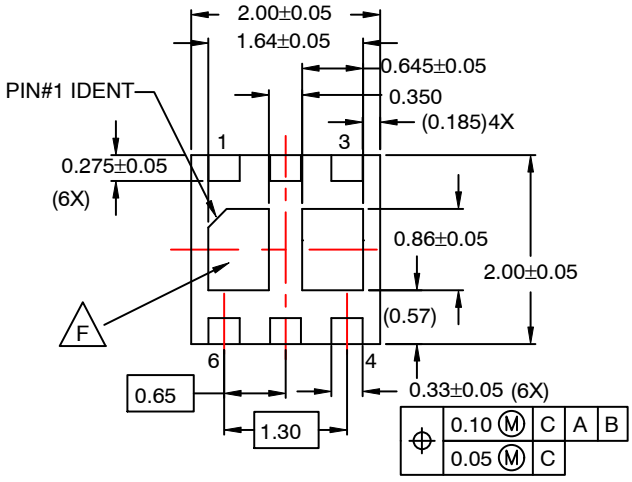
DATE 31 JUL 2016





RECOMMENDED
LAND PATTERN





NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO−229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

F. NON−JEDEC DUAL DAP

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DESCRIPTION:	**WDFN6 2X2, 0.65P**	**PAGE 1 OF 1**

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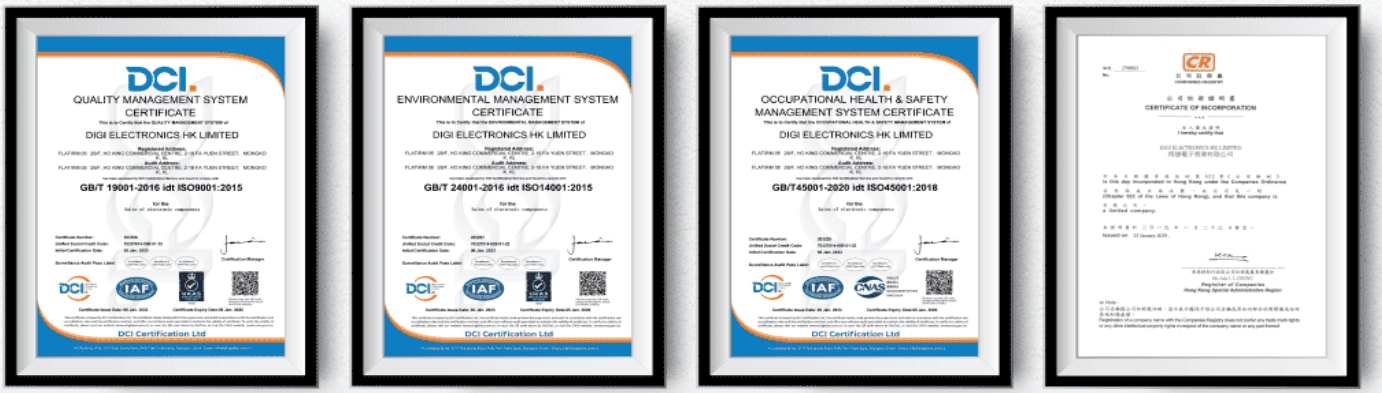

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