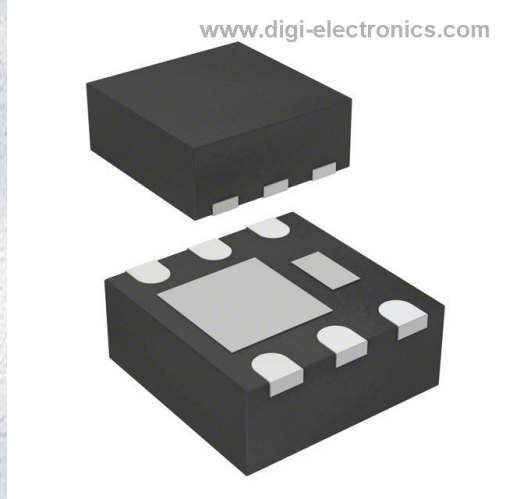
FDMA86551L Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	FDMA86551L-DG
Manufacturer	onsemi
Manufacturer Product Number	FDMA86551L
Description	MOSFET N-CH 60V 7.5A 6MICROFET
Detailed Description	N-Channel 60 V 7.5A (Ta) 2.4W (Ta) Surface Mount 6-MicroFET (2x2)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDMA86551L	onsemi
Series:	Product Status:
PowerTrench®	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
60 V	7.5A (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	23mOhm @ 7.5A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
3V @ 250µA	17 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	1235 pF @ 30 V
FET Feature:	Power Dissipation (Max):
-	2.4W (Ta)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
6-MicroFET (2x2)	6-WDFN Exposed Pad
Base Product Number:	
FDMA86551	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

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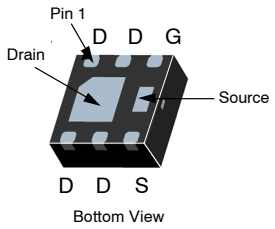
DATA SHEET
www.onsemi.com

MOSFET – Single N-Channel, POWERTRENCH®

60 V, 7.5 A, 23 mΩ

FDMA86551L



WDFN6 2x2, 0.65P
CASE 511DB

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $R_{DS(on)}$ and gate charge provide excellent switching performance.

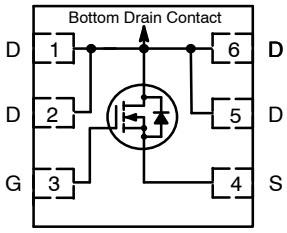
Features

- Max $R_{DS(on)}$ = 23 mΩ @ V_{GS} = 10 V, I_D = 7.5 A
- Max $R_{DS(on)}$ = 35 mΩ @ V_{GS} = 4.5 V, I_D = 6 A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET™ 2x2 mm
- This Device is Pb–Free, Halide Free and RoHS Compliant

Applications

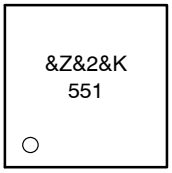
- DC–DC Buck Converters

PIN CONNECTIONS



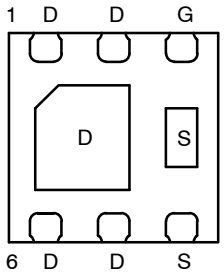
Top View

MARKING DIAGRAM



&Z	= Assembly Plant Code
&2	= Data Code (Year & Week)
&K	= Lot Run Code
551	= Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous (Note 1a) T_A = 25°C – Pulsed (Note 4)	 7.5 45	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	37	mJ
P_D	Power Dissipation (Note 1a) T_A = 25°C Power Dissipation (Note 1b) T_A = 25°C	2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

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FDMA86551L

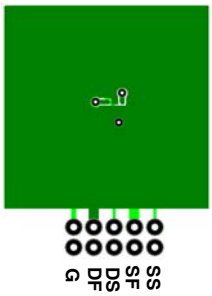
ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	31	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	–5	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7.5 A	–	19	23	mΩ
		V_{GS} = 4.5 V, I_D = 6 A	–	26	35	
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C	–	28	33	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 7.5 A	–	21	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz	–	881	1235	pF
C_{oss}	Output Capacitance		–	182	255	
C_{rss}	Reverse Transfer Capacitance		–	6.1	15	
R_G	Gate Resistance		0.1	0.5	1.5	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 30 V, I_D = 7.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	7.3	15	ns
t_r	Rise Time		–	1.7	10	
$t_{d(off)}$	Turn–Off Delay Time		–	16	29	
t_f	Fall Time		–	1.4	10	
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_D = 7.5 A	–	12	17	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 30 V, I_D = 7.5 A	–	5.8	8.1	
Q_{gs}	Gate to Source Charge	V_{DD} = 30 V, I_D = 7.5 A	–	2.7	3.8	
Q_{gd}	Gate to Drain “Miller” Charge		–	1.4	2.0	
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.8	1.2	V
		V_{GS} = 0 V, I_S = 7.5 A (Note 2)		0.9	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7.5 A, di/dt = 100 A/μs	–	23	37	ns
Q_{rr}	Reverse Recovery Charge		–	9.7	19	nC

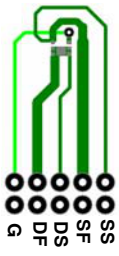
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.



a. 52°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. E_{AS} of 37 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 5 A, V_{DD} = 60 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 16 A.
4. Pulsed Id measured at td ≤ 250 μs, refer to Figure 11 SOA graph for more details.

FDMA86551L

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

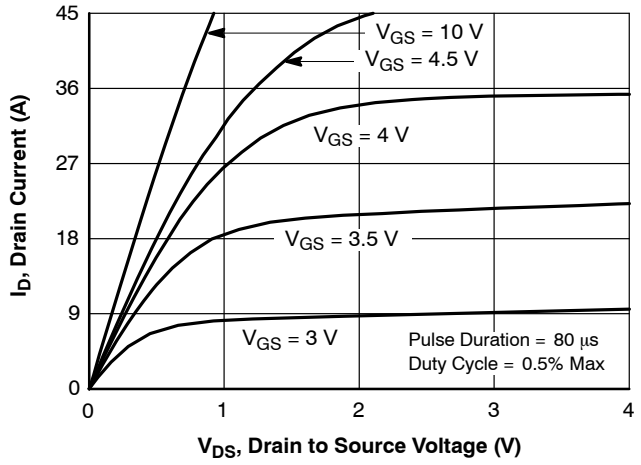


Figure 1. On−Region Characteristics

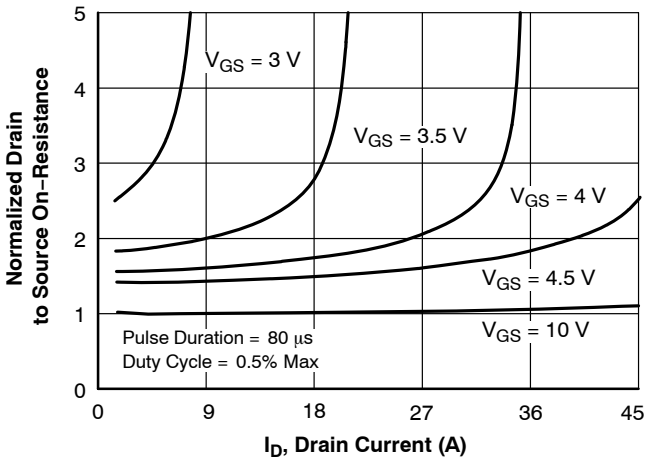


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

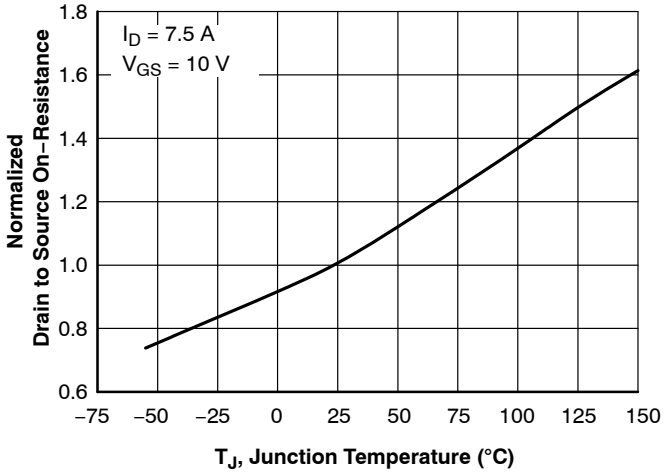


Figure 3. Normalized On−Resistance vs. Junction Temperature

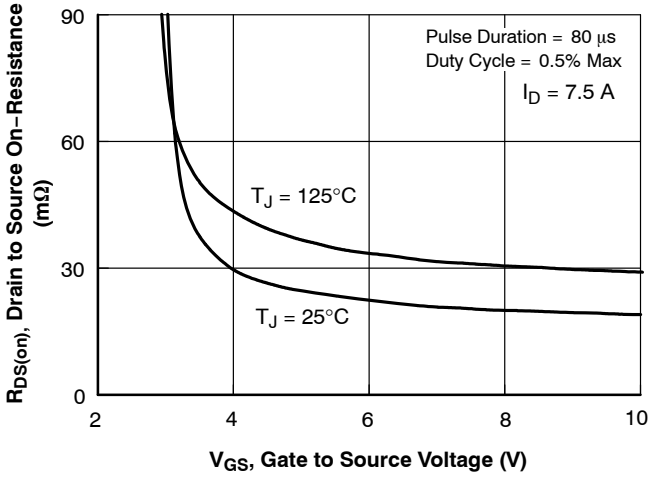


Figure 4. On−Resistance vs. Gate to Source Voltage

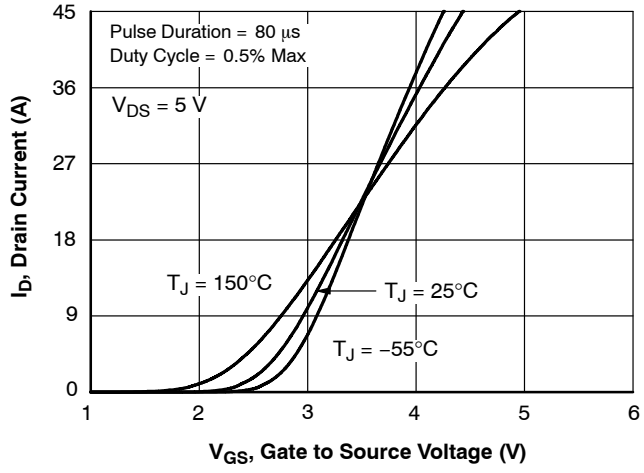


Figure 5. Transfer Characteristics

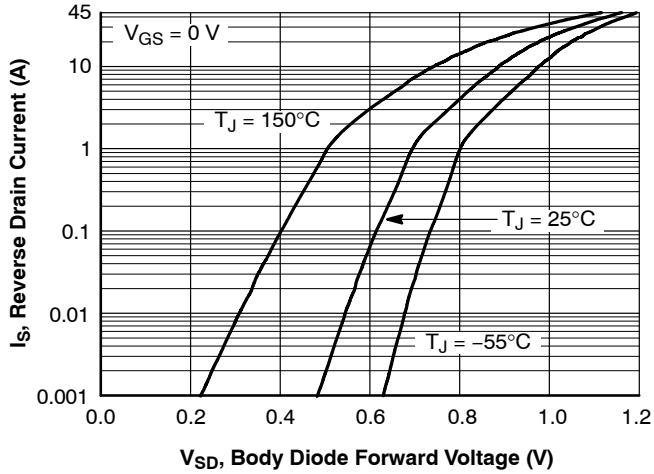


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

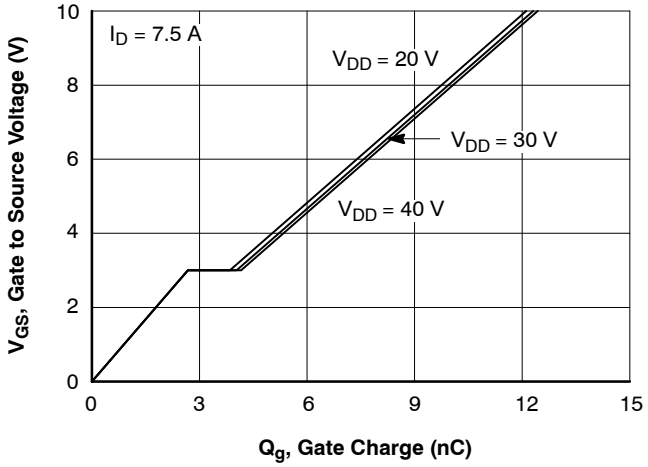


Figure 7. Gate Charge Characteristics

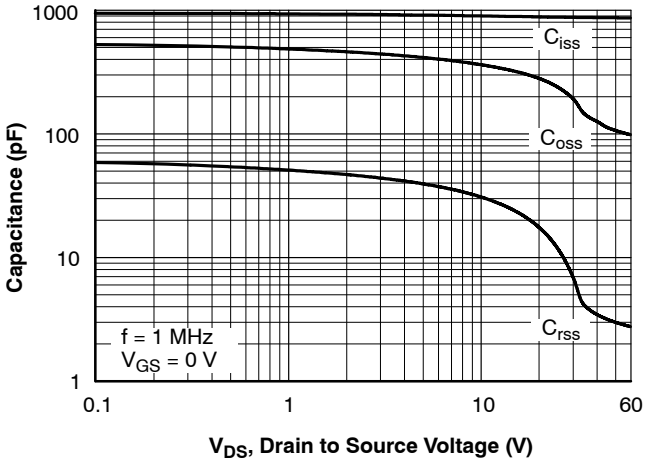


Figure 8. Capacitance vs. Drain to Source Voltage

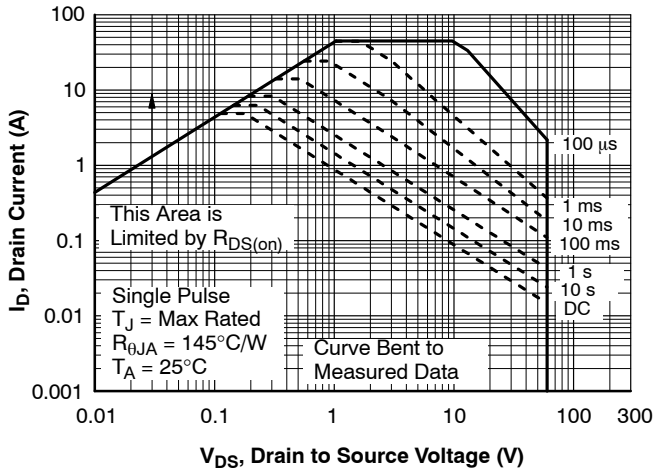


Figure 9. Forward Bias Safe Operating Area

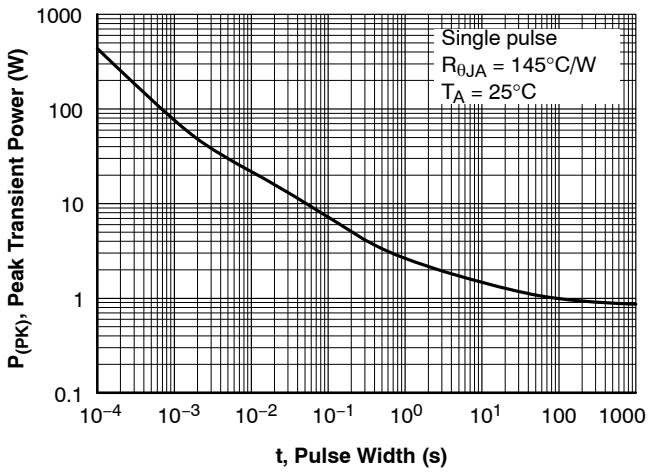


Figure 10. Single Pulse Maximum Power Dissipation

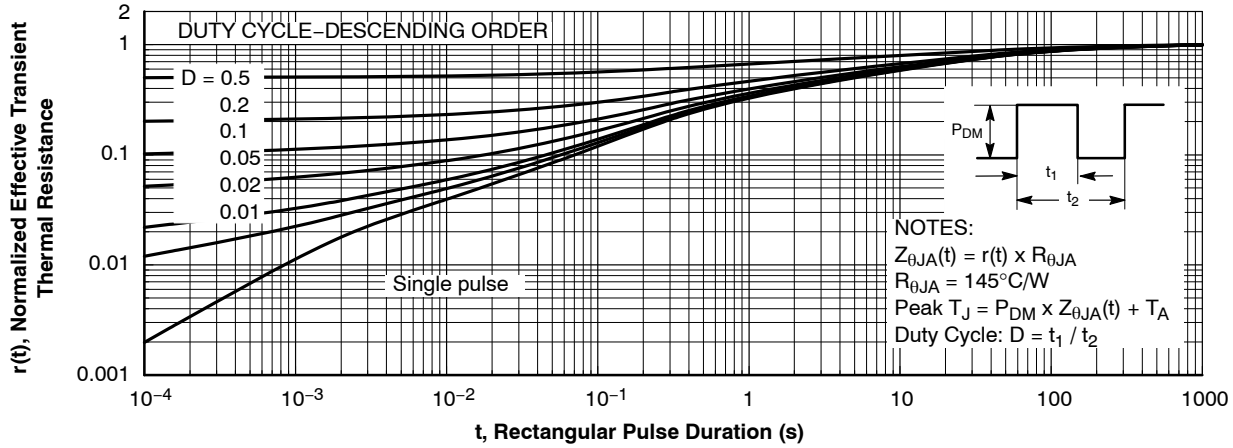


Figure 11. Junction–to–Ambient Transient Thermal Response Curve

FDMA86551L

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMA86551L	551	WDFN6 2x2, 0.65P (Pb−Free/Halide Free)	7”	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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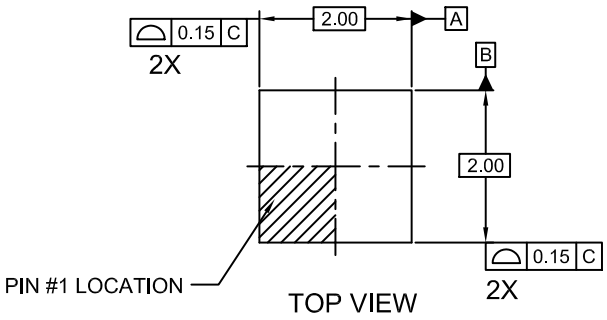
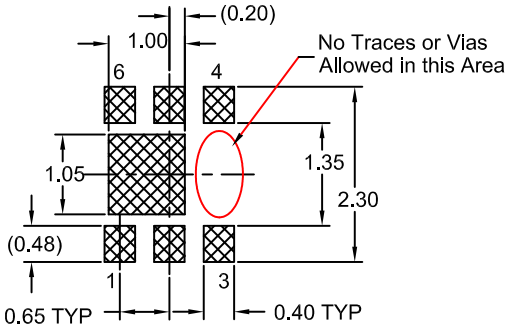
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

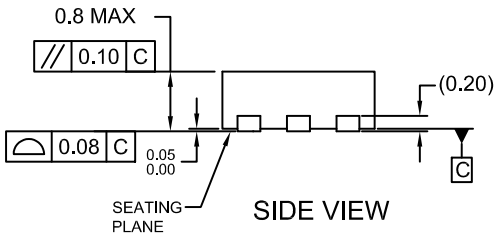
WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

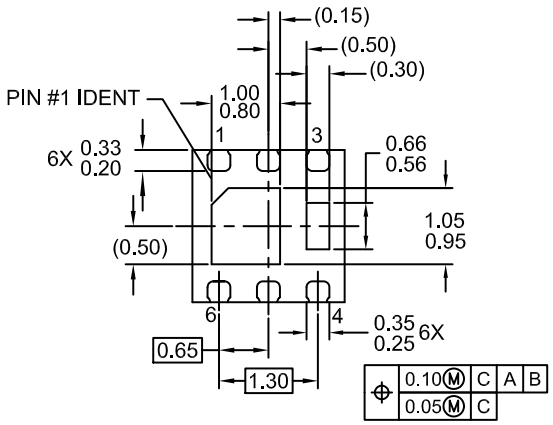
DATE 31 AUG 2016



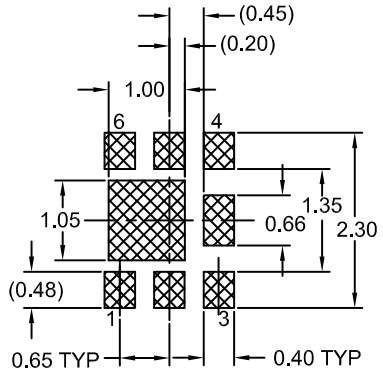


RECOMMENDED LAND PATTERN OPT 1





BOTTOM VIEW



RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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DESCRIPTION:	**WDFN6 2X2, 0.65P**		**PAGE 1 OF 1**

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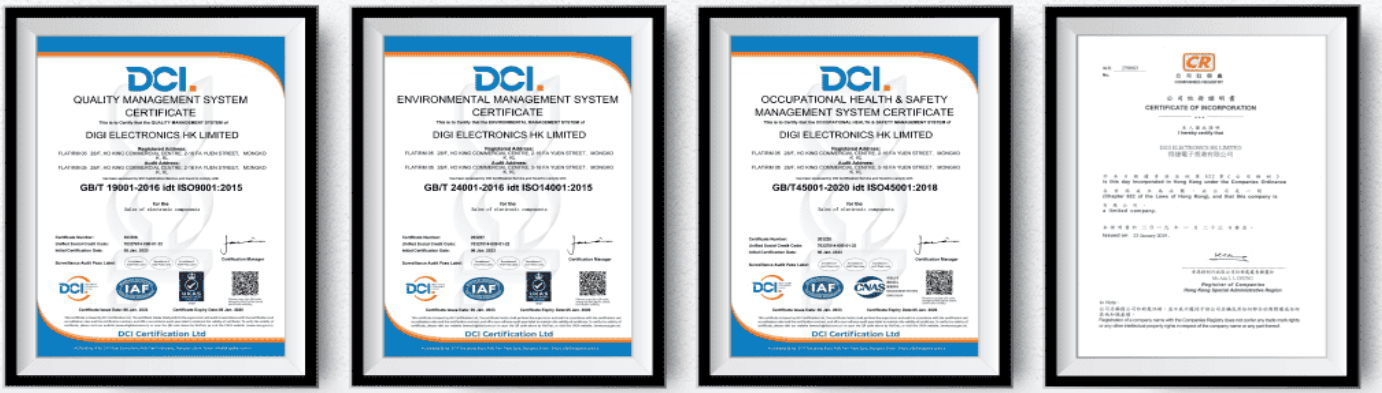

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