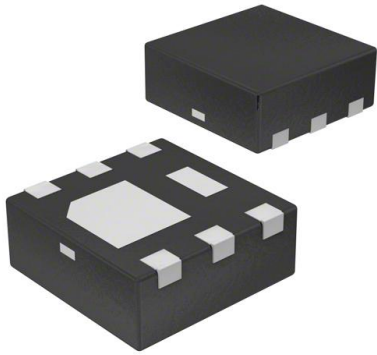


FDMA908PZ Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	FDMA908PZ-DG
Manufacturer	onsemi
Manufacturer Product Number	FDMA908PZ
Description	MOSFET P-CH 12V 12A 6MICROFET
Detailed Description	P-Channel 12 V 12A (Ta) 2.4W (Ta) Surface Mount 6 -MicroFET (2x2)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

FDMA908PZ

Series:

PowerTrench®

FET Type:

P-Channel

Drain to Source Voltage (Vdss):

12 V

Drive Voltage (Max Rds On, Min Rds On):

1.8V, 4.5V

Vgs(th) (Max) @ Id:

1V @ 250µA

Vgs (Max):

±8V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

6-MicroFET (2x2)

Base Product Number:

FDMA908

Manufacturer:

onsemi

Product Status:

Last Time Buy

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

12A (Ta)

Rds On (Max) @ Id, Vgs:

12.5mOhm @ 12A, 4.5V

Gate Charge (Qg) (Max) @ Vgs:

34 nC @ 4.5 V

Input Capacitance (Ciss) (Max) @ Vds:

3957 pF @ 6 V

Power Dissipation (Max):

2.4W (Ta)

Mounting Type:

Surface Mount

Package / Case:

6-WDFN Exposed Pad

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

**MOSFET – Single, P-Channel,
POWERTRENCH®****-12 V, -12 A, 12.5 mΩ****FDMA908PZ****General Description**

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $R_{DS(on)}$ = 12.5 mΩ at $V_{GS} = -4.5$ V, $I_D = -12$ A
- Max $R_{DS(on)}$ = 18 mΩ at $V_{GS} = -2.5$ V, $I_D = -10$ A
- Max $R_{DS(on)}$ = 28 mΩ at $V_{GS} = -1.8$ V, $I_D = -8$ A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2.8 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

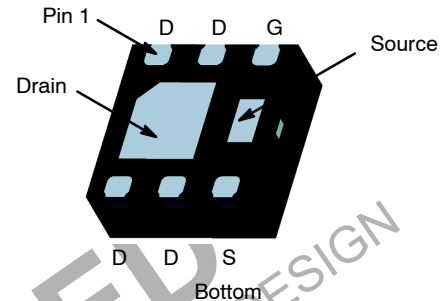
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-12	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	$T_A = 25^\circ\text{C}$ -12 -40	A
P_D	Power Dissipation – (Note 1a) – (Note 1b)	$T_A = 25^\circ\text{C}$ 2.4 $T_A = 25^\circ\text{C}$ 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

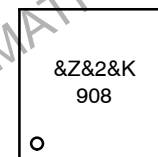
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

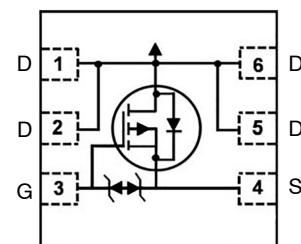
V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
-12 V	12.5 mΩ @ -4.5 V	-12 A
	18 mΩ @ -2.5 V	
	28 mΩ @ -1.8 V	



DFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 506DT

MARKING DIAGRAM

&Z = Assembly Plant Code
&2 = 2-Digit Date Code
&K = 2-Digits Lot Run Traceability Code
908 = Specific Device Code

PIN ASSIGNMENT**ORDERING INFORMATION**

Device	Package	Shipping†
FDMA908PZ	DFN6 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDMA908PZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	-12	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	-10	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -9.6 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	2.8	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}$, $I_D = -12 \text{ A}$	-	10	12.5	$\text{m}\Omega$
		$V_{GS} = -2.5 \text{ V}$, $I_D = -10 \text{ A}$	-	13	18	
		$V_{GS} = -1.8 \text{ V}$, $I_D = -8 \text{ A}$	-	18	28	
		$V_{GS} = -4.5 \text{ V}$, $I_D = -12 \text{ A}$, $T_J = 125^\circ\text{C}$	-	13	16	
g_{FS}	Forward Transconductance	$V_{DD} = -5 \text{ V}$, $I_D = -12 \text{ A}$	-	63	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -6 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	2638	3957	pF
C_{oss}	Output Capacitance		-	649	974	pF
C_{rss}	Reverse Transfer Capacitance		-	602	903	pF

SWITCHING CHARACTERISTICS

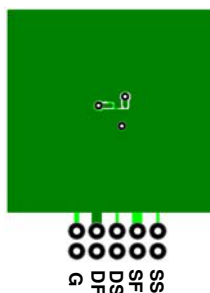
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -6 \text{ V}$, $I_D = -12 \text{ A}$, $V_{GS} = -4.5 \text{ V}$, $R_{GEN} = 6 \Omega$	-	11	21	ns
t_r	Rise Time		-	12	23	ns
$t_{d(off)}$	Turn-Off Delay Time		-	131	223	ns
t_f	Fall Time		-	71	121	ns
Q_g	Total Gate Charge		$V_{DD} = -6 \text{ V}$, $I_D = -12 \text{ A}$, $V_{GS} = -4.5 \text{ V}$	-	24	34
Q_{gs}	Gate to Source Charge		-	3.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	5.3	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

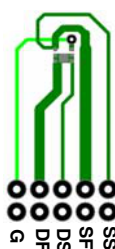
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = -2 \text{ A}$ (Note 2)	-	-0.6	-1.2	V
		$V_{GS} = 0 \text{ V}$, $I_S = -12 \text{ A}$ (Note 2)	-	-0.8	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -12 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	26	42	ns
Q_{rr}	Reverse Recovery Charge		-	8.5	17	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5 \text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $52^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $145^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty cycle $< 2.0\%$.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

FDMA908PZ

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

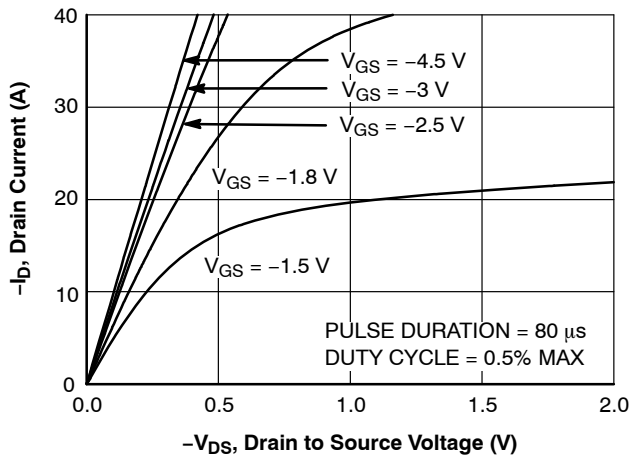


Figure 1. On-Region Characteristics

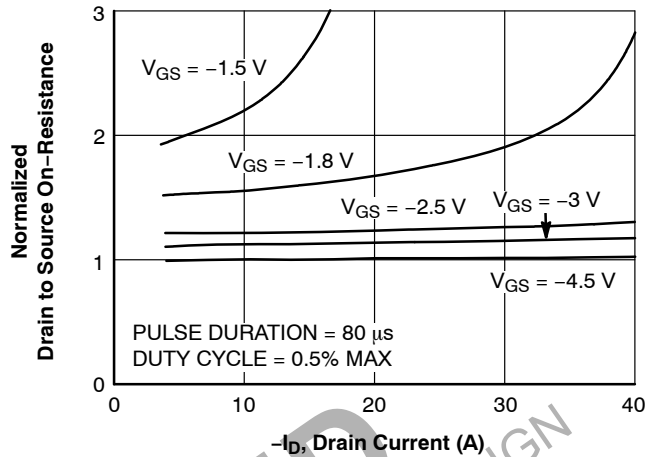


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

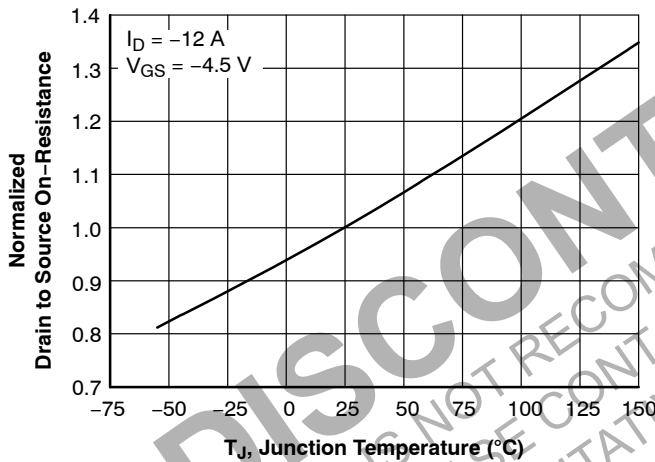


Figure 3. Normalized On-Resistance vs. Junction Temperature

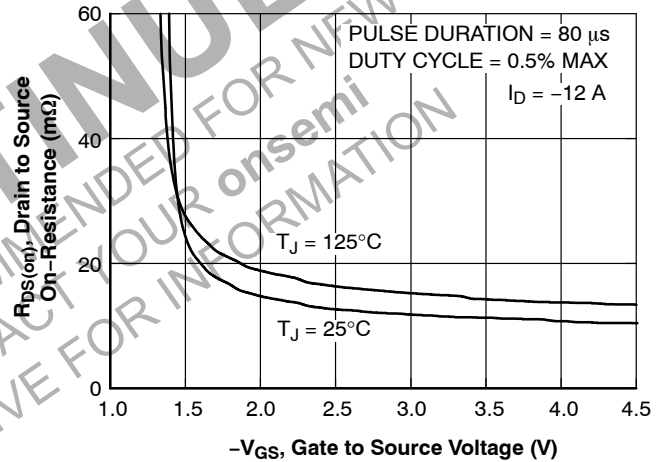


Figure 4. On-Resistance vs. Gate to Source Voltage

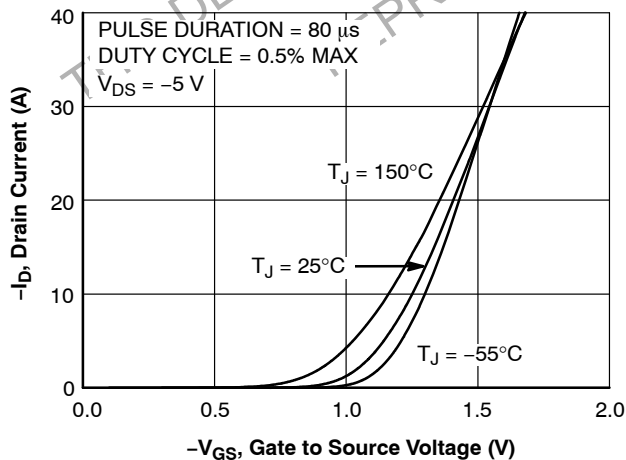


Figure 5. Transfer Characteristics

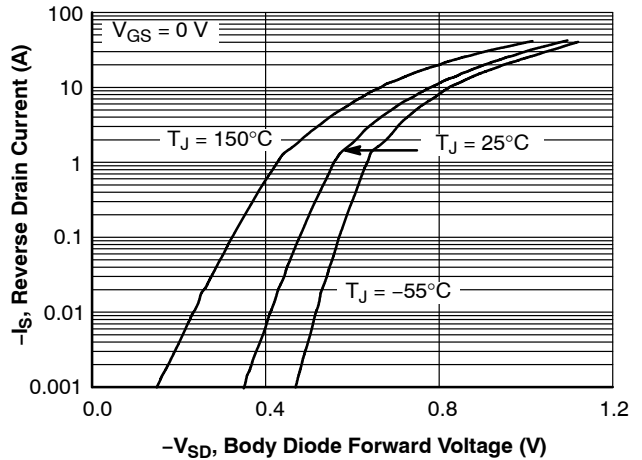


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDMA908PZ

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

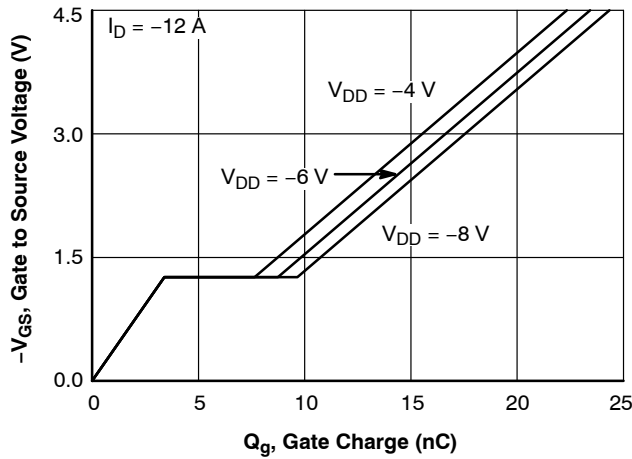


Figure 7. Gate Charge Characteristics

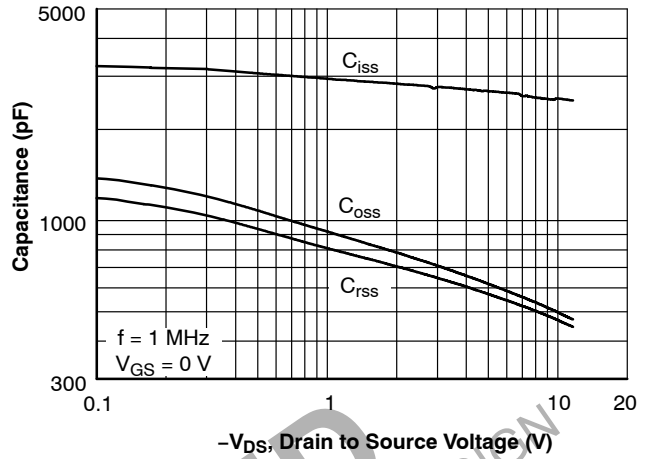


Figure 8. Capacitance vs. Drain to Source Voltage

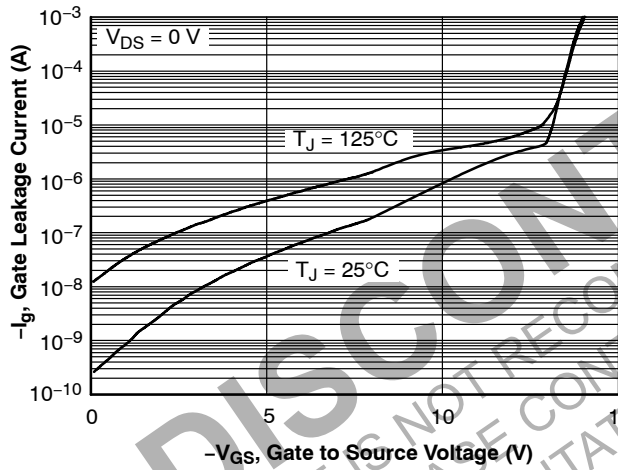


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

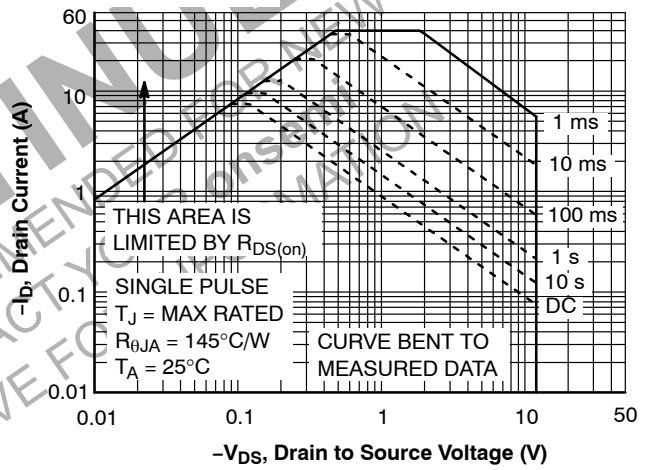


Figure 10. Forward Bias Safe Operating Area

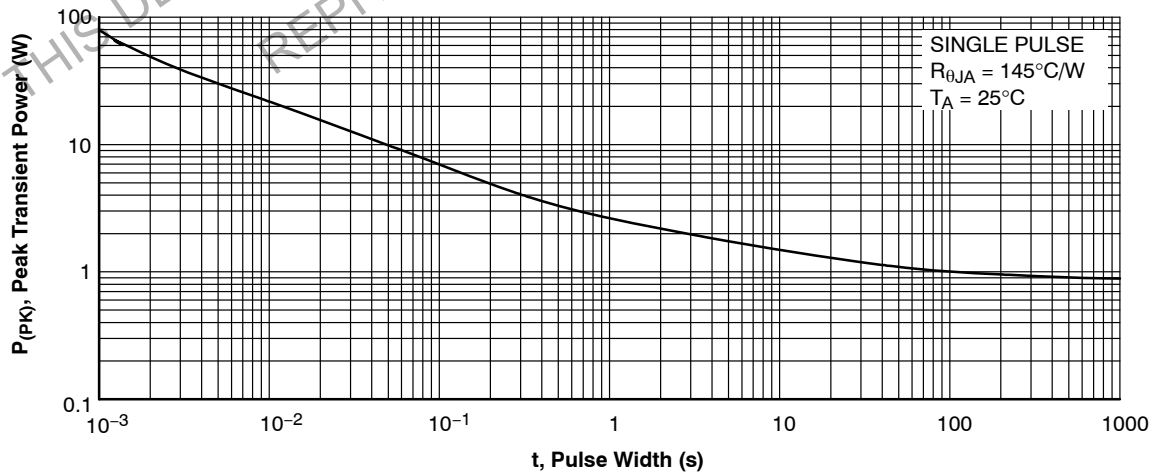


Figure 11. Single Pulse Maximum Power Dissipation

FDMA908PZ

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

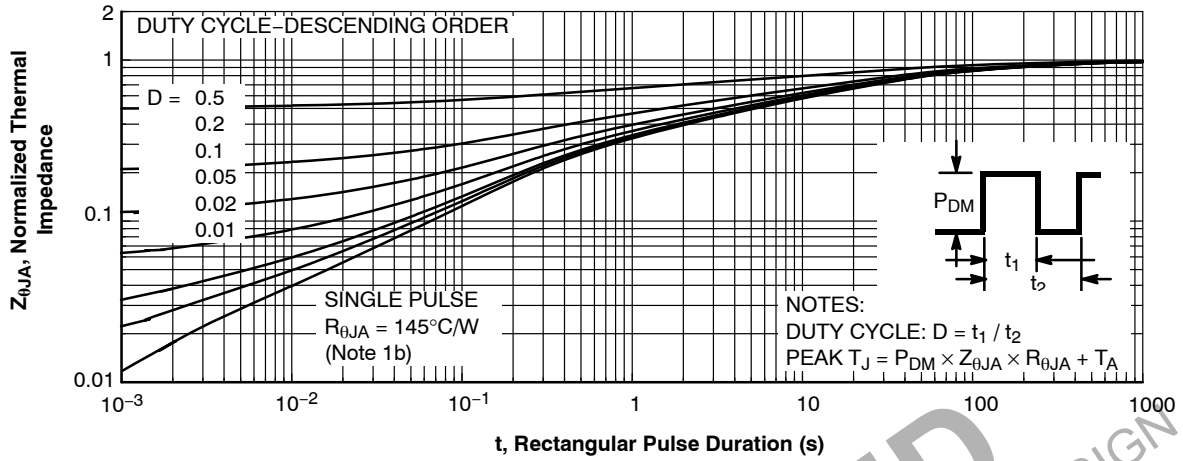


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

DISCONTINUED

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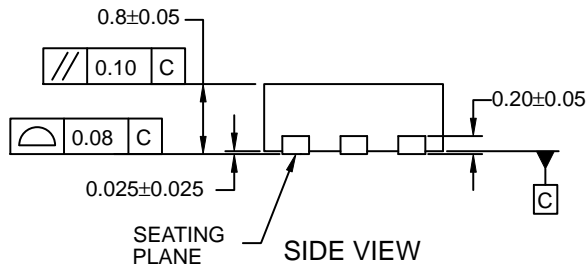
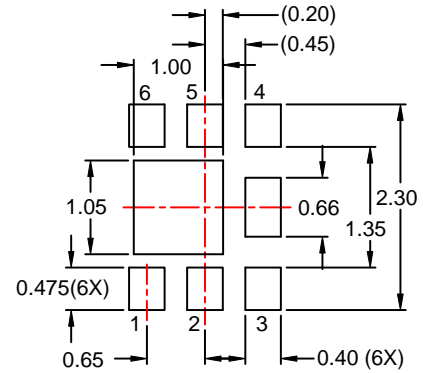
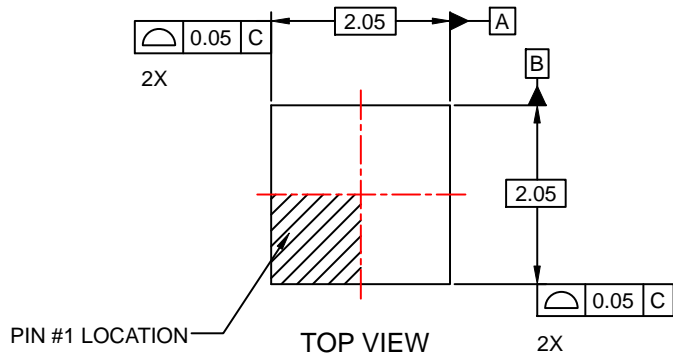
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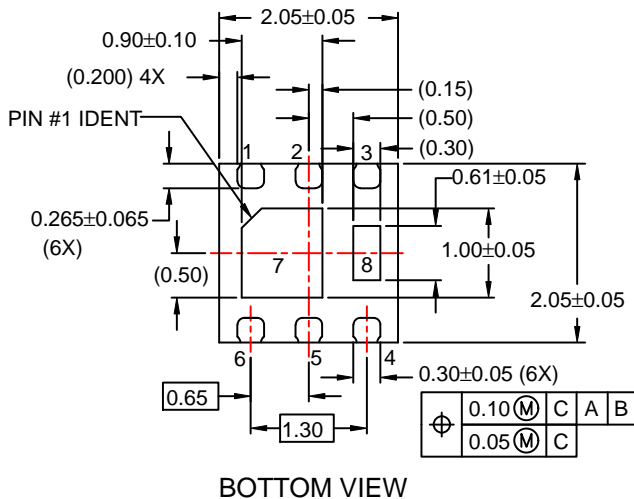
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**

DFN6 2x2, 0.65P
CASE 506DT
ISSUE O

DATE 31 JUL 2016



Pin #	Function
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain
7	Drain
8	Source



NOTES:

- A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	DFN6 2X2, 0.65P	PAGE 1 OF 1

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