

FDMC6688P Datasheet



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DiGi Electronics Part Number FDMC6688P-DG

Manufacturer onsemi

Manufacturer Product Number FDMC6688P

Description MOSFET P-CH 20V 14A/56A 8PQFN

Detailed Description P-Channel 20 V 14A (Ta), 56A (Tc) 2.3W (Ta), 30W (T

c) Surface Mount 8-PQFN (3.3x3.3), Power33



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RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDMC6688P	onsemi
Series:	Product Status:
PowerTrench®	Obsolete
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
20 V	14A (Ta), 56A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
1.8V, 4.5V	6.5mOhm @ 14A, 4.5V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
1V @ 250μA	61 nC @ 4.5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±8V	7435 pF @ 10 V
FET Feature:	Power Dissipation (Max):
	2.3W (Ta), 30W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (3.3x3.3), Power33	8-PowerWDFN
Base Product Number:	
FDMC6688	

Environmental & Export classification

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

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MOSFET – P-Channel, POWERTRENCH®

-20 V, -56 A, 6.5 m Ω

FDMC6688P

General Description

This P-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for $R_{DS(on)}$, switching performance and ruggedness.

Features

- Max $R_{DS(on)} = 6.5 \text{ m}\Omega$ at $V_{GS} = -4.5 \text{ V}$, $I_D = -14 \text{ A}$
- Max $R_{DS(on)} = 9.8 \text{ m}\Omega$ at $V_{GS} = -2.5 \text{ V}$, $I_D = -11 \text{ A}$
- Max $R_{DS(on)} = 20 \text{ m}\Omega$ at $V_{GS} = -1.8 \text{ V}$, $I_D = -9 \text{ A}$
- High Performance Trench Technology for Extremely Low R_{DS(on)}
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- · Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I _D	Drain Current -Continuous, T _C = 25°C -Continuous, T _A = 25°C (Note 1a) -Pulsed (Note 3)	-56 -14 -226	Α
P _D	Power Dissipation $T_C = 25^{\circ}C$ $T_A = 25^{\circ}C$ (Note 1a)	30 2.3	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

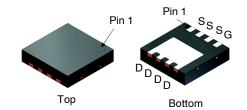
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.8	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

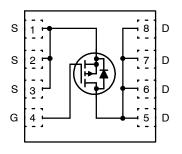
1

V _{DS}	R _{DS(on)} MAX	I _D MAX
-20 V	6.5 mΩ @ -4.5 V	–56 A
	9.8 mΩ @ -2.5 V	
	20 mΩ @ –1.8 V	



PQFN8 3.3X3.3, 0.65P (Power 33) CASE 483AX

PIN ASSIGNMENT



MARKING DIAGRAM



Z = Assembly Plant Code
YWW = Date Code (Year & Week)
KK = Lot Traceability Code
FDMC6688P = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC6688P	PQFN8 (Power 33) (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

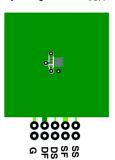
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	TERISTICS	•	-	•	-	•
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20	_	_	V
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25°C	-	-16	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
ON CHARACTE	ERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.75	-1	V
$\Delta V_{GS(th)} / \Delta T_{J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	3	-	mV/°C
R _{DS(on)}	Static Drain to Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -14 \text{ A}$	-	5.3	6.5	mΩ
		V _{GS} = -2.5 V, I _D = -11 A		7	9.8	
		$V_{GS} = -1.8 \text{ V}, I_D = -9 \text{ A}$	-	10.7	20	
		$V_{GS} = -4.5 \text{ V}, I_D = -14 \text{ A},$ $T_J = 125^{\circ}\text{C}$	-	7.3	11	
9FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_D = -14 \text{ A}$	_	80	_	S
DYNAMIC CHA	RACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$	_	4956	7435	pF
C _{oss}	Output Capacitance	f = 1 MHz	_	678	1020	pF
C_{rss}	Reverse Transfer Capacitance	1	_	618	930	pF
R_{g}	Gate Resistance		-	4.5	-	Ω
SWITCHING CH	HARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_{D} = -14 \text{ A},$	_	19	35	ns
t _r	Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$	_	33	53	ns
t _{d(off)}	Turn-Off Delay Time		_	119	190	ns
t _f	Fall Time		-	68	109	ns
Q_g	Total Gate Charge	$V_{DD} = -10 \text{ V}, I_D = -14 \text{ A},$ $V_{GS} = -4.5 \text{ V}$	_	44	61	nC
Q_{gs}	Gate to Source Charge	$V_{GS} = -4.5 \text{ V}$	_	7.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	11	-	nC
DRAIN-SOUR	CE DIODE CHARACTERISTICS					
V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -14 A (Note 2)	_	-0.8	-1.2	V
		V _{GS} = 0 V, I _S = -2 A (Note 2)	_	-0.6	-1.2	
t _{rr}	Reverse Recovery Time	I _F = -14 A, di/dt = 100 A/μs	_	26	41	ns
Q_{rr}	Reverse Recovery Charge		_	10	20	nC

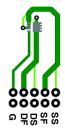
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



 a. 53°C/W when mounted on a 1 in² pad of 2 oz copper.



 b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0 %.
- 3. Pulse Id refers to Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS

(T_J = 25°C Unless Otherwise Noted)

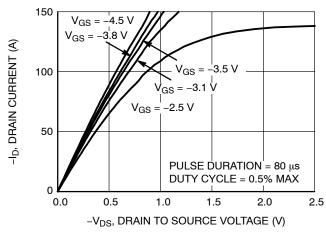


Figure 1. On-Region Characteristics

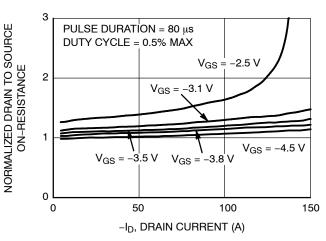


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

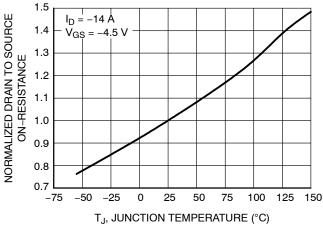


Figure 3. Normalized On-Resistance vs.

Junction Temperature

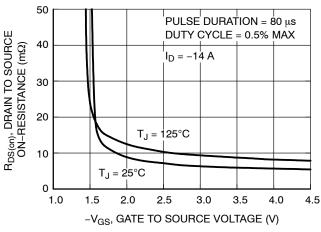


Figure 4. On-Resistance vs. Gate to Source Voltage

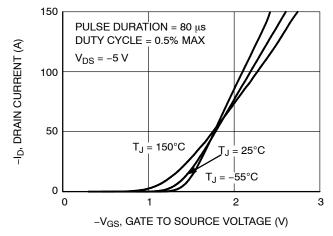


Figure 5. Transfer Characteristics

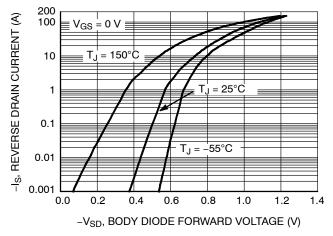


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T_J = 25°C Unless Otherwise Noted)

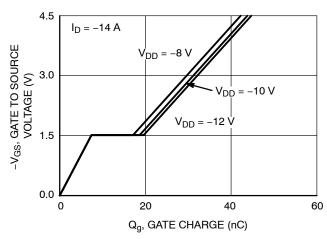


Figure 7. Gate Charge Characteristics

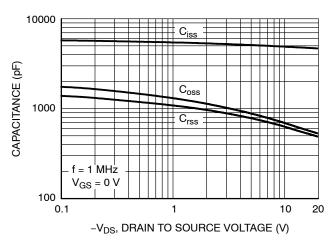


Figure 8. Capacitance vs. Drain to Source Voltage

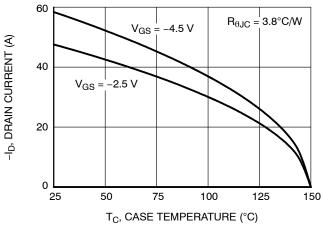


Figure 9. Maximum Continuous Drain Current vs. Case Temperature

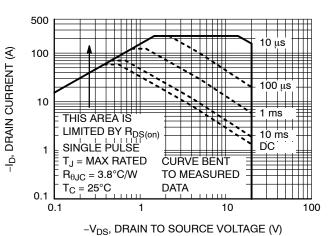


Figure 10. Forward Bias Safe Operating Area

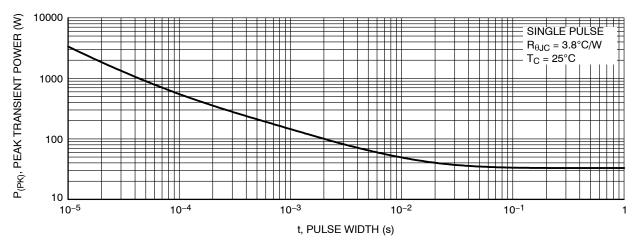


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T_J = 25°C Unless Otherwise Noted)

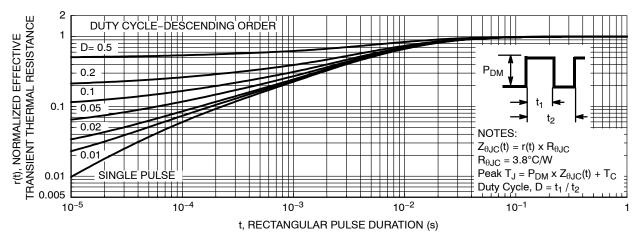


Figure 12. Junction-to-Case Transient Thermal Response Curve



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



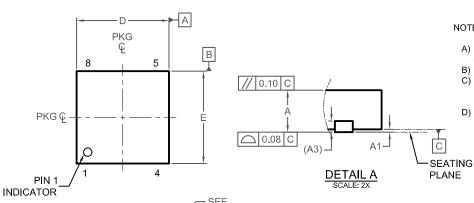
PQFN8 3.3X3.3, 0.65P CASE 483AX **ISSUE B**

DATE 24 JUN 2022

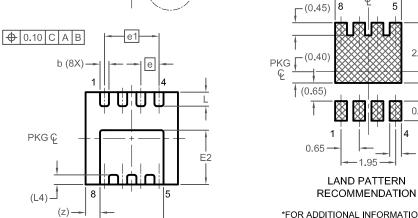
NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

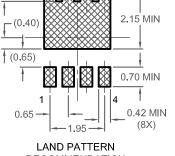
DIM	MILLIMETERS		
Diivi	MIN.	NOM.	MAX.
Α	0.70	0.75	0.80
A1	0.00	ı	0.05
A3	().20 REF	
b	0.27	0.32	0.37
D	3,20	3,30	3.40
D2	2.17	2.27	2,37
Е	3.20	3.30	3.40
E2	1.84	1.94	2.04
е	0.65 BSC		
e1	1.95 BSC		
L	0.40	0.50	0.60
L4	0.34 REF		
z	0.52 REF		



DETAIL A



D2



-2.37 MIN →

SYM

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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