FDMC8462 Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	FDMC8462-DG
Manufacturer	onsemi
Manufacturer Product Number	FDMC8462
Description	MOSFET N-CH 40V 14A/20A POWER33
Detailed Description	N-Channel 40 V 14A (Ta), 20A (Tc) 2W (Ta), 41W (Tc) Surface Mount Power33

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDMC8462	onsemi
Series:	Product Status:
PowerTrench®	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
40 V	14A (Ta), 20A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	5.8mOhm @ 13.5A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
3V @ 250µA	43 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	2660 pF @ 20 V
FET Feature:	Power Dissipation (Max):
-	2W (Ta), 41W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
Power33	8-PowerTDFN
Base Product Number:	
FDMC84	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

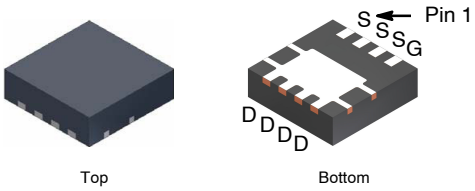
DATA SHEET
www.onsemi.com

MOSFET – N-Channel, POWERTRENCH®

40 V, 20 A, 5.8 mΩ

FDMC8462

V_{DS}	$r_{DS(ON)}$ MAX	I_D MAX
40 V	5.8 mΩ @ 10 V	20 A
	8.0 mΩ @ 4.5 V	



PQFN8 3.3 × 3.3, 0.65P
(Power 33)
CASE 483AK

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

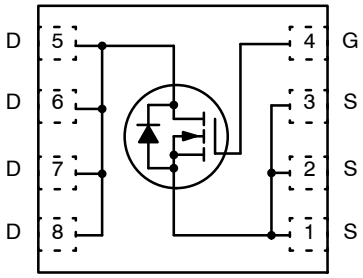
Features

- Max $r_{DS(on)}$ = 5.8 mΩ at V_{GS} = 10 V, I_D = 13.5 A
  Max $r_{DS(on)}$ = 8.0 mΩ at V_{GS} = 4.5 V, I_D = 11.8 A
- Low Profile – 1 mm Max in Power 33
- 100% UIL Tested
- Pb−Free, Halide Free and RoHS Compliant

Applications

- DC – DC Conversion

ELECTRICAL CONNECTION



N−Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

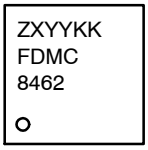
Symbol	Parameter		Value	Unit
V_{DS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current – Continuous (Package Limited) – Continuous (Silicon Limited) – Continuous (Note 1a) – Pulsed	 T_C = 25°C T_C = 25°C T_A = 25°C 	 20 64 14 50	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)		216	mJ
P_D	Power Dissipation Power Dissipation (Note 1a)	T_C = 25°C T_A = 25°C	41 2.0	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

MARKING DIAGRAM



Z = Assembly Plant Code
XYY = 3−Digit Date Code (Year and Week)
KK = 2−Digits Lot Run Traceability Code
FDMC8462 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDMC8462

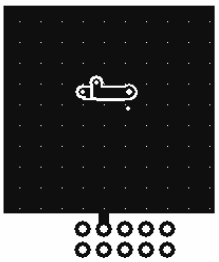
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	31	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 32 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	–6.6	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On–Resistance	V_{GS} = 10 V, I_D = 13.5 A V_{GS} = 4.5 V, I_D = 11.8 A V_{GS} = 10 V, I_D = 13.5 A, T_J = 125°C	– – –	4.7 6.4 7.1	5.8 8.0 9.3	mΩ
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 13.5 A	–	60	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	–	2000	2660	pF
C_{oss}	Output Capacitance		–	545	725	pF
C_{rss}	Reverse Transfer Capacitance		–	80	120	pF
R_g	Gate Resistance	f = 1 MHz	–	2.7	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 20 V, I_D = 13.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	12	21	ns
t_r	Rise Time		–	4	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	27	43	ns
t_f	Fall Time		–	3	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 20 V, I_D = 13.5 A	–	30	43	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 20 V, I_D = 13.5 A	–	15	21	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 13.5 A	–	6	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	5	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13.5 A (Note 2)	–	0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.7 A (Note 2)	–	0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 13.5 A, di/dt = 100 A/μs	–	35	57	ns
Q_{rr}	Reverse Recovery Charge		–	20	32	nC

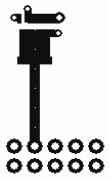
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR–4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
3. Starting T_J = 25°C; N–ch: L = 3 mH, I_{AS} = 12 A, V_{DD} = 40 V, V_{GS} = 10 V.

FDMC8462

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

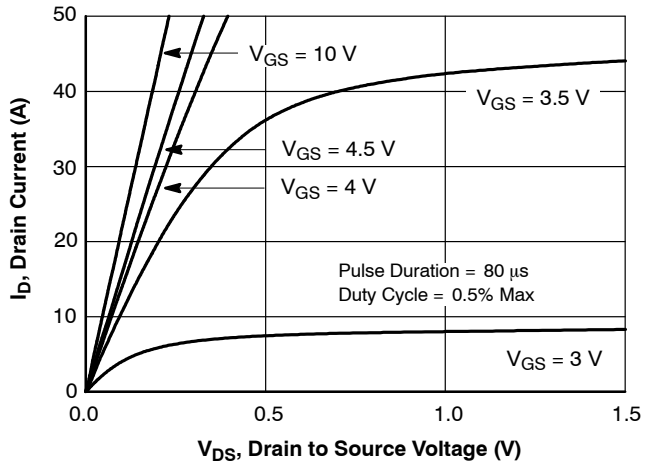


Figure 1. On−Region Characteristics

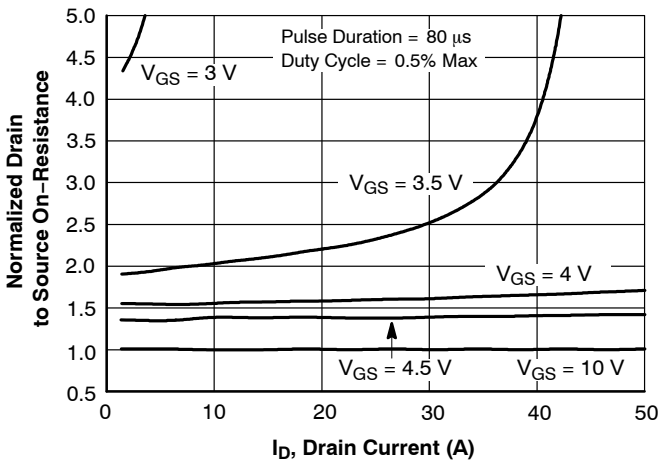


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

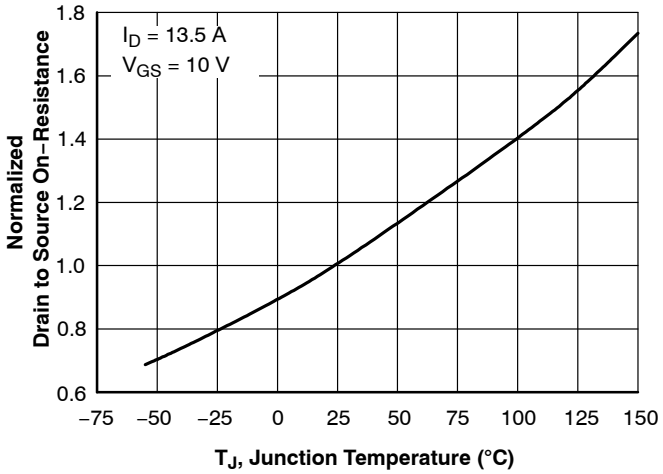


Figure 3. Normalized On−Resistance vs. Junction Temperature

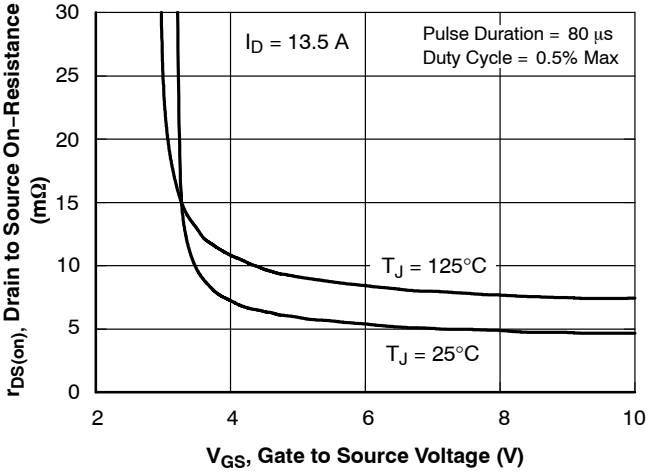


Figure 4. On−Resistance vs. Gate to Source Voltage

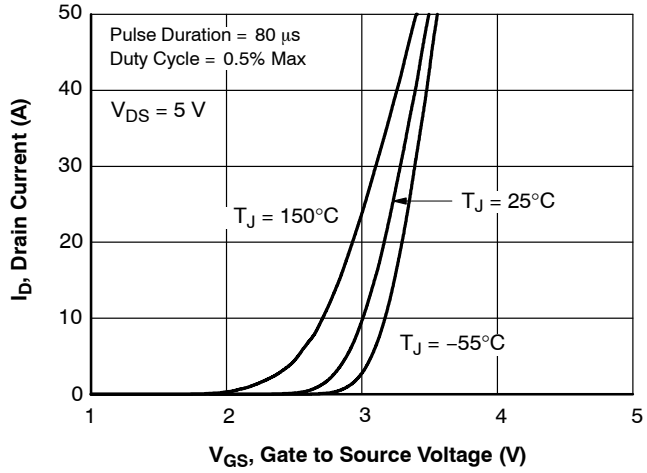


Figure 5. Transfer Characteristics

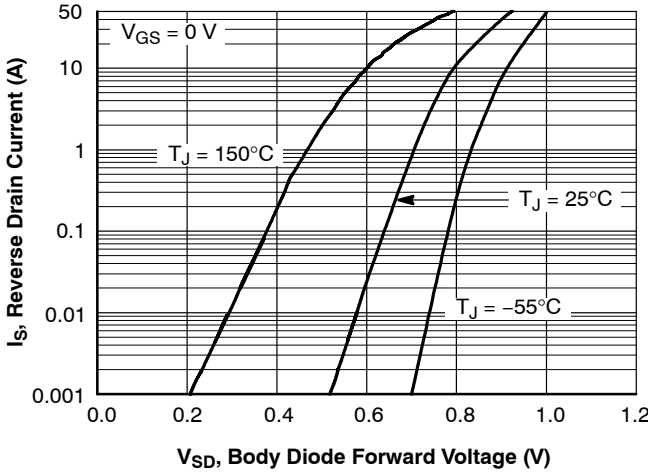


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDMC8462

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

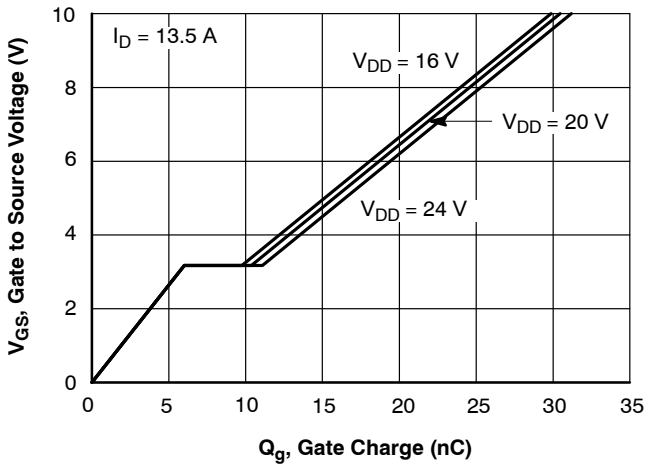


Figure 7. Gate Charge Characteristics

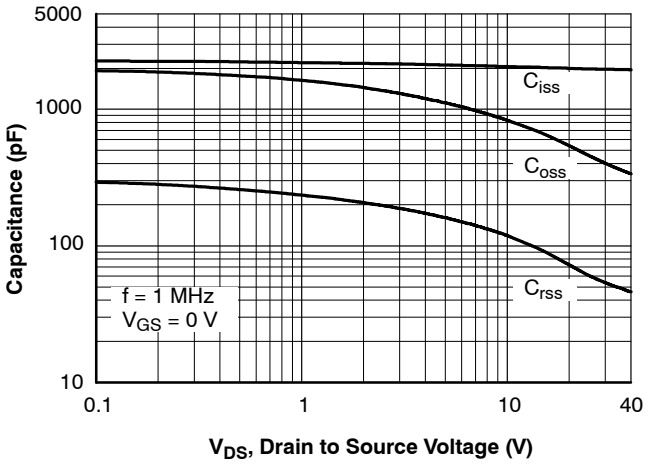


Figure 8. Capacitance vs. Drain to Source Voltage

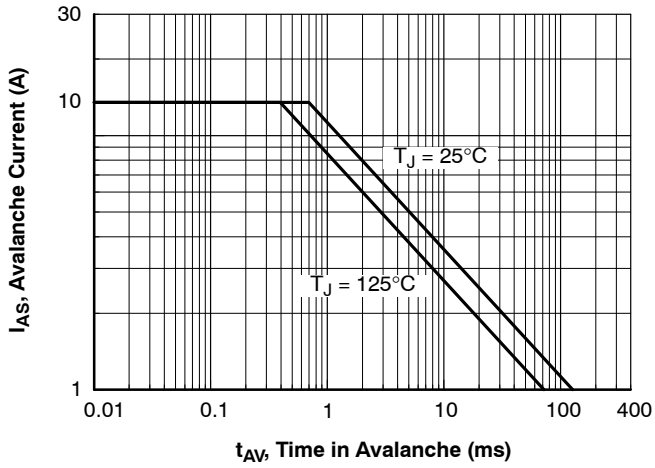


Figure 9. Unclamped Inductive Switching Capability

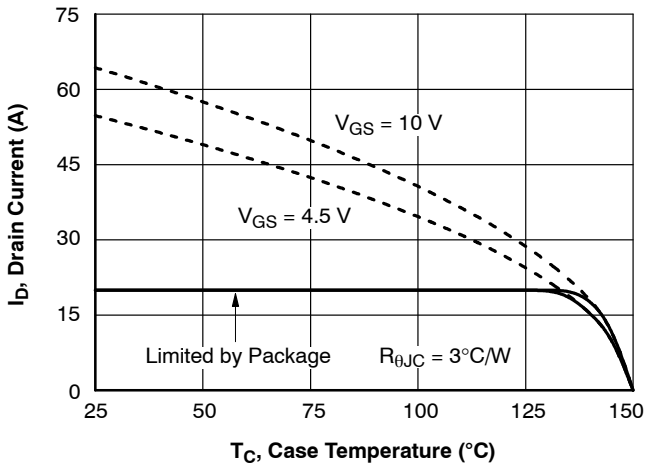


Figure 10. Maximum Continuous Drain Current vs Case Temperature

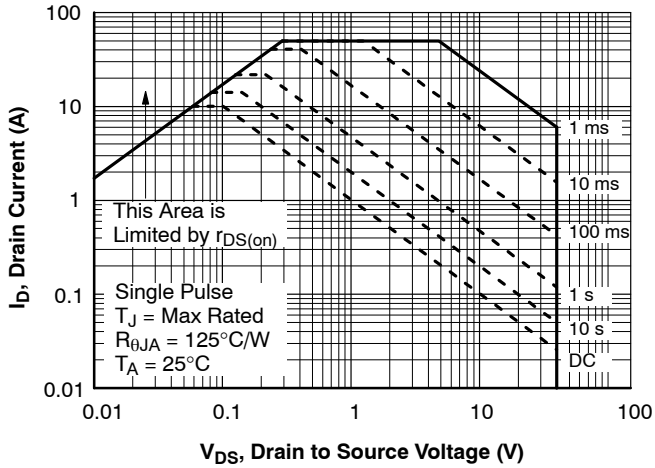


Figure 11. Forward Bias Safe Operating Area

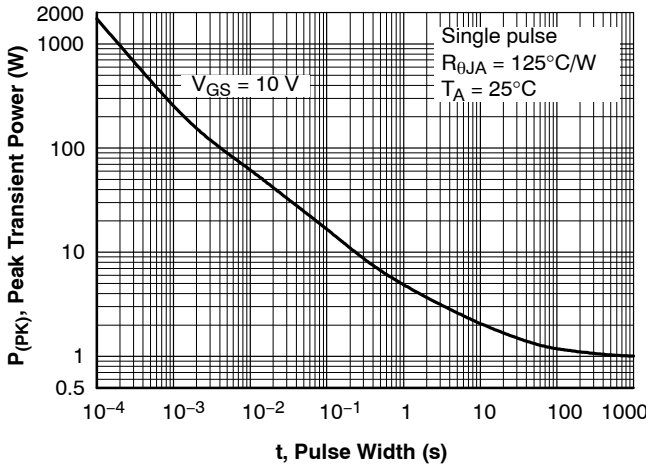


Figure 12. Single Pulse Maximum Power Dissipation

FDMC8462

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

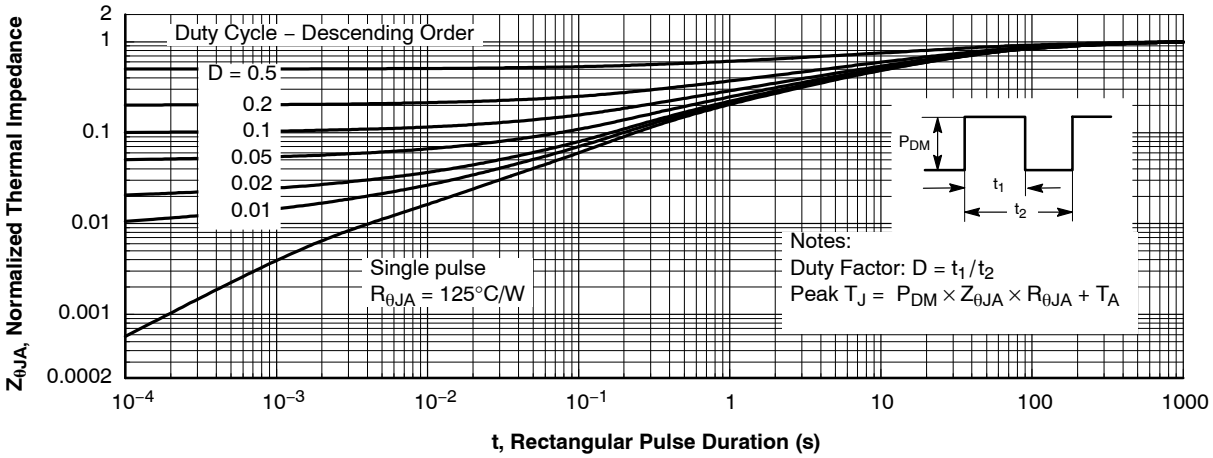


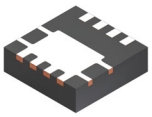
Figure 13. Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMC8462	FDMC8462	PQFN8 3.3 x 3.3, 0.65P (Power 33) (Pb–Free/Halide Free)	13”	12 mm	3000 / Tape & Reel

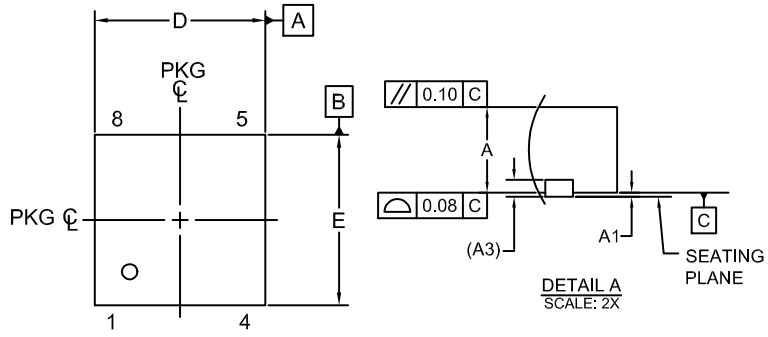
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

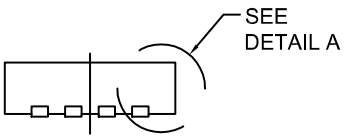


PQFN8 3.3X3.3, 0.65P
CASE 483AK
ISSUE B

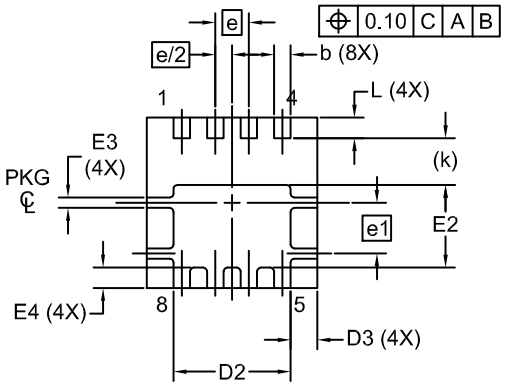
DATE 12 OCT 2021



TOP VIEW



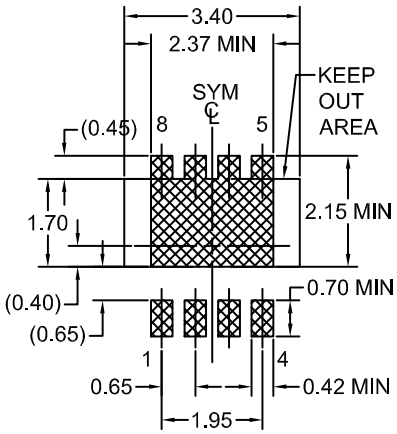
FRONT VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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DESCRIPTION:	**PQFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

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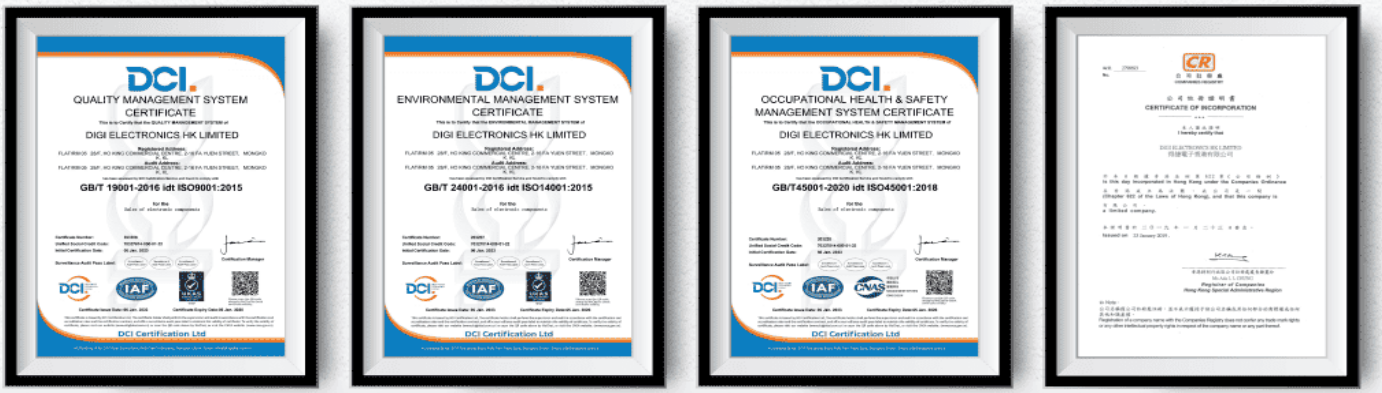

Tel: +00 852-30501935

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