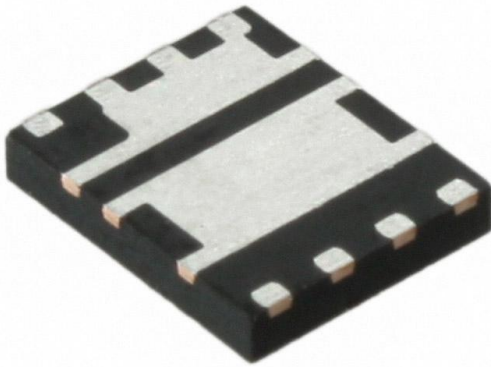


FDMS3610S Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | FDMS3610S-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | FDMS3610S |
| Description | MOSFET 2N-CH 25V 17.5/30A PWR56 |
| Detailed Description | Mosfet Array 25V 17.5A, 30A 1W Surface Mount Power56 |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

FDMS3610S

Series:

PowerTrench®

Technology:

MOSFET (Metal Oxide)

FET Feature:

Logic Level Gate

Current - Continuous Drain (Id) @ 25°C:

17.5A, 30A

Vgs(th) (Max) @ Id:

2V @ 250µA

Input Capacitance (Ciss) (Max) @ Vds:

1570pF @ 13V

Operating Temperature:

-55°C ~ 150°C (Tj)

Package / Case:

8-PowerTDFN

Base Product Number:

FDMS3610

Manufacturer:

onsemi

Product Status:

Obsolete

Configuration:

2 N-Channel (Dual) Asymmetrical

Drain to Source Voltage (Vdss):

25V

Rds On (Max) @ Id, Vgs:

5mOhm @ 17.5A, 10V

Gate Charge (Qg) (Max) @ Vgs:

26nC @ 10V

Power - Max:

1W

Mounting Type:

Surface Mount

Supplier Device Package:

Power56

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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December 2011

FDMS3610S

PowerTrench® Power Stage

25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.0 m Ω at V_{GS} = 10 V, I_D = 17.5 A
- Max $r_{DS(on)}$ = 5.7 m Ω at V_{GS} = 4.5 V, I_D = 16 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.8 m Ω at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 2.2 m Ω at V_{GS} = 4.5 V, I_D = 27 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

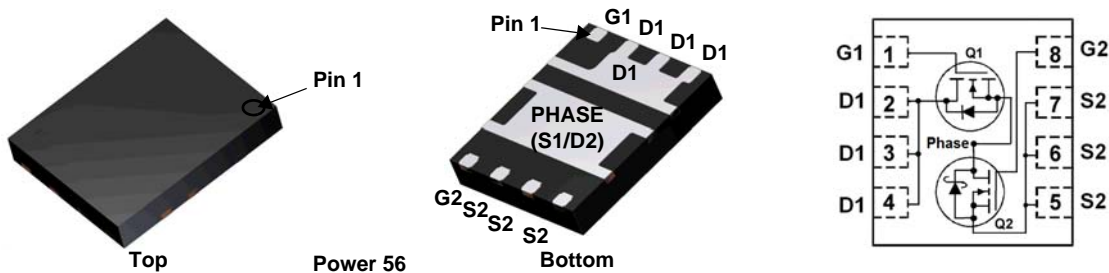


General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCore



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Q1 | Q2 | Units | |
|----------------|--|--------------------------|--------------------|-------------------|------------------|
| V_{DS} | Drain to Source Voltage | 25 | 25 | V | |
| V_{GS} | Gate to Source Voltage | (Note 4) | ± 12 | V | |
| I_D | Drain Current -Continuous (Package limited) | $T_C = 25^\circ\text{C}$ | 30 | A | |
| | -Continuous | $T_A = 25^\circ\text{C}$ | 17.5 ^{1a} | | |
| | -Pulsed | | 70 | | |
| E_{AS} | Single Pulse Avalanche Energy | (Note 3) | 29 | 86 | mJ |
| P_D | Power Dissipation for Single Operation | $T_A = 25^\circ\text{C}$ | 2.2 ^{1a} | 2.5 ^{1b} | W |
| | Power Dissipation for Single Operation | $T_A = 25^\circ\text{C}$ | 1.0 ^{1c} | 1.0 ^{1d} | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | | -55 to +150 | | $^\circ\text{C}$ |

Thermal Characteristics

| | | | | |
|-----------------|---|-------------------|-------------------|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 57 ^{1a} | 50 ^{1b} | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 125 ^{1c} | 120 ^{1d} | |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 3.0 | 2.2 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|-----------|----------|-----------|------------|------------|
| 08OD 07OD | FDMS3610S | Power 56 | 13 " | 12 mm | 3000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | | |
|--------------------------------------|---|--|----------|----------|----------|------------------------|--------------------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | Q1 Q2 | 25 25 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$ | Q1 Q2 | | 12 24 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$ | Q1 Q2 | | | 1 500 | μA μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = 12\text{ V}/-8\text{ V}$, $V_{DS} = 0\text{ V}$ | Q1 Q2 | | | ± 100 ± 100 | nA nA |

On Characteristics

| | | | | | | | |
|--|--|---|----------|------------|-------------------|-------------------|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$ | Q1 Q2 | 0.8 1.1 | 1.2 1.4 | 2.0 2.2 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$ | Q1 Q2 | | -4 -3 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = 10\text{ V}$, $I_D = 17.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 16\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 17.5\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$ | Q1 | | 3.8 4.4 5.4 | 5.0 5.7 7.0 | m Ω |
| | | $V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 27\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$ | Q2 | | 1.5 1.8 2.1 | 1.8 2.2 2.7 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{ V}$, $I_D = 17.5\text{ A}$ | Q1 | | 100 | | S |
| | | $V_{DS} = 5\text{ V}$, $I_D = 30\text{ A}$ | Q2 | | 240 | | |

Dynamic Characteristics

| | | | | | | | |
|-----------|------------------------------|--|----------|--|--------------|--|----------|
| C_{iss} | Input Capacitance | Q1: $V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | Q1 Q2 | | 1570 4045 | | pF |
| C_{oss} | Output Capacitance | Q2: $V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | Q1 Q2 | | 448 946 | | pF |
| C_{rss} | Reverse Transfer Capacitance | $V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | Q1 Q2 | | 61 117 | | pF |
| R_g | Gate Resistance | | Q1 | | 0.4 | | Ω |
| | | | Q2 | | 0.9 | | |

Switching Characteristics

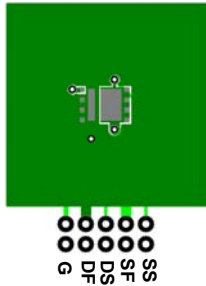
| | | | | | | | |
|--------------|-------------------------------|---|---|----|------------|--|----|
| $t_{d(on)}$ | Turn-On Delay Time | Q1: $V_{DD} = 13\text{ V}$, $I_D = 17.5\text{ A}$, $R_{GEN} = 6\text{ }\Omega$ | Q1 Q2 | | 7 11 | | ns |
| t_r | Rise Time | | Q1 Q2 | | 2 5 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | Q2: $V_{DD} = 13\text{ V}$, $I_D = 30\text{ A}$, $R_{GEN} = 6\text{ }\Omega$ | Q1 Q2 | | 23 39 | | ns |
| t_f | Fall Time | | Q1 Q2 | | 2 4 | | |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V}$ to 10 V | Q1 $V_{DD} = 13\text{ V}$, $I_D = 17.5\text{ A}$ | Q1 | 26 | | nC |
| | | | | Q2 | 59 | | |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V}$ to 4.5 V | Q1 $V_{DD} = 13\text{ V}$, $I_D = 17.5\text{ A}$ | Q1 | 12 | | nC |
| | | | | Q2 | 27 | | |
| Q_{gs} | Gate to Source Gate Charge | Q2 $V_{DD} = 13\text{ V}$, $I_D = 30\text{ A}$ | Q1 Q2 | | 3.3 8.2 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | Q1 Q2 | | 2.7 7.6 | | |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

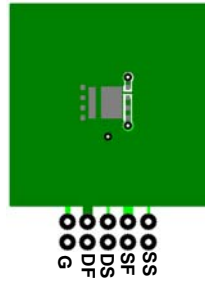
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|----------|---------------------------------------|---|------|-----|-----|-----|-------|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 17.5\text{ A}$ (Note 2) | Q1 | | 0.8 | 1.2 | V |
| | | $V_{GS} = 0\text{ V}, I_S = 30\text{ A}$ (Note 2) | Q2 | | 0.8 | 1.2 | |
| t_{rr} | Reverse Recovery Time | Q1 $I_F = 17.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | Q1 | | 23 | | ns |
| | | | Q2 | | 28 | | |
| Q_{rr} | Reverse Recovery Charge | Q2 $I_F = 30\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$ | Q1 | | 9 | | nC |
| | | | Q2 | | 28 | | |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 57 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1 : E_{AS} of 29 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1.2\text{ mH}, I_{AS} = 7\text{ A}, V_{DD} = 23\text{ V}, V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}, I_{AS} = 16\text{ A}$.

Q2: E_{AS} of 86 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 0.6\text{ mH}, I_{AS} = 17\text{ A}, V_{DD} = 23\text{ V}, V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}, I_{AS} = 31\text{ A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

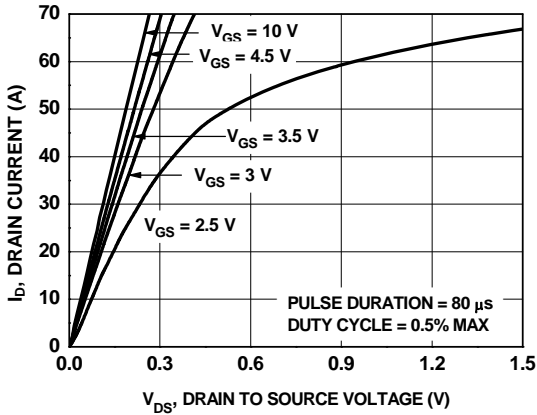


Figure 1. On Region Characteristics

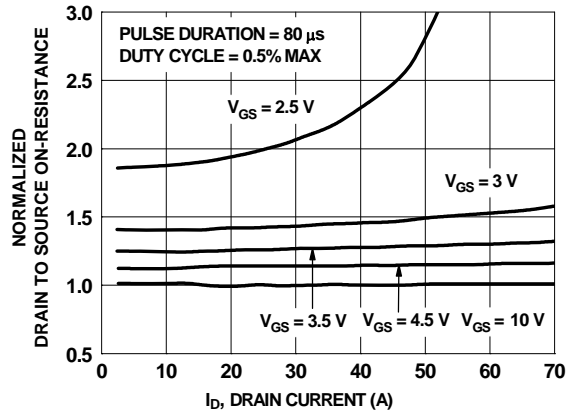


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

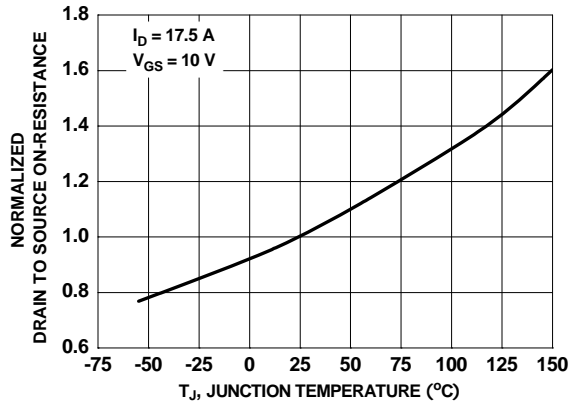


Figure 3. Normalized On Resistance vs Junction Temperature

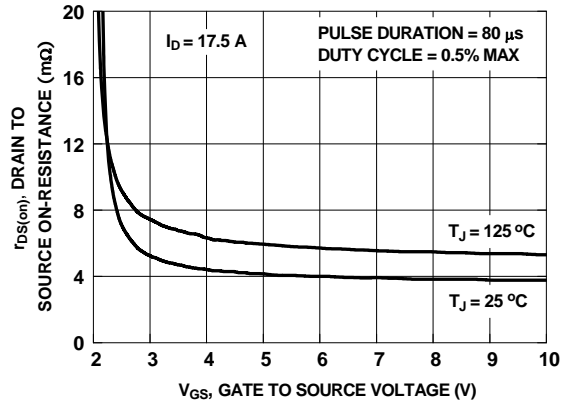


Figure 4. On-Resistance vs Gate to Source Voltage

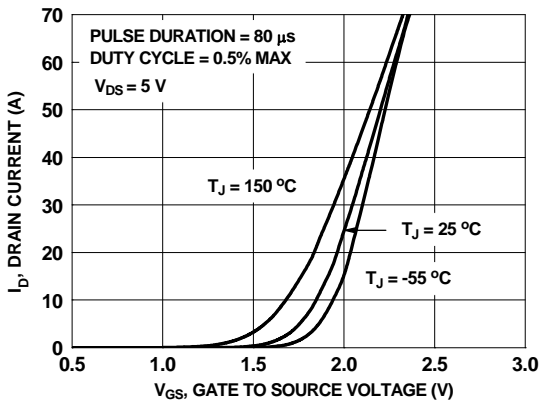


Figure 5. Transfer Characteristics

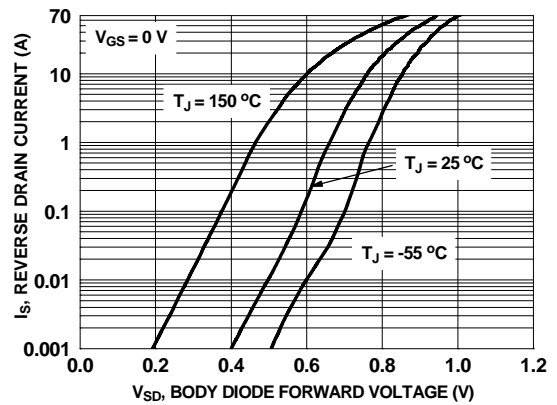


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

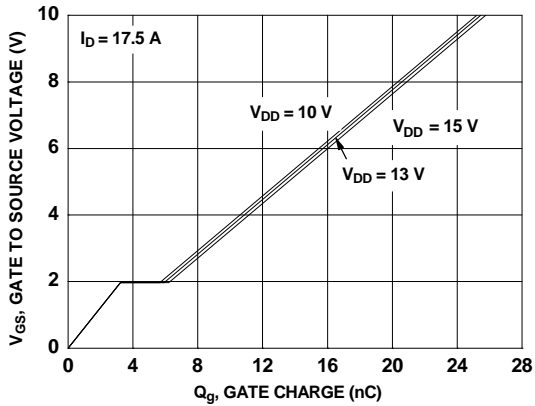


Figure 7. Gate Charge Characteristics

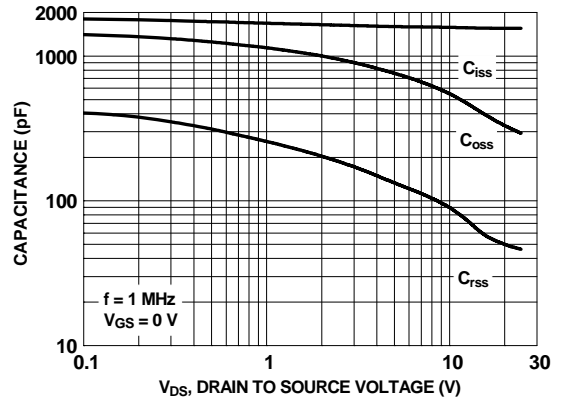


Figure 8. Capacitance vs Drain to Source Voltage

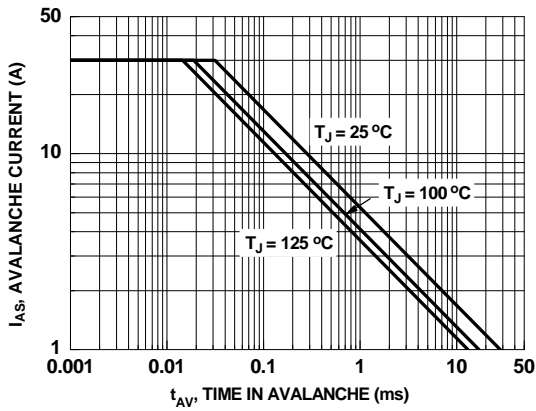


Figure 9. Unclamped Inductive Switching Capability

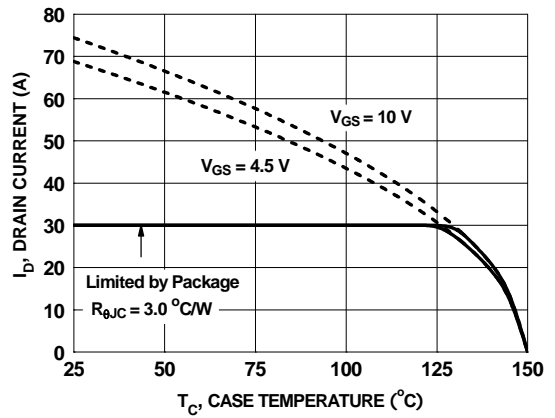


Figure 10. Maximum Continuous Drain Current vs Case Temperature

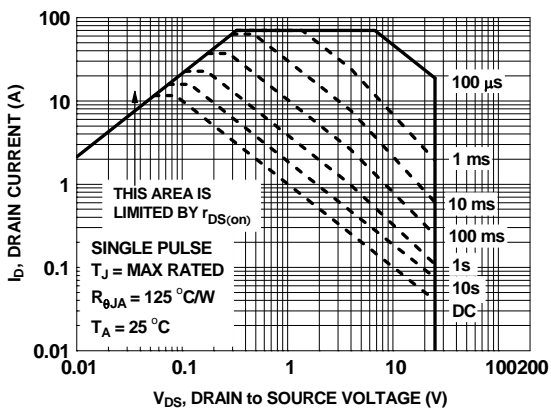


Figure 11. Forward Bias Safe Operating Area

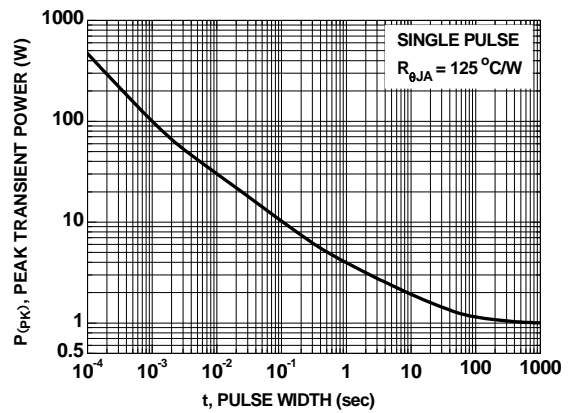


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

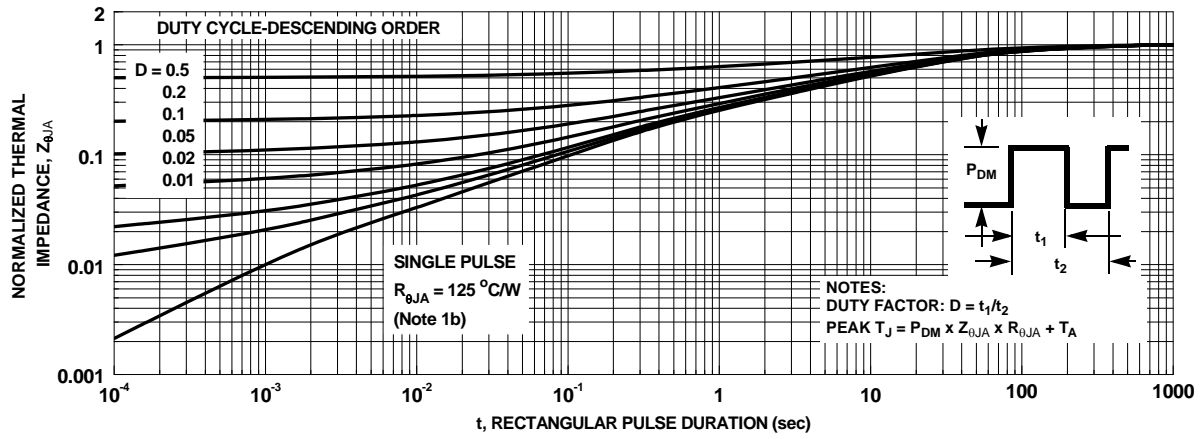


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

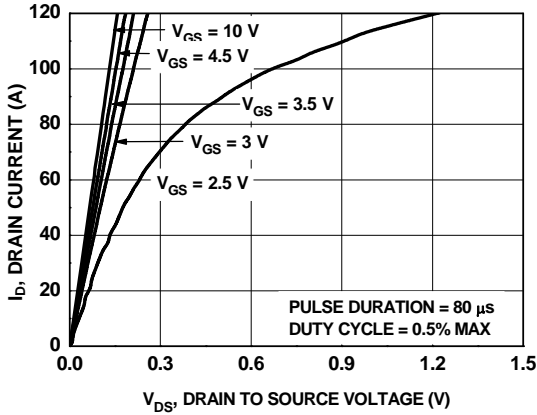


Figure 14. On-Region Characteristics

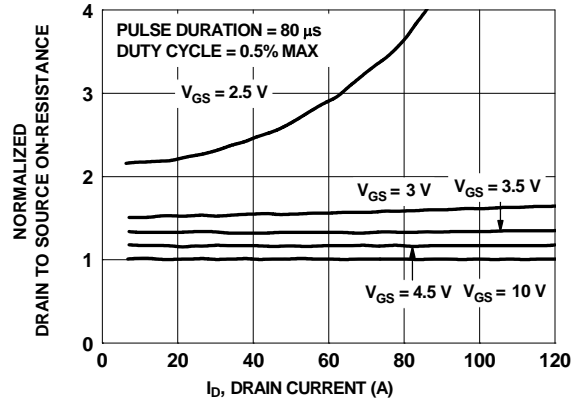


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

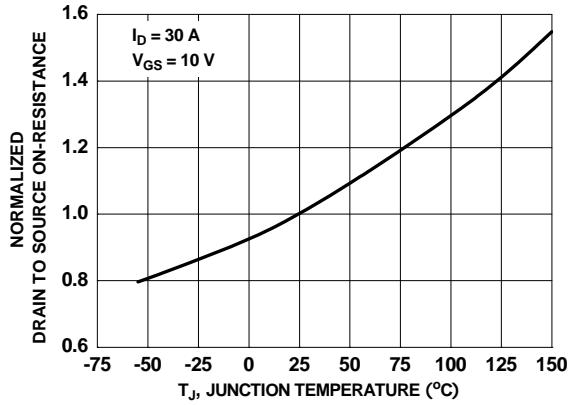


Figure 16. Normalized On-Resistance vs Junction Temperature

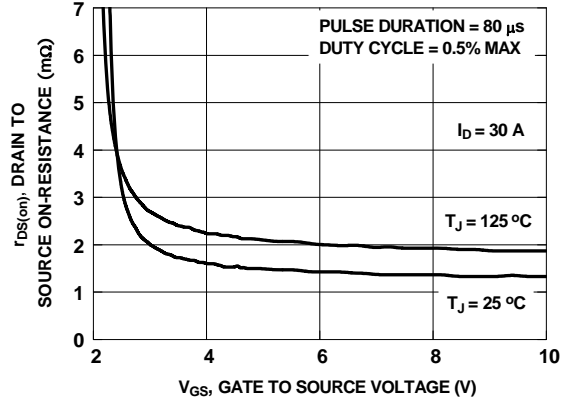


Figure 17. On-Resistance vs Gate to Source Voltage

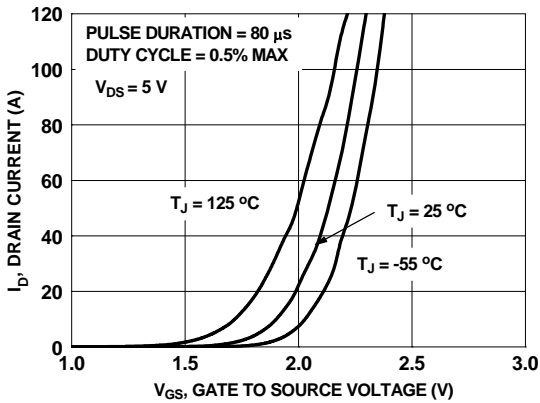


Figure 18. Transfer Characteristics

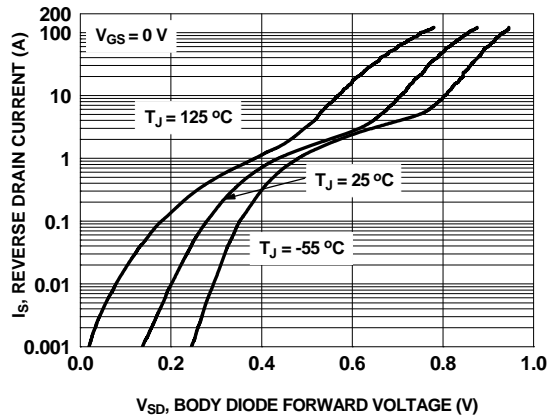


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

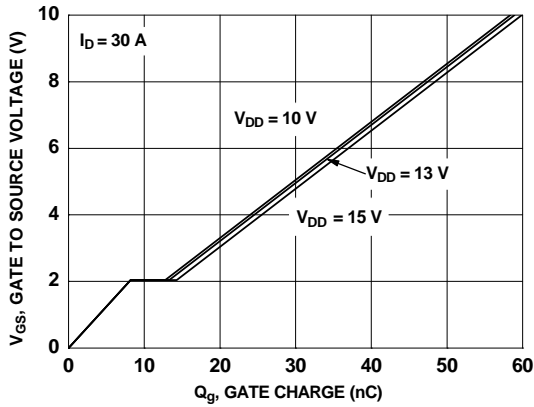


Figure 20. Gate Charge Characteristics

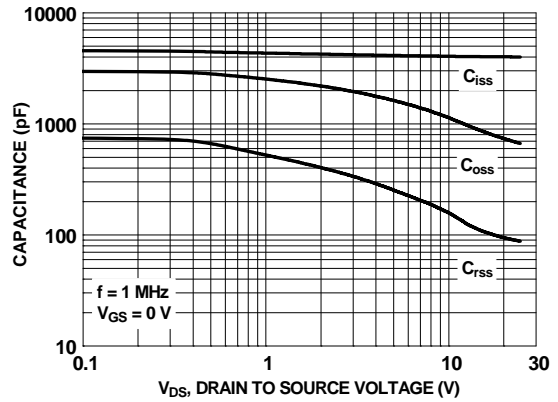


Figure 21. Capacitance vs Drain to Source Voltage

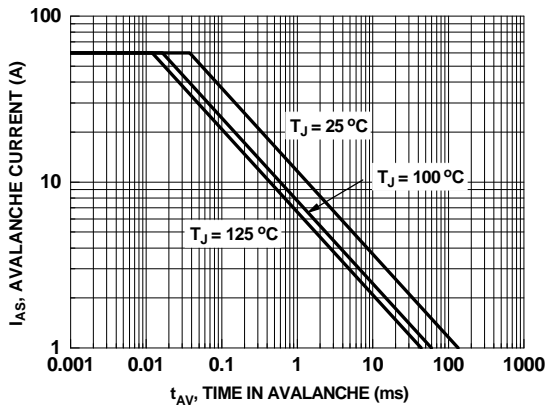


Figure 22. Unclamped Inductive Switching Capability

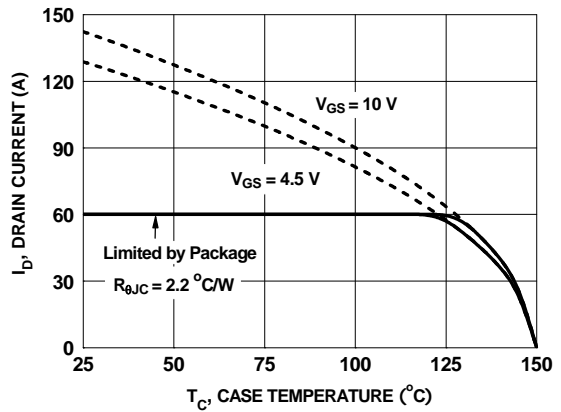


Figure 23. Maximum Continuous Drain Current vs Case Temperature

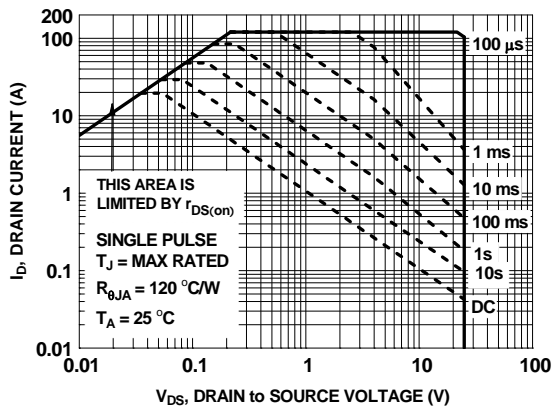


Figure 24. Forward Bias Safe Operating Area

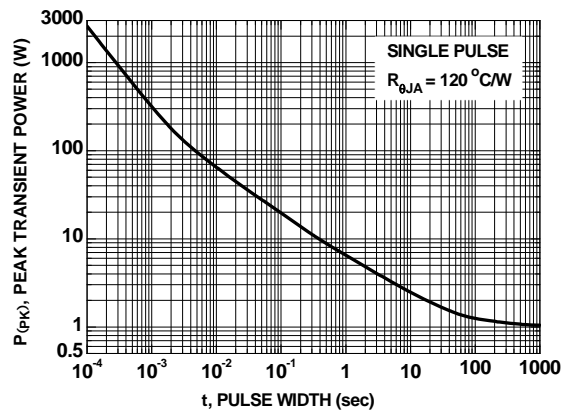


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

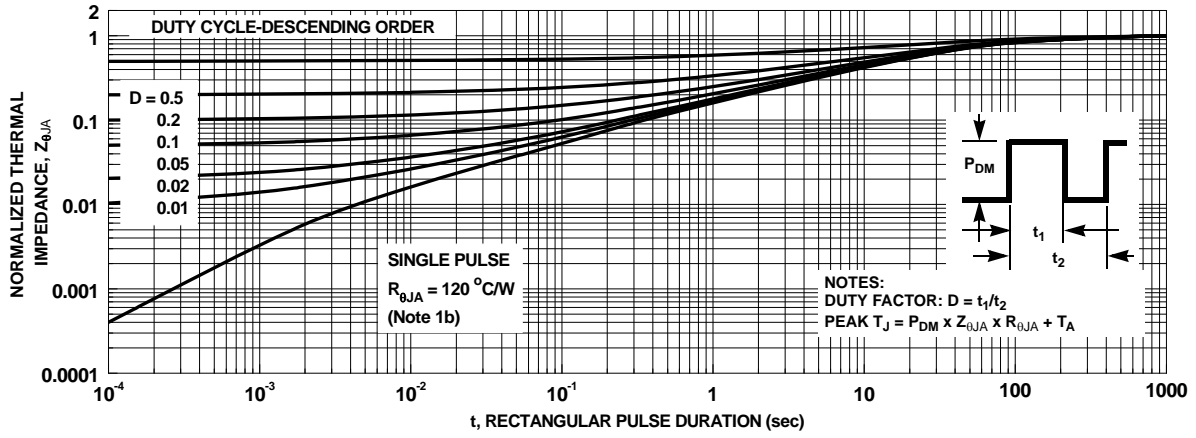


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3610S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

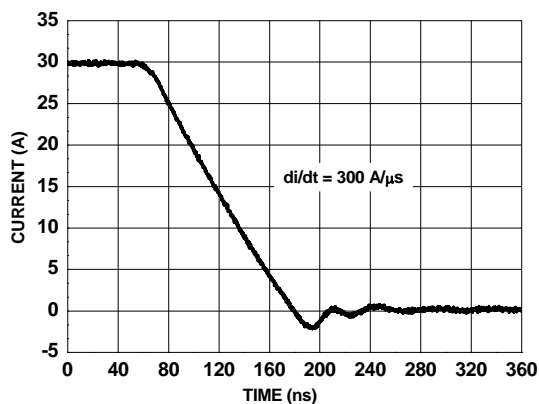


Figure 27. FDMS3610S SyncFET body diode reverse recovery characteristic

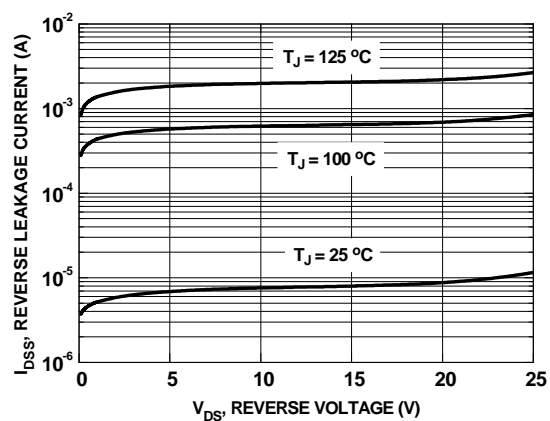
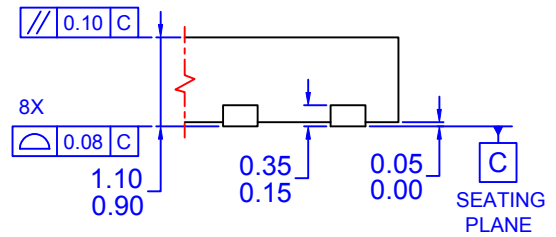
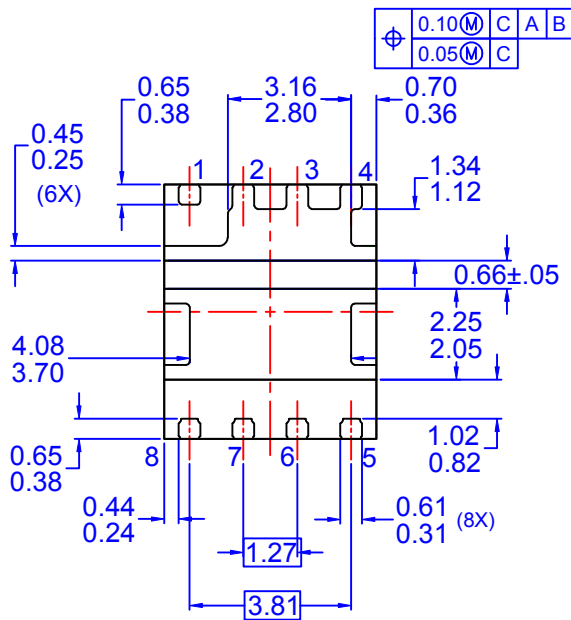
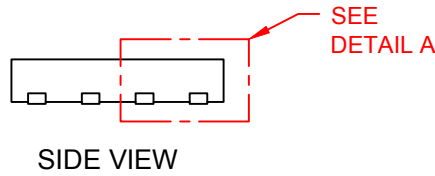
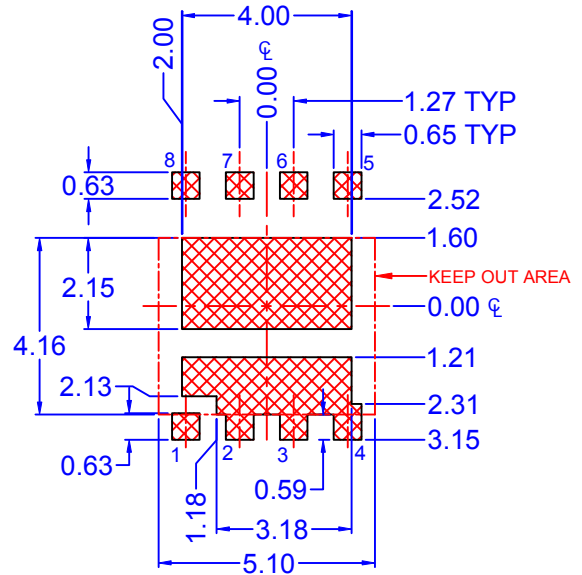
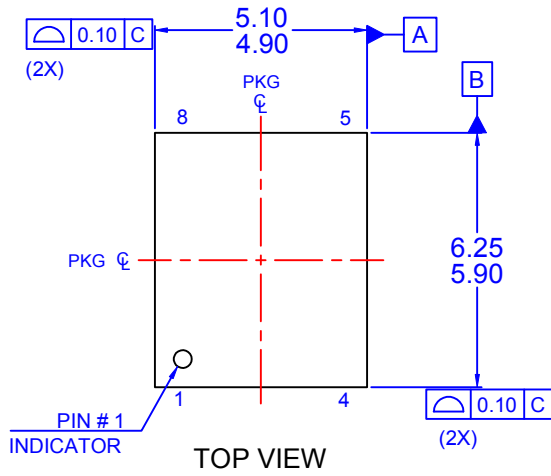
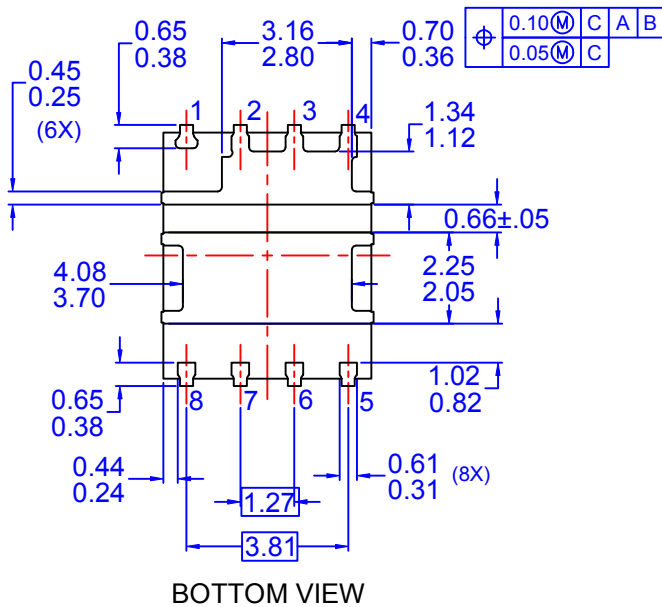
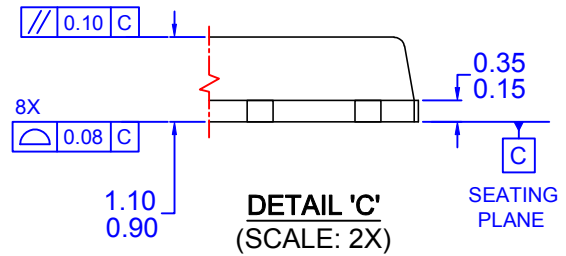
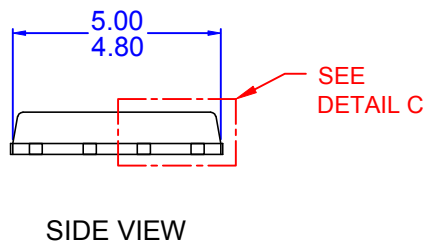
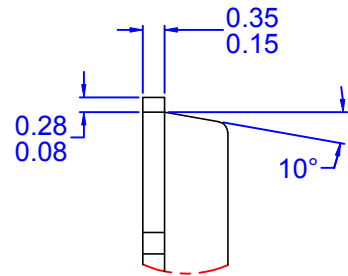
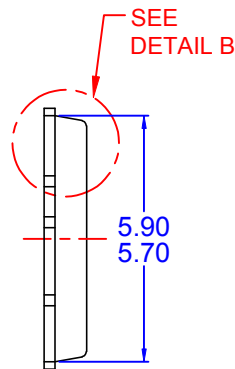
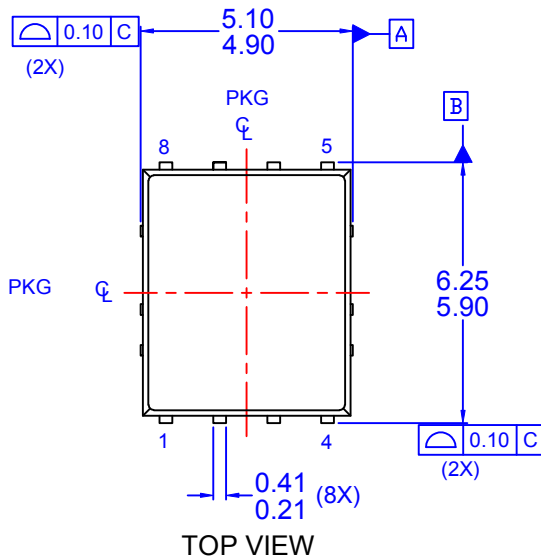


Figure 28. SyncFET body diode reverse leakage versus drain-source voltage




DETAIL 'A'
(SCALE: 2X)

BOTTOM VIEW
OPTION - A (SAWN TYPE)



OPTION - B (PUNCHED TYPE)

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
 - F) DRAWING FILE NAME: PQFN08EREV6.
 - G) FAIRCHILD SEMICONDUCTOR

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