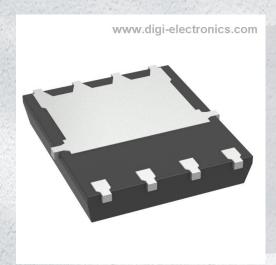


FDMS86181 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number FDMS86181-DG

Manufacturer onsemi

Manufacturer Product Number FDMS86181

Description MOSFET N-CH 100V 44A/124A 8PQFN

Detailed Description N-Channel 100 V 44A (Ta), 124A (Tc) 2.5W (Ta), 125

W (Tc) Surface Mount 8-PQFN (5x6)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDMS86181	onsemi
Series:	Product Status:
PowerTrench®	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
100 V	44A (Ta), 124A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
6V, 10V	4.2mOhm @ 44A, 10V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250μA	59 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	4125 pF @ 50 V
FET Feature:	Power Dissipation (Max):
	2.5W (Ta), 125W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (5x6)	8-PowerTDFN
Base Product Number:	
FDMS86	

Environmental & Export classification

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

www.onsemi.com

MOSFET - Power, Single N-Channel, Shielded Gate, POWERTRENCH[®] 100 V, 124 A, 4.2 mΩ

FDMS86181

General Description

This N-Channel MV MOSFET is produced using **onsemi**'s advanced POWERTRENCH[®] process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)} = 4.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 44 \text{ A}$
- Max $r_{DS(on)} = 12 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 22 \text{ A}$
- ADD
- 50% lower Qrr than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

Applications

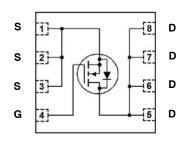
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DS}	Drain to Source Voltage	100	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current: - Continuous $T_C = 25^{\circ}C$ (Note 5) - Continuous $T_C = 100^{\circ}C$ (Note 5) - Continuous $T_A = 25^{\circ}C$ (Note 1a) - Pulsed (Note 4)	124 78 17 510	Α
E _{AS}	Single Pulse Avalanche Energy (Note 3)	337	mJ
P _D	Power Dissipation: $T_C = 25^{\circ}C$ $T_A = 25^{\circ}C$ (Note 1a)	125 2.5	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1



N-Channel MOSFET



MARKING DIAGRAM



\$Y = onsemi Logo &Z = Assembly Plant Code &3 = Data Code (Year & Week) &K = Lot FDMS86181 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMS86181	FDMS86181	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000/Tape&Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case	1.0	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
OFF CHARA	CTERISTICS			•		
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25°C		60		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
ON CHARAC	CTERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS}=V_{DS},I_D=250\;\mu A$	2.0	3.1	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25°C		-9		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 44 A		3.3	4.2	mΩ
		V _{GS} = 6 V, I _D = 22 A		5.3	12	
		V _{GS} = 10 V, I _D = 44 A, T _J = 125°C		5.7	7.8	
9FS	Forward Transconductance	V _{DS} = 10 V, I _D = 44 A		116		S
OYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		2945	4125	pF
C _{oss}	Output Capacitance			1730	2425	pF
C _{rss}	Reverse Transfer Capacitance			20	40	pF
R_g	Gate Resistance	f = 1MHz	0.1	1.3	2.6	Ω
WITCHING	CHARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 44 \text{ A}, V_{GS} = 10 \text{ V},$		17	31	ns
t _r	Rise Time	$R_{GEN} = 6 \Omega$		9	18	ns
t _{d(off)}	Turn-Off Delay Time			25	40	ns
t _f	Fall Time			6	12	ns
Qg	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 44 A		42	59	nC
		V_{GS} = 0 V to 6 V, V_{DD} = 50 V, I_D = 44 A		27	38	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 50 V, I _D = 44 A		13		nC
Q _{gd}	Gate to Drain "Miller" Charge			9.3		nC

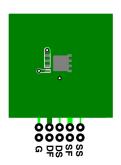
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit	
DRAIN-SOU	DRAIN-SOURCE DIODE CHARACTERISTICS						
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.1 A (Note 2)		0.7	1.2	V	
		V _{GS} = 0 V, I _S = 44 A (Note 2)		0.8	1.3		
t _{rr}	Reverse Recovery Time	I _F = 20 A, di/dt = 300 A/μs		32	52	ns	
Q _{rr}	Reverse Recovery Charge	1		57	92	nC	
t _{rr}	Reverse Recovery Time	I _F = 20 A, di/dt = 1000 A/μs		25	40	ns	
Q _{rr}	Reverse Recovery Charge			158	253	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

 R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θCA} is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 $^{\circ}$ C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 3. E_{AS} of 337 mJ is based on starting $T_J = 25^{\circ}C$, N-ch: L = 3 mH, $I_{AS} = 15$ A, $V_{DD} = 100$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 49$ A.
- 4. Pulsed Id please refer to Figure 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED)

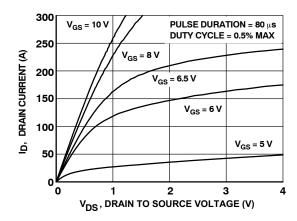


Figure 1. On Region Characteristics

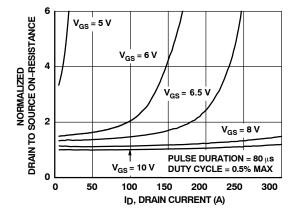


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C UNLESS OTHERWISE NOTED)

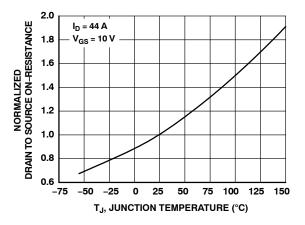


Figure 3. Normalized On Resistance vs. Junction Temperature

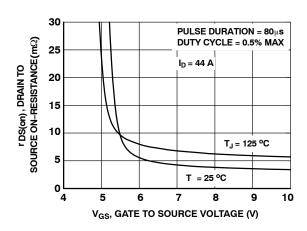


Figure 4. On-Resistance vs. Gate to Source Voltage

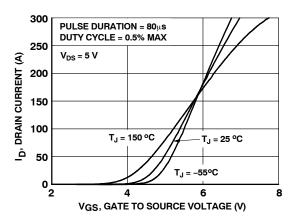


Figure 5. Transfer Characteristics

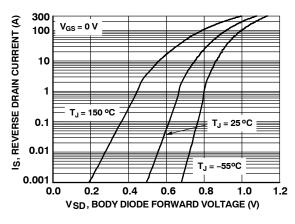


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

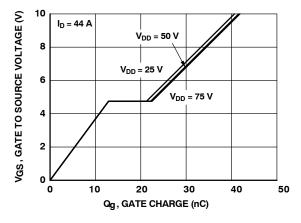


Figure 7. Gate Charge Characteristics

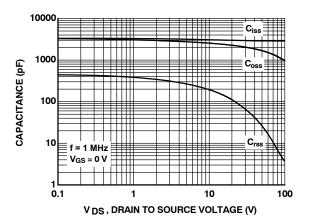


Figure 8. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C UNLESS OTHERWISE NOTED)

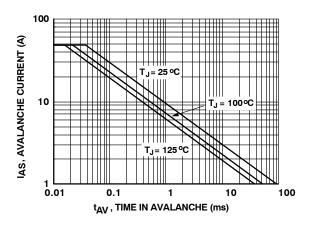


Figure 9. Unclamped Inductive Switching Capability

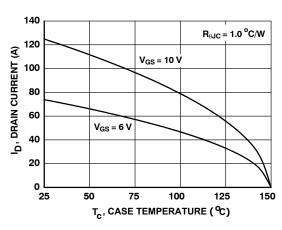


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

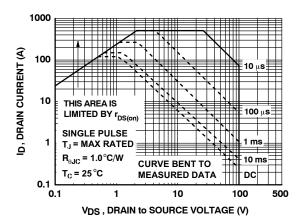


Figure 11. Forward Bias Safe Operating Area

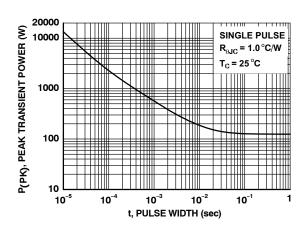


Figure 12. Single Pulse Maximum Power Dissipation

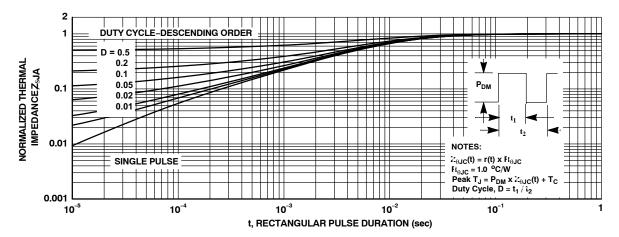


Figure 13. Transient Thermal Response Curve

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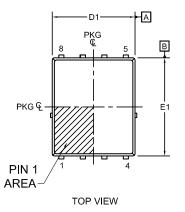


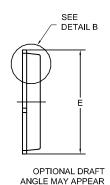
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



DATE 21 JAN 2022



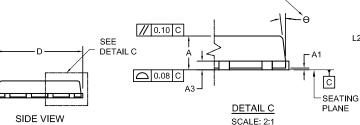


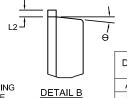
ON FOUR SIDES

OF THE PACKAGE

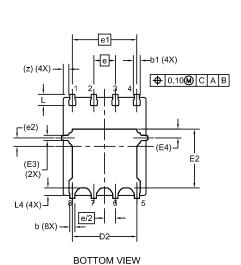


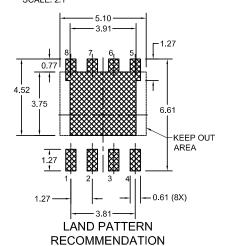
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.





SCALE: 2:1





*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS				
DIIVI	MIN.	NOM. MAX			
Α	0.90	1.00	1.10		
A1	0.00	-	0.05		
b	0.21	0.31	0.41		
b1	0.31	0.41	0.51		
А3	0.15	0.25	0.35		
D	4.90	5.00	5.20		
D1	4.80	4.90	5.00		
D2	3.61	3.82	3.96		
Е	5.90	6.15	6.25		
E1	5.70	5.80	5.90		
E2	3.38	3.48	3.78		
E3	0.30 REF				
E4	Ü).52 REF			
е	,	1.27 BSC	;		
e/2	(0.635 BS	С		
e1	* *	3.81 BSC	;		
e2	Û).50 REF	:		
L	0.51	0.66	0.76		
L2	0.05	0.18	0.30		
L4	0.34	0.44	0.54		
z	0.34 REF				
θ	0°	- 12°			

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DESCRIPTION:	PQFN8 5X6, 1.27P		PAGE 1 OF 1	

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