

## FDMS86581 Datasheet



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DiGi Electronics Part Number FDMS86581-DG

Manufacturer onsemi

Manufacturer Product Number FDMS86581

Description MOSFET N-CH 60V 30A 8PQFN

Detailed Description N-Channel 60 V 30A (Tc) 50W (Tj) Surface Mount 8-

PQFN (5x6)



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## **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:
FDMS86581	onsemi
Series:	Product Status:
	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
60 V	30A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ ld, Vgs:
10V	15mOhm @ 30A, 10V
Vgs(th) (Max) @ ld:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 250μA	19 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	881 pF @ 30 V
FET Feature:	Power Dissipation (Max):
	50W (Tj)
Operating Temperature:	Mounting Type:
-55°C ~ 175°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (5x6)	8-PowerTDFN
Base Product Number:	
FDMS86581	

## **Environmental & Export classification**

8541.29.0095

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	



# **MOSFET** – N-Channel, POWERTRENCH®

60 V, 30 A, 15 m $\Omega$ 

## FDMS86581

#### **Features**

- Typical  $R_{DS(on)} = 12.5 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 30 \text{ A}$
- Typical  $Q_{G(tot)} = 13 \text{ nC}$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 25 \text{ A}$
- UIS Capability
- RoHS Compliant

#### **Applications**

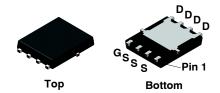
- DC-DC Power Supplies
- AC–DC Power Supplies
- Motor Control
- Load Switching

#### MOSFET MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V <sub>DSS</sub>	Drain-to-Source Voltage	60	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (VGS = 10) T <sub>C</sub> = 25°C (Note 1)	30	Α
	Pulsed Drain Current, T <sub>C</sub> = 25°C	See Figure 4	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 2)	13.5	mJ
P <sub>D</sub>	Power Dissipation	50	W
	Derate Above 25°C	0.33	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	°C/W

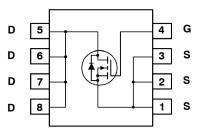
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Current is limited by bondwire configuration.
- 2. Starting  $T_J$  = 25°C,  $\dot{L}$  = 40  $\mu$ H,  $I_{AS}$  = 26 A,  $V_{DD}$  = 60 V during inductor charging and  $V_{DD}$  = 0 V during time in avalanche.
- 3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.



Power 56 (PQFN8 5x6) CASE 483AE

#### **ELECTRICAL CONNECTION**



**N-Channel MOSFET** 

#### **MARKING DIAGRAM**

\$Y&Z&3&K FDMS 86581

\$Y = onsemi Logo &Z = Assembly Plant Code &3 = Numeric Date Code

&K = Lot Code

FDMS86581 = Specific Device Code

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 6 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>.I</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Тур.	Max.	Units
OFF CHARA	ACTERISTICS	-			-	<u>-</u>	-
B <sub>VDSS</sub>	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		60	_	_	V
I <sub>DSS</sub>	I <sub>DSS</sub> Drain-to-Source Leakage Current	$V_{DS} = 60 \text{ V},$ $V_{GS} = 0 \text{ V}$ $T_{J} = 25^{\circ}\text{C}$ $T_{J} = 175^{\circ}\text{C}$ (Note 4)	T <sub>J</sub> = 25°C	-	-	1	Α
			T <sub>J</sub> = 175°C (Note 4)	-	-	1	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±[20 V		-	-	±100	nA
ON CHARAC	CTERISTICS						
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$		2.0	2.7	4.0	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 30 A,	T <sub>J</sub> = 25°C	-	12.5	15.0	mΩ
		V <sub>GS</sub> = 10 V	T <sub>J</sub> = 175°C (Note 4)	_	25.1	30.1	mΩ
DYNAMIC C	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz		-	881	_	pF
C <sub>oss</sub>	Output Capacitance			-	281	_	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			_	15	-	pF
$R_{G}$	Gate Resistance	f = 1 MHz		_	3.1	-	Ω
Q <sub>g(ToT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10 V, V <sub>DD</sub> = 30 V, I <sub>D</sub> = 25 A		-	13	19	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2 V, V <sub>DD</sub> = 30 V, I <sub>D</sub> = 25 A		-	2	_	nC
$Q_{gs}$	Gate-to-Source Gate Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 25 A		-	4	_	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge			_	3	-	nC
SWITCHING	CHARACTERISTICS						
t <sub>on</sub>	Turn-On Time	$V_{DD} = 30 \text{ V}, I_D = 30 \text{ A}, V_{GS} = 10 \text{ V},$		-	_	20	ns
t <sub>d(on)</sub>	Turn-On Delay	$R_{GEN} = 6 \Omega$		-	9	-	ns
t <sub>r</sub>	Rise Time	1		_	5	-	ns
t <sub>d(off)</sub>	Turn-Off Delay	<del>-</del> - -		-	15	_	ns
t <sub>f</sub>	Fall Time			-	4	_	ns
t <sub>off</sub>	Turn-Off Time			-	-	28	ns
DRAIN-SOU	JRCE DIODE CHARACTERISTICS						
V <sub>SD</sub> Source-to-Drain Diode Voltage		I <sub>SD</sub> = 30 A, V <sub>GS</sub> = 0 V		-	-	1.25	V
		$I_{SD} = 15 \text{ A}, V_{GS} = 0$	V	-		1.2	V
t <sub>rr</sub>	Reverse-Recovery Time	$I_F = 30 \text{ A}, dI_{SD}/dt = 30 \text{ A}$	100 A/μs, V <sub>DD</sub> = 48 V	-	37	55	ns
Q <sub>rr</sub>	Reverse Recovery Charge	]		_	22	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

#### **TYPICAL CHARACTERISTICS**

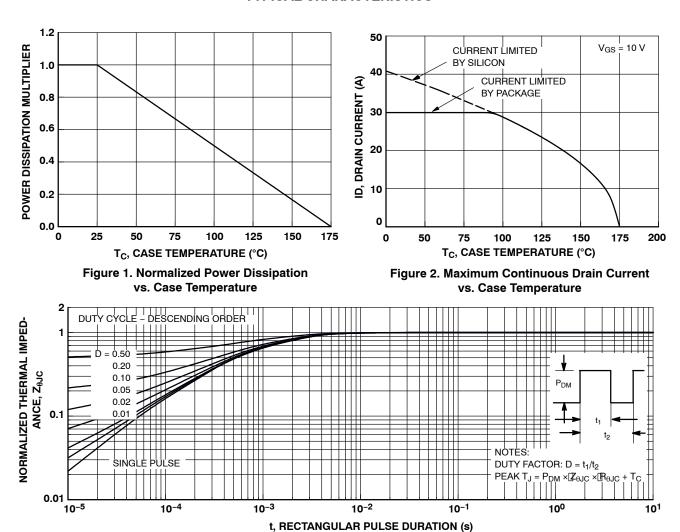


Figure 3. Normalized Maximum Transient Thermal Impedance

#### TYPICAL CHARACTERISTICS (continued)

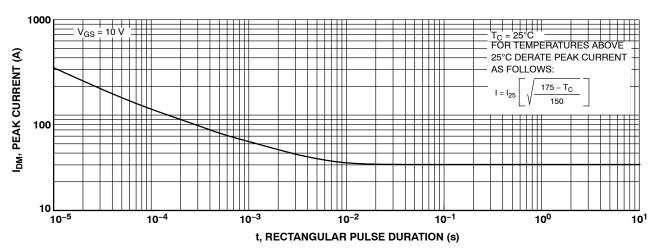


Figure 4. Peak Current Capability

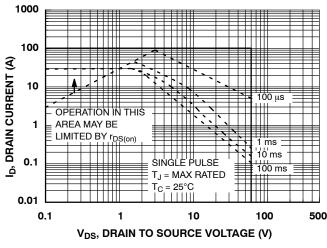
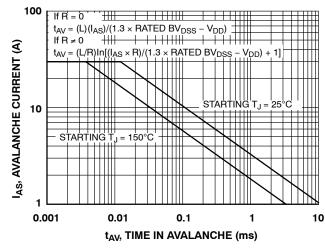


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes <u>AN7514</u> and <u>AN7515</u>.

Figure 6. Unclamped Inductive Switching Capability

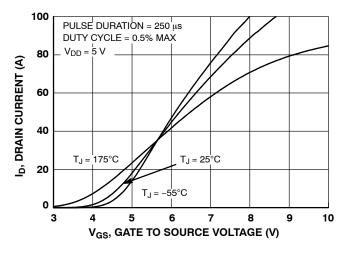


Figure 7. Transfer Characteristics

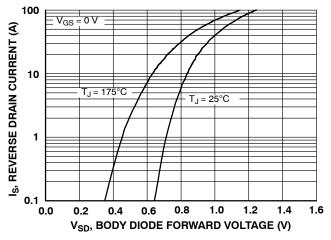


Figure 8. Forward Diode Characteristics

#### TYPICAL CHARACTERISTICS (CONTINUED)

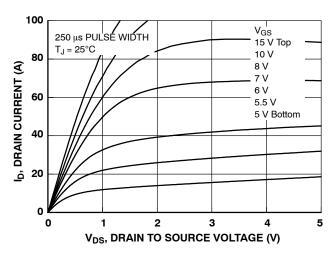
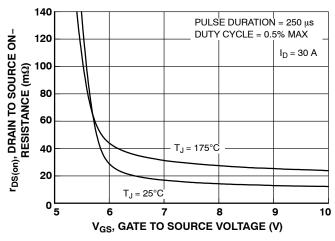
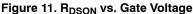


Figure 9. Saturation Characteristics

Figure 10. Saturation Characteristics





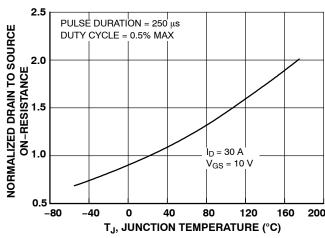


Figure 12. Normalized R<sub>DSON</sub> vs. Junction Temperature

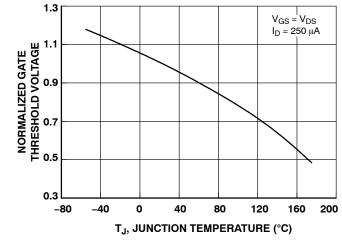


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

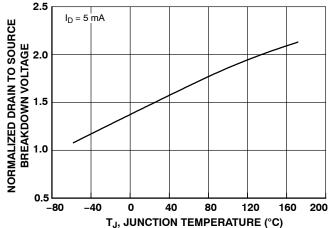
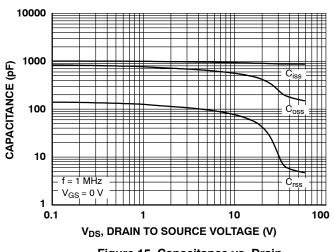


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

#### TYPICAL CHARACTERISTICS (continued)



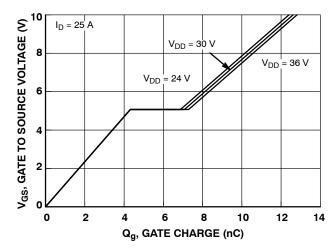


Figure 15. Capacitance vs. Drain to Source Voltage

Figure 16. Gate Charge vs. Gate to Source Voltage

#### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping <sup>†</sup>
FDMS86581	FDMS86581	Power 56	3000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <a href="https://example.com/BRD8011/D">BRD8011/D</a>.

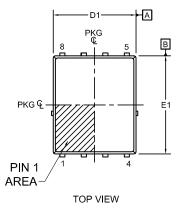


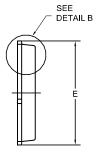
## **MECHANICAL CASE OUTLINE**

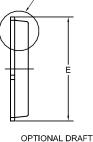
## PACKAGE DIMENSIONS



**DATE 21 JAN 2022** 





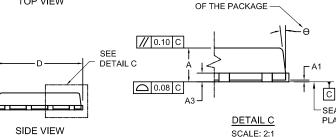


ANGLE MAY APPEAR

ON FOUR SIDES

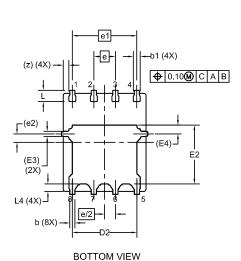
#### NOTES:

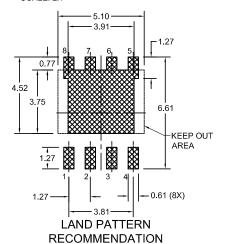
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



<del>ل</del> 22

SEATING **DETAIL B** PLANE SCALE: 2:1





\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS			
DIIVI	MIN.	NOM.	MAX.	
Α	0.90	1.00	1.10	
A1	0.00	-	0.05	
b	0.21	0.31	0.41	
b1	0.31	0.41	0.51	
А3	0.15	0.25	0.35	
D	4.90	5.00	5.20	
D1	4.80	4.90	5.00	
D2	3.61	3.82	3.96	
Е	5.90	6.15	6.25	
E1	5.70	5.80	5.90	
E2	3.38	3.48	3.78	
E3	0.30 REF			
E4	(	0.52 REF		
е	1.27 BSC			
e/2	0.635 BSC			
e1	3.81 BSC			
e2	0.50 REF			
L	0.51	0.66	0.76	
L2	0.05	0.18	0.30	
L4	0.34	0.44	0.54	
z	0.34 REF			
θ	0°	-	12°	

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DESCRIPTION:	PQFN8 5X6, 1.27P		PAGE 1 OF 1	

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