

FDP8D5N10C Datasheet

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DiGi Electronics Part Number	FDP8D5N10C-DG
Manufacturer	onsemi
Manufacturer Product Number	FDP8D5N10C
Description	MOSFET N-CH 100V 76A TO220-3
Detailed Description	N-Channel 100 V 76A (Tc) 2.4W (Ta), 107W (Tc) Through Hole TO-220-3



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Purchase and inquiry

Manufacturer Product Number:

FDP8D5N10C

Series:

PowerTrench®

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

100 V

Drive Voltage (Max Rds On, Min Rds On):

10V

Vgs(th) (Max) @ Id:

4V @ 130µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Supplier Device Package:

TO-220-3

Base Product Number:

FDP8D5

Manufacturer:

onsemi

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

76A (Tc)

Rds On (Max) @ Id, Vgs:

8.5mOhm @ 76A, 10V

Gate Charge (Qg) (Max) @ Vgs:

34 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

2475 pF @ 50 V

Power Dissipation (Max):

2.4W (Ta), 107W (Tc)

Mounting Type:

Through Hole

Package / Case:

TO-220-3

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

Not Applicable

ECCN:

EAR99

MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 76 A, 8.5 mΩ
**FDP8D5N10C,
FDPF8D5N10C**

General Description

This N-Channel MV MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

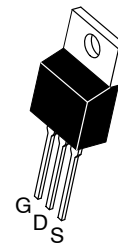
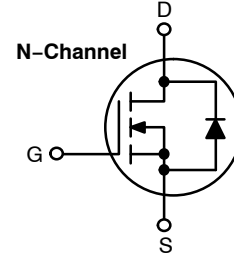
- Max $R_{DS(on)}$ = 8.5 mΩ at $V_{GS} = 10$ V, $I_D = 76$ A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIL Tested
- RoHS Compliant

Applications

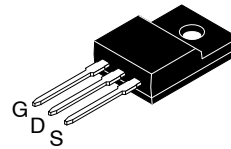
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	8.5 mΩ @ 10 V	76 A*

*Drain current limited by maximum junction temperature.



TO-220
CASE 221A



TO-220 Fullpack, 3-Lead
/ TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



XXX8D5N10C = Device Code (XXX = FDP, FDPF)
 A = Assembly Location
 YWW = Date Code (Year & Week)
 ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDP8D5N10C	TO-220	800 Units / Tube
FDPF8D5N10C	TO-220F	1000 Units / Tube

FDP8D5N10C, FDPF8D5N10C**MOSFET MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating		Unit
			FDP8D5N10C	FDPF8D5N10C	
V_{DS}	Drain to Source Voltage		100	100	V
V_{GS}	Gate to Source Voltage		± 20	± 20	V
I_D	Drain Current	- Continuous, $T_C = 25^\circ\text{C}$ (Note 3)	76	76*	A
		- Continuous, $T_C = 100^\circ\text{C}$ (Note 3)	54	54*	
		- Pulsed (Note 1)	304	304*	
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		181		mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	107	35	W
		$T_A = 25^\circ\text{C}$	2.4	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +175		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Pulsed I_D please refer to Figure 11 and Figure 12 "Forward Bias Safe Operating Area" for more details.
2. E_{AS} of 181 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 11\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 25\text{ A}$.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP8D5N10C	FDPF8D5N10C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	4.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

FDP8D5N10C, FDPF8D5N10C**ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	57	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	μA
		$V_{DS} = 80 \text{ V}, T_J = 150^\circ\text{C}$	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 130 \mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 76 \text{ A}$	–	7.4	8.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 76 \text{ A}$	–	68	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	1765	2475	pF
C_{oss}	Output Capacitance		–	1010	1415	pF
C_{rss}	Reverse Transfer Capacitance		–	16	25	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 76 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	–	12	22	ns
t_r	Rise Time		–	11	20	ns
$t_{d(off)}$	Turn-Off Delay Time		–	18	28	ns
t_f	Fall Time		–	4	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 76 \text{ A}$	–	25	34	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50 \text{ V}, I_D = 76 \text{ A}$	–	9	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	5	–	nC
Q_{oss}	Output Charge	$V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	–	68	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current	–	–	76	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	304	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 76 \text{ A}$	–	1.0	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 50 \text{ V}, I_F = 76 \text{ A}, dl_F/dt = 100 \text{ A}/\mu\text{s}$	–	58	92	ns
Q_{rr}	Reverse Recovery Charge		–	53	85	nC
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 50 \text{ V}, I_F = 76 \text{ A}, dl_F/dt = 300 \text{ A}/\mu\text{s}$	–	51	81	ns
Q_{rr}	Reverse Recovery Charge		–	141	226	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDP8D5N10C, FDPF8D5N10C

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

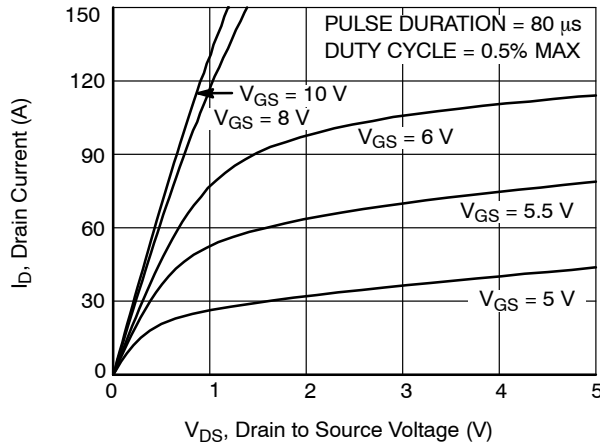


Figure 1. On-Region Characteristics

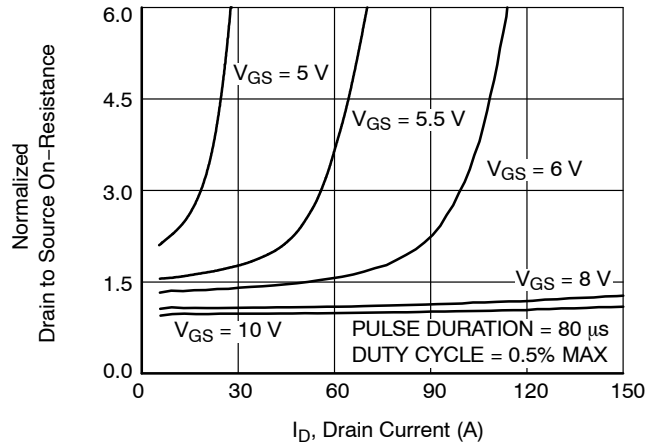


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

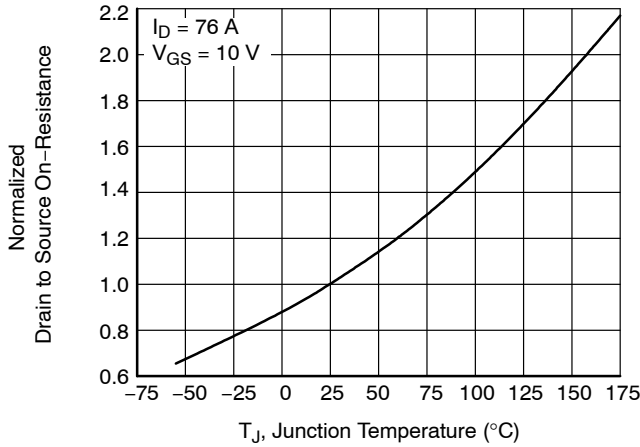


Figure 3. Normalized On-Resistance vs. Junction Temperature

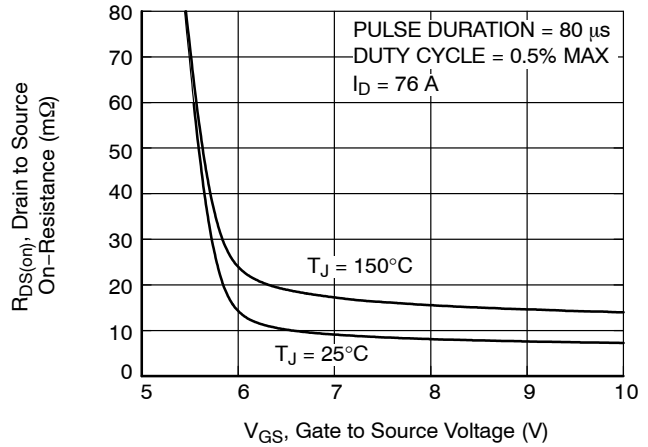


Figure 4. On-Resistance vs. Gate to Source Voltage

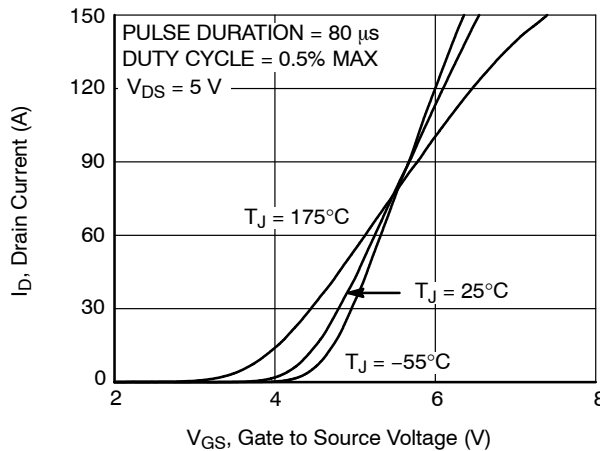


Figure 5. Transfer Characteristics

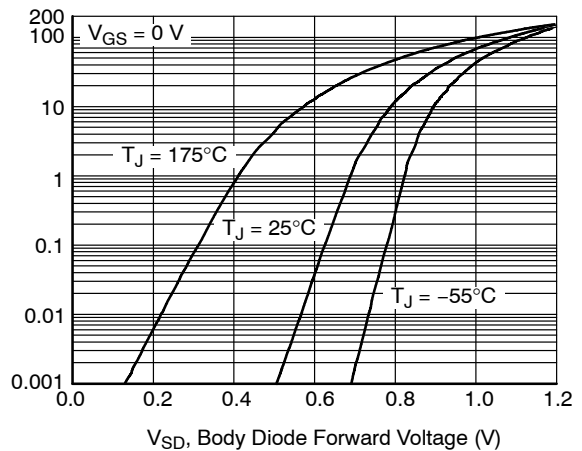


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDP8D5N10C, FDPF8D5N10C

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

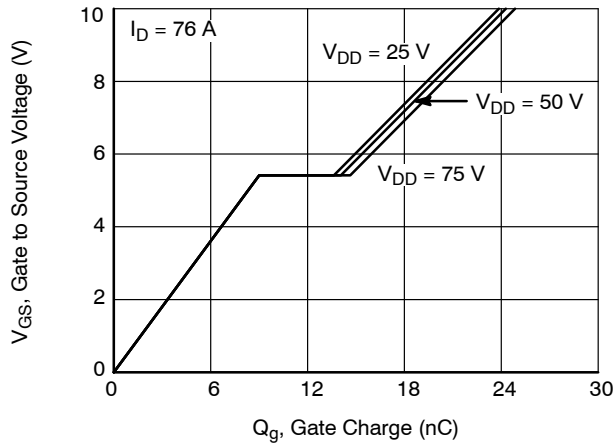


Figure 7. Gate Charge Characteristics

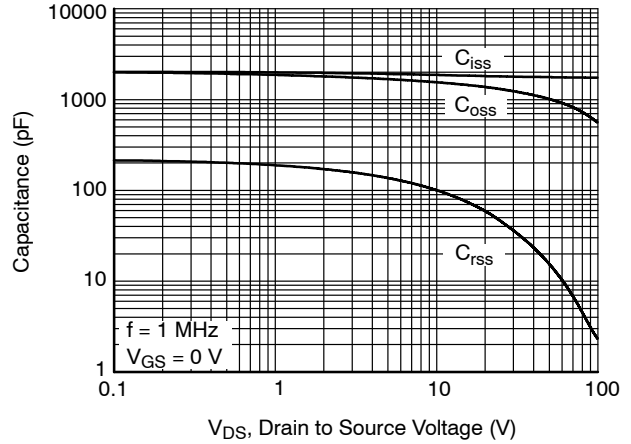


Figure 8. Capacitance vs. Drain to Source Voltage

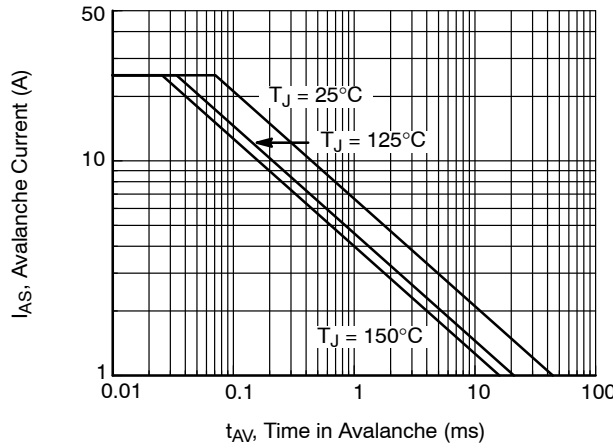


Figure 9. Unclamped Inductive Switching Capability

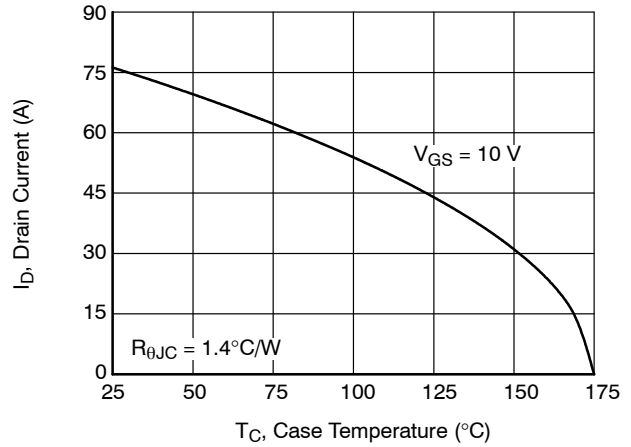


Figure 10. Maximum Continuous Drain Current vs. Case Temperature for FDP8D5N10C

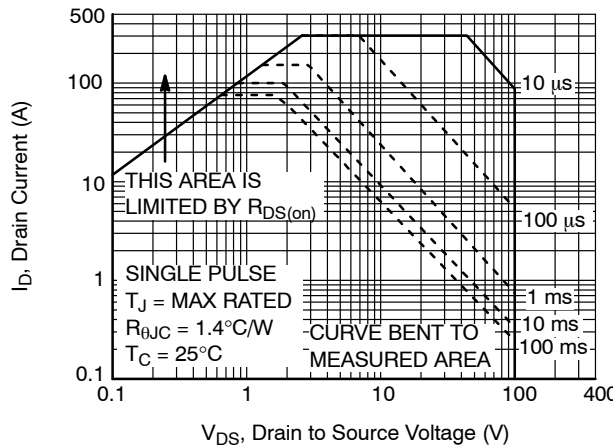


Figure 11. Forward Bias Safe Operating Area for FDP8D5N10C

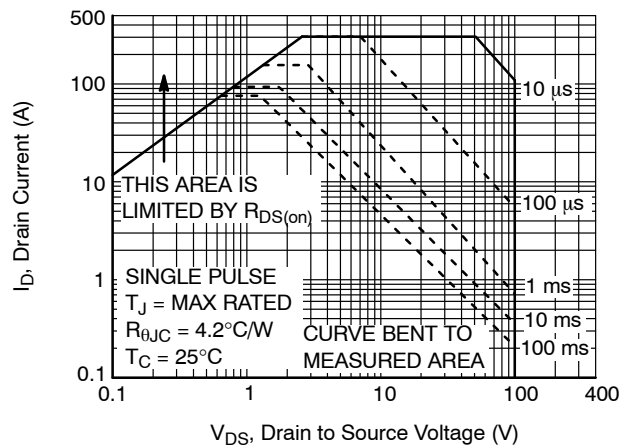


Figure 12. Forward Bias Safe Operating Area for FDPF8D5N10C

FDP8D5N10C, FDPF8D5N10C

TYPICAL PERFORMANCE CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

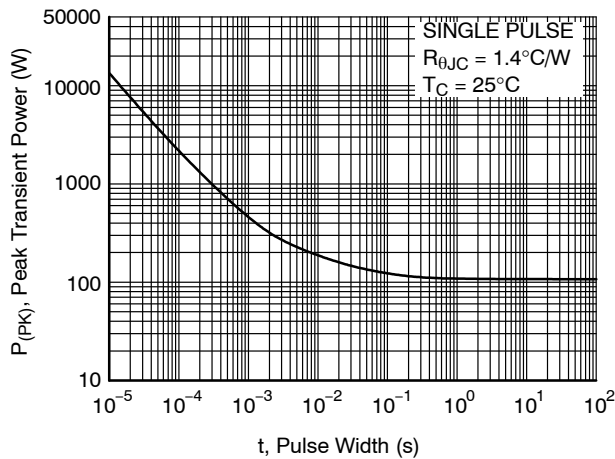


Figure 13. Single Pulse Maximum Power Dissipation for FDP8D5N10C

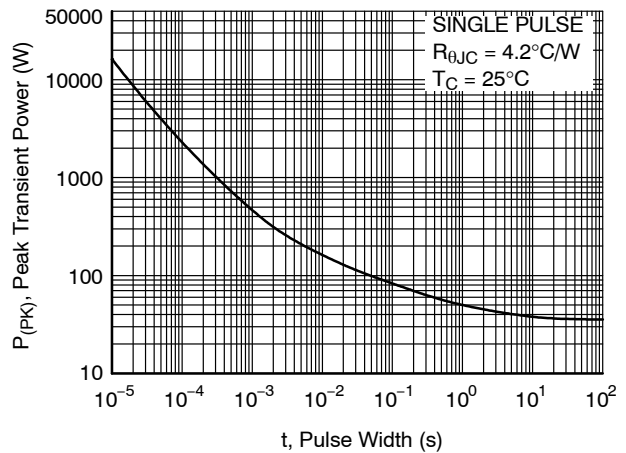


Figure 14. Single Pulse Maximum Power Dissipation for FDPF8D5N10C

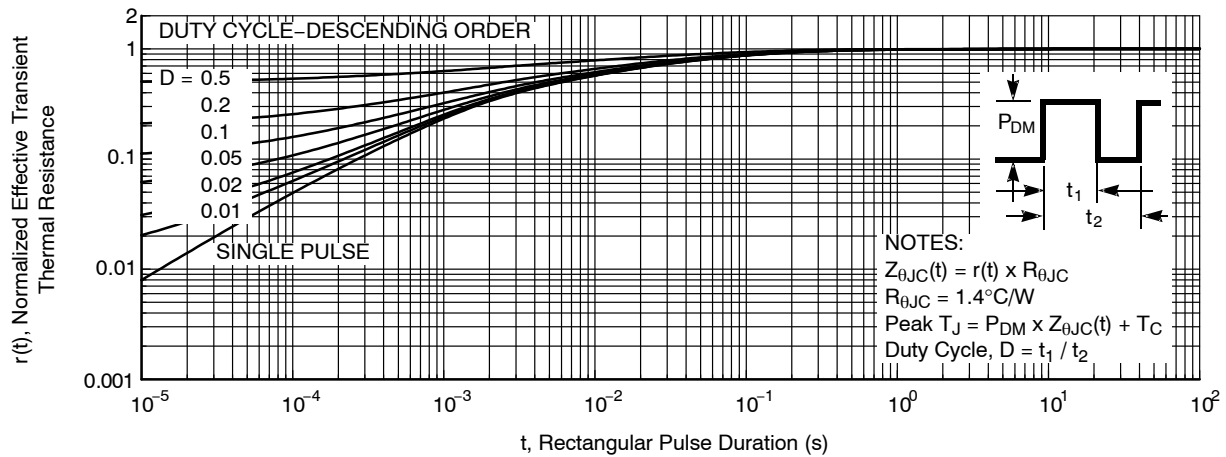


Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP8D5N10C

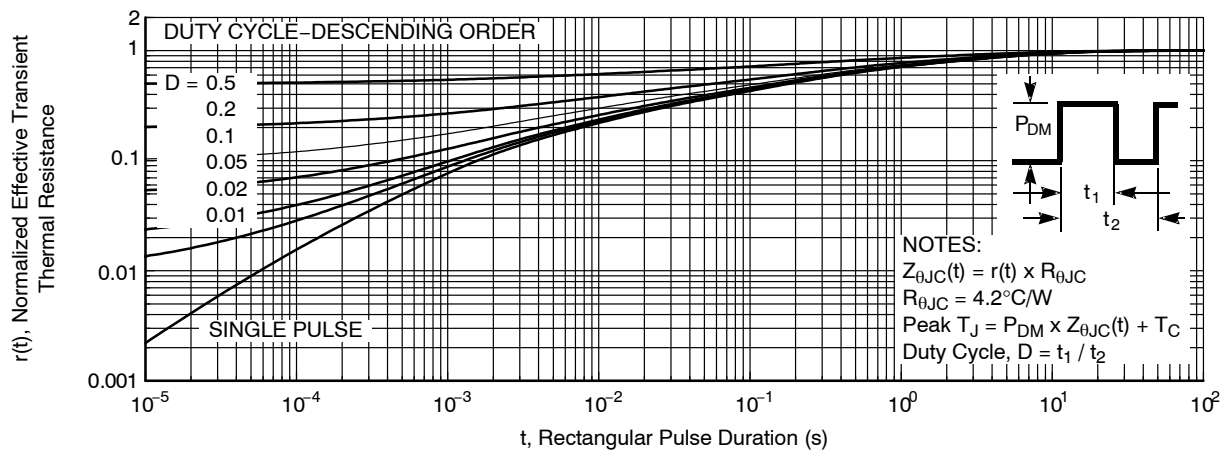


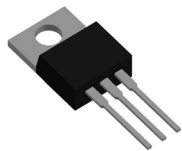
Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF8D5N10C

FDP8D5N10C, FDPF8D5N10C

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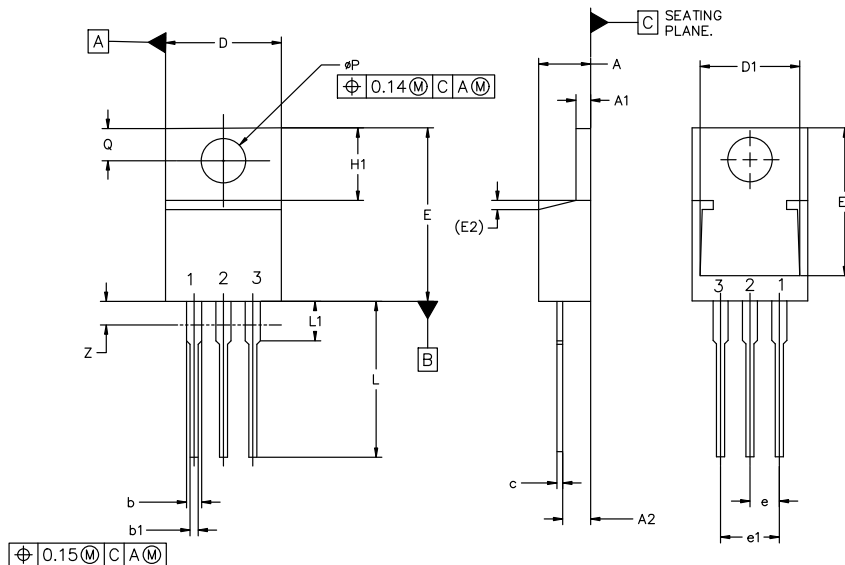


MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO-220-3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
φP	3.60	3.85	4.09
Z	---	---	3.48

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

- | | | | |
|--|--|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER</p> | <p>STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2</p> |
| <p>STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE</p> |
| <p>STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE</p> | <p>STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE</p> | <p>STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED</p> |

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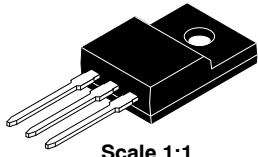
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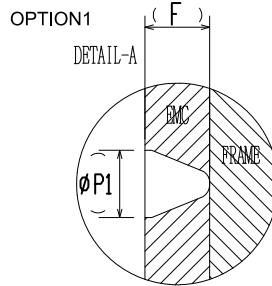
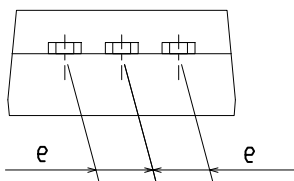
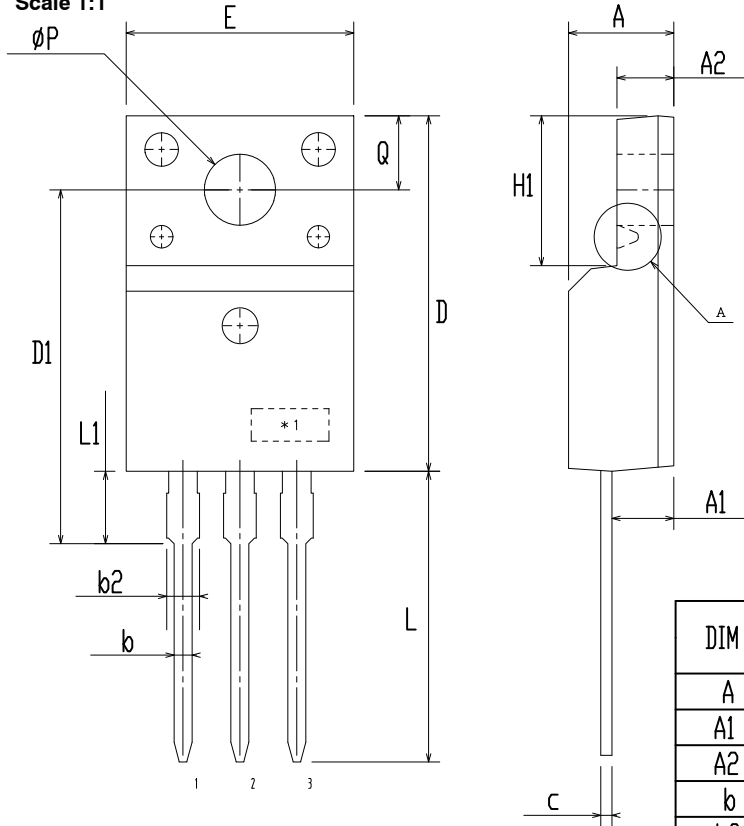
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**

**TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE B**

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
∅ P	2.98	3.18	3.38
∅ P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD / TO-220F-3SG	PAGE 1 OF 1

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