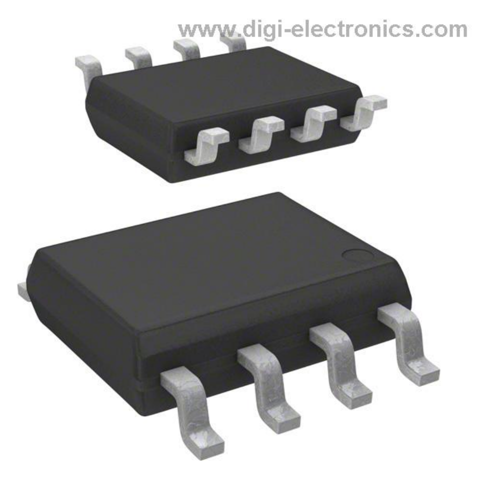
FDR844P Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	FDR844P-DG
Manufacturer	onsemi
Manufacturer Product Number	FDR844P
Description	MOSFET P-CH 20V 10A SUPERSOT8
Detailed Description	P-Channel 20 V 10A (Ta) 1.8W (Ta) Surface Mount SuperSOT™-8

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDR844P	onsemi
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
20 V	10A (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
1.8V, 4.5V	11mOhm @ 10A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
1.5V @ 250μA	74 nC @ 4.5 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±8V	4951 pF @ 10 V
FET Feature:	Power Dissipation (Max):
-	1.8W (Ta)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
SuperSOT™-8	8-LSOP (0.130", 3.30mm Width)
Base Product Number:	
FDR84	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

FAIRCHILD
SEMICONDUCTOR™

October 2001

FDR844P

P-Channel 1.8V Specified PowerTrench® MOSFET

General Description

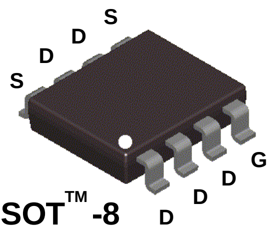
This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

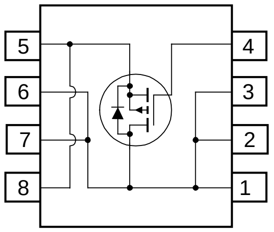
- Power management
- Load switch
- Battery protection

Features

- –10 A, –20 V. $R_{DS(ON)} = 11\ m\Omega$ @ $V_{GS} = -4.5\ V$
  $R_{DS(ON)} = 14\ m\Omega$ @ $V_{GS} = -2.5\ V$
  $R_{DS(ON)} = 20\ m\Omega$ @$V_{GS} = -1.8\ V$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



SuperSOT™ -8



Absolute Maximum Ratings

$T_A=25^{o}C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		± 8	V
I_D	Drain Current – Continuous	(Note 1a)	–10	A
	– Pulsed		–50	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.8	W
		(Note 1b)	1.0	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.844P	FDR844P	13''	12mm	2500 units

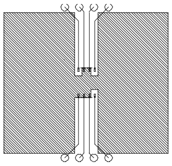
Electrical Characteristics

T_A = 25°C unless otherwise noted

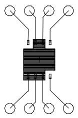
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16V, V_{GS} = 0 V			–1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –8 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.7	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –10 A V_{GS} = –2.5 V, I_D = –9 A V_{GS} = –1.8 V, I_D = –7.5 A V_{GS}= –4.5 V, I_D = –10 A, T_J=125°C		7 9.5 13 9.5	11 14 20 15	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–50			A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –10 A		57		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		4951		pF
C_{oss}	Output Capacitance			884		pF
C_{rss}	Reverse Transfer Capacitance			451		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		16	29	ns
t_r	Turn–On Rise Time			9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			196	314	ns
t_f	Turn–Off Fall Time			78	125	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –10 A, V_{GS} = –4.5 V		53	74	nC
Q_{gs}	Gate–Source Charge			6		nC
Q_{gd}	Gate–Drain Charge			12		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.5 A (Note 2)		–0.56	–1.2	V

Notes:

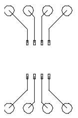
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 70°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 125°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

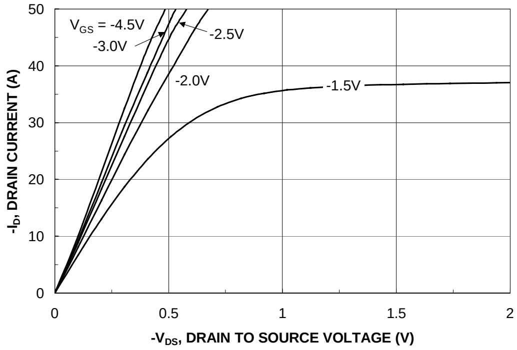


Figure 1. On-Region Characteristics.

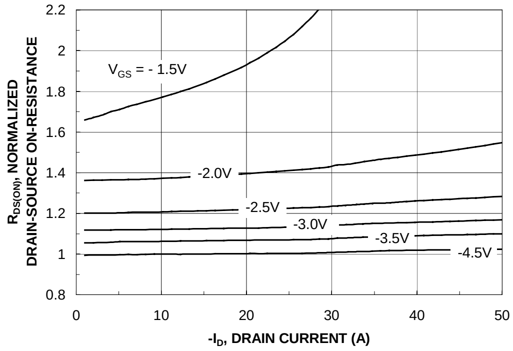


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

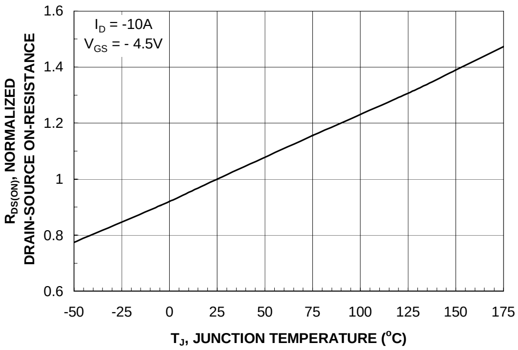


Figure 3. On-Resistance Variation with Temperature.

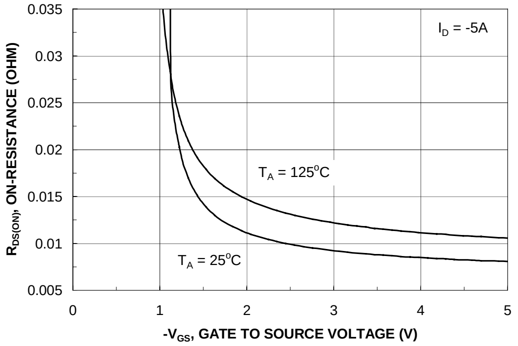


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

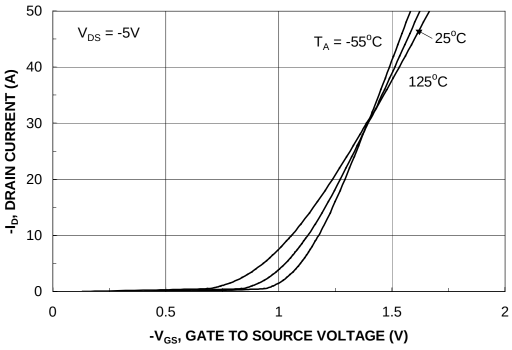


Figure 5. Transfer Characteristics.

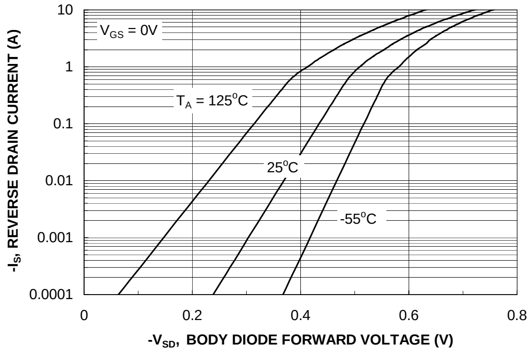


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

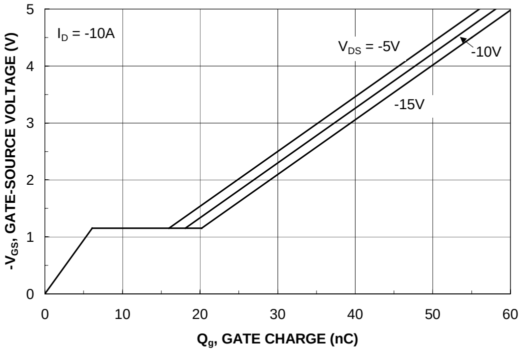


Figure 7. Gate Charge Characteristics.

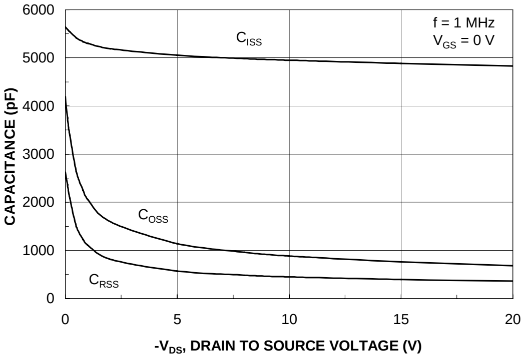


Figure 8. Capacitance Characteristics.

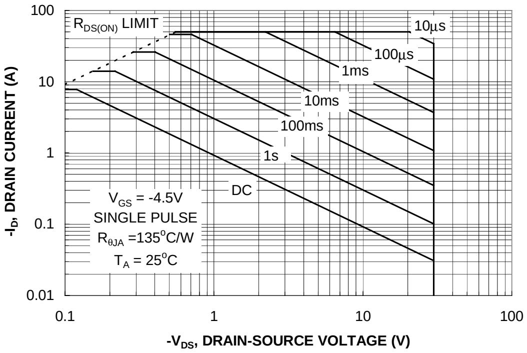


Figure 9. Maximum Safe Operating Area.

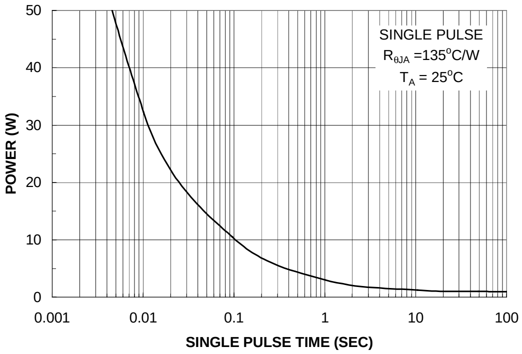


Figure 10. Single Pulse Maximum Power Dissipation.

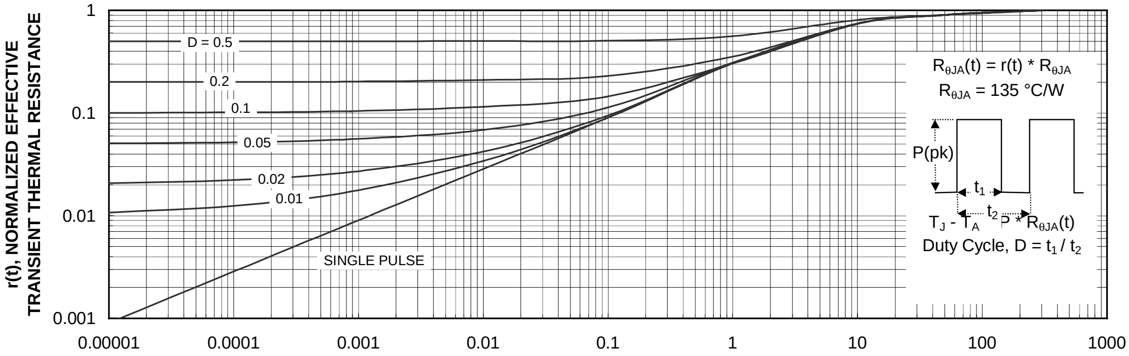


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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Michele Dickstein
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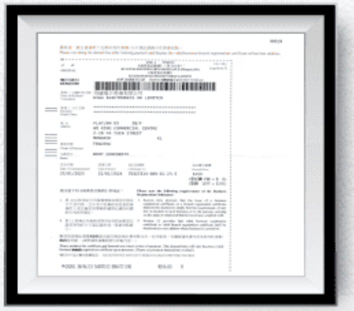

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