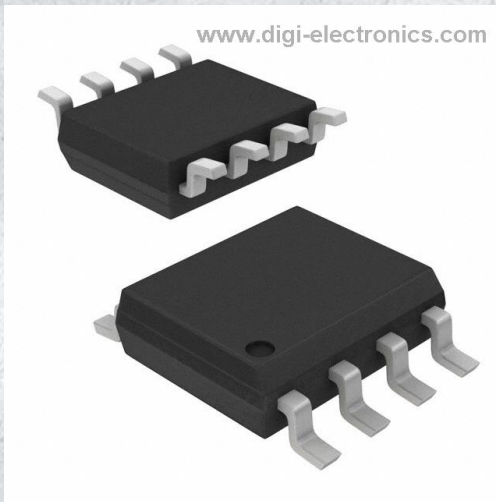


FDS4897AC Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	FDS4897AC-DG
Manufacturer	onsemi
Manufacturer Product Number	FDS4897AC
Description	MOSFET N/P-CH 40V 6.1A 8SOIC
Detailed Description	Mosfet Array 40V 6.1A, 5.2A 900mW Surface Mount 8-SOIC



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

FDS4897AC

Series:

PowerTrench®

Technology:

MOSFET (Metal Oxide)

FET Feature:

Logic Level Gate

Current - Continuous Drain (Id) @ 25°C:

6.1A, 5.2A

Vgs(th) (Max) @ Id:

3V @ 250µA

Input Capacitance (Ciss) (Max) @ Vds:

1055pF @ 20V

Operating Temperature:

-55°C ~ 150°C (Tj)

Package / Case:

8-SOIC (0.154", 3.90mm Width)

Base Product Number:

FDS4897

Manufacturer:

onsemi

Product Status:

Obsolete

Configuration:

N and P-Channel

Drain to Source Voltage (Vdss):

40V

Rds On (Max) @ Id, Vgs:

26mOhm @ 6.1A, 10V

Gate Charge (Qg) (Max) @ Vgs:

21nC @ 10V

Power - Max:

900mW

Mounting Type:

Surface Mount

Supplier Device Package:

8-SOIC

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.21.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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FDS4897AC

Dual N & P-Channel PowerTrench[®] MOSFET

N-Channel: 40 V, 6.1 A, 26 mΩ P-Channel: -40 V, -5.2 A, 39 mΩ

October 2008

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 26 mΩ at $V_{GS} = 10$ V, $I_D = 6.1$ A
- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS} = 4.5$ V, $I_D = 5.6$ A

Q2: P-Channel

- Max $r_{DS(on)}$ = 39 mΩ at $V_{GS} = -10$ V, $I_D = -5.2$ A
- Max $r_{DS(on)}$ = 65 mΩ at $V_{GS} = -4.5$ V, $I_D = -4.1$ A
- 100% UIL Tested
- RoHS Compliant

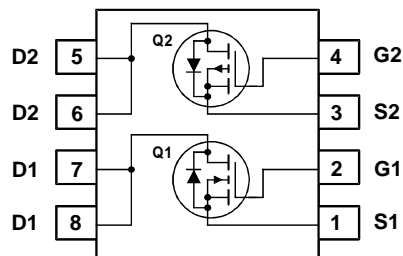
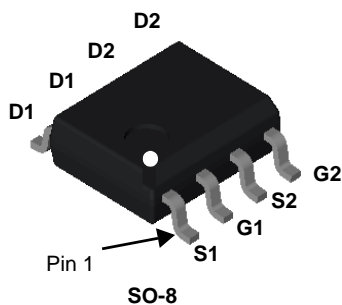


General Description

These dual N- and P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Applications

- Inverter
- Power Supplies



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	40	-40	V
V_{GS}	Gate to Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous	6.1	-5.2	A
	- Pulsed	24	-24	
P_D	Power Dissipation for Dual Operation	2.0		W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ (Note 1a)		
		$T_A = 25^\circ\text{C}$ (Note 1b)		
E_{AS}	Single Pulse Avalanche Energy (Note 3)	37	73	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, (Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, (Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4897AC	FDS4897AC	SO-8	13"	12 mm	2500 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$ $I_D = -250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	Q1 Q2	40 -40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		37 -32		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}$, $V_{GS} = 0\ \text{V}$ $V_{DS} = -32\ \text{V}$, $V_{GS} = 0\ \text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	Q1 Q2	1.5 -1.5	2.0 -2.0	3.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-6 6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 6.1\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 5.6\ \text{A}$ $V_{GS} = 10\ \text{V}$, $I_D = 6.1\ \text{A}$, $T_J = 125\text{ }^\circ\text{C}$	Q1		20 24 30	26 31 39	m Ω
		$V_{GS} = -10\ \text{V}$, $I_D = -5.2\ \text{A}$ $V_{GS} = -4.5\ \text{V}$, $I_D = -4.1\ \text{A}$ $V_{GS} = -10\ \text{V}$, $I_D = -5.2\ \text{A}$, $T_J = 125\text{ }^\circ\text{C}$	Q2		28 45 41	39 65 57	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}$, $I_D = 6.1\ \text{A}$ $V_{DD} = -5\ \text{V}$, $I_D = -5.2\ \text{A}$	Q1 Q2		24 14		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	Q1 Q2		795 765	1055 1015	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		95 135	130 180	pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	Q1 Q2		65 80	100 120	pF
R_g	Gate Resistance		Q1 Q2		1.7 3.6		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 20\ \text{V}$, $I_D = 6.1\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	Q1 Q2		6 8	12 15	ns
t_r	Rise Time		Q1 Q2		2 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -20\ \text{V}$, $I_D = -5.2\ \text{A}$, $V_{GS} = -10\ \text{V}$, $R_{GEN} = 6\ \Omega$	Q1 Q2		17 17	30 30	ns
t_f	Fall Time		Q1 Q2		2 3	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 10\ \text{V}$, $V_{DD} = 20\ \text{V}$, $I_D = 6.1\ \text{A}$	Q1 Q2		15 15	21 20	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		2.5 2.6		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = -10\ \text{V}$, $V_{DD} = -20\ \text{V}$, $I_D = -5.2\ \text{A}$	Q1 Q2		2.9 3.2		nC

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1		0.75	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q2		-0.76	-1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 6.1\text{ A}, di/dt = 100\text{ A/s}$	Q1		17	31	ns
			Q2		20	36	
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -5.2\text{ A}, di/dt = 100\text{ A/s}$	Q1		7	15	nC
			Q2		10	20	

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 135 °C/W when mounted on a minimum pad

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3: Starting $T_J = 25\text{ }^\circ\text{C}$, N-ch: L = 3 mH, $I_{AS} = 5\text{ A}$, $V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$; P-ch: L = 3 mH, $I_{AS} = -7\text{ A}$, $V_{DD} = -40\text{ V}$, $V_{GS} = -10\text{ V}$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

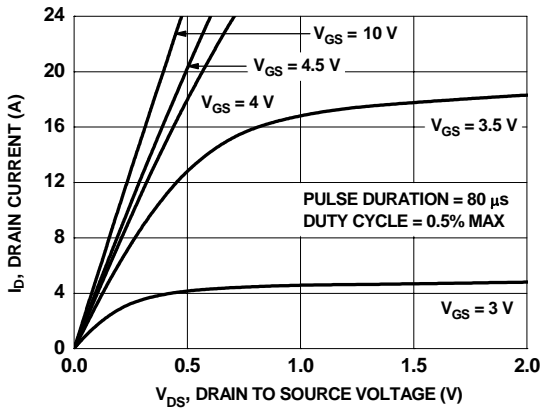


Figure 1. On Region Characteristics

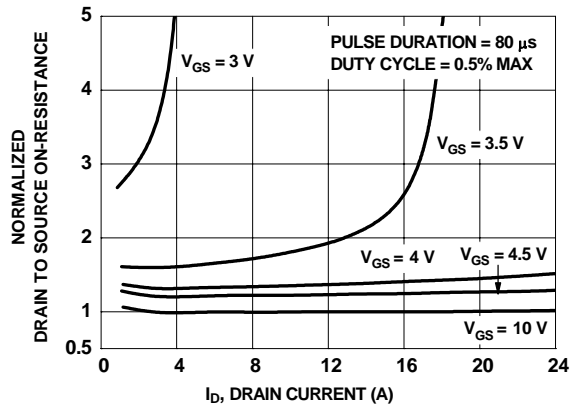


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

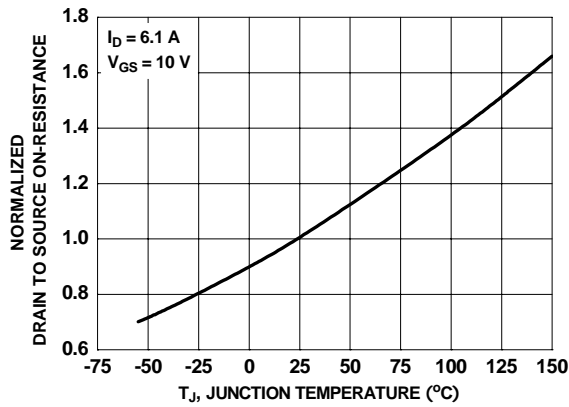


Figure 3. Normalized On Resistance vs Junction Temperature

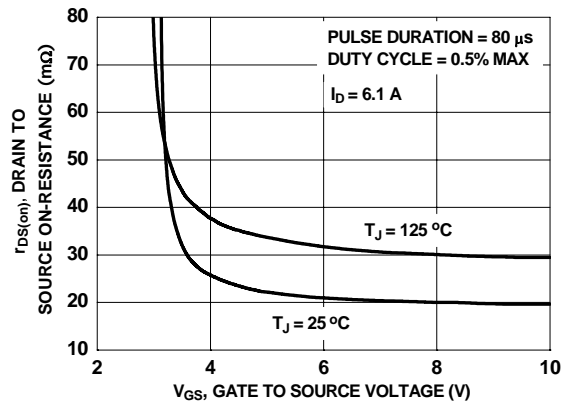


Figure 4. On-Resistance vs Gate to Source Voltage

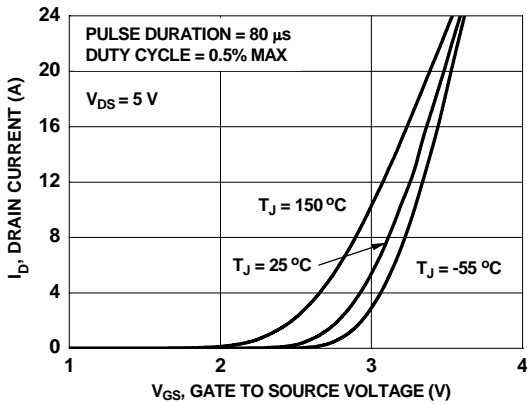


Figure 5. Transfer Characteristics

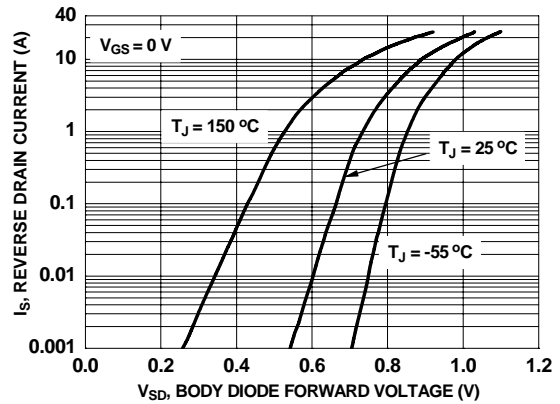


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

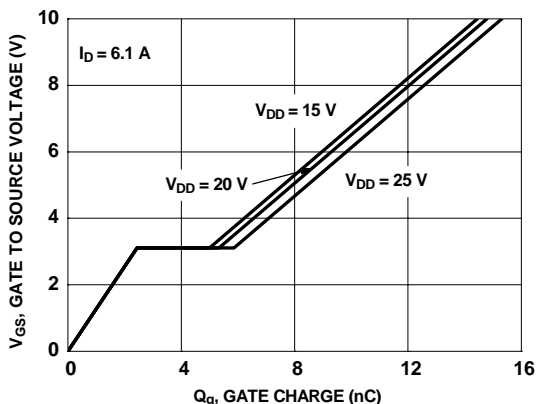


Figure 7. Gate Charge Characteristics

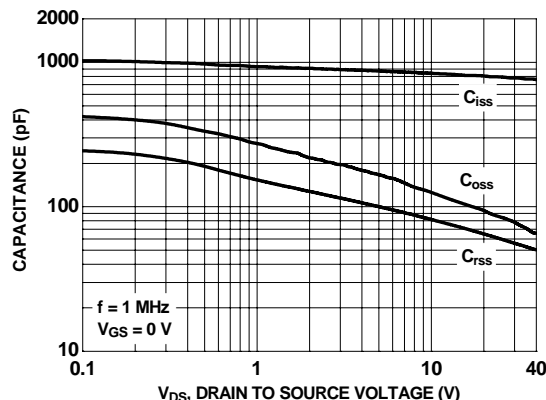


Figure 8. Capacitance vs Drain to Source Voltage

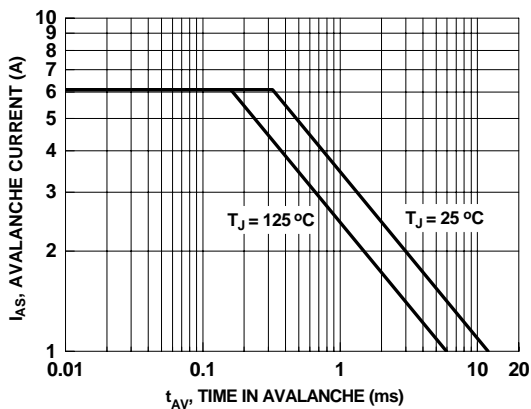


Figure 9. Unclamped Inductive Switching Capability

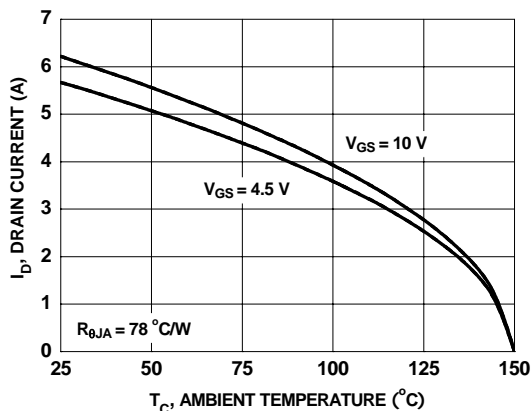


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

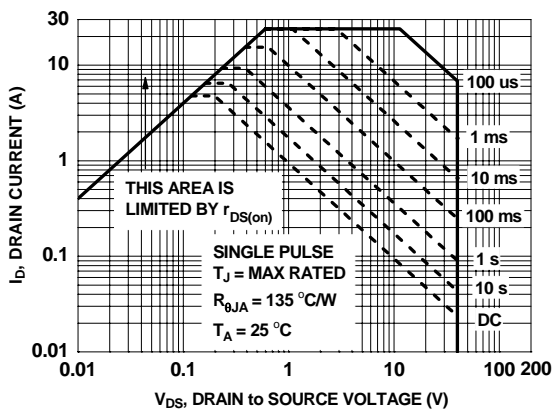


Figure 11. Forward Bias Safe Operating Area

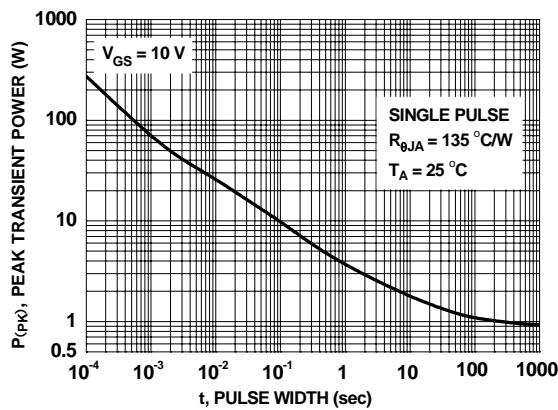


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

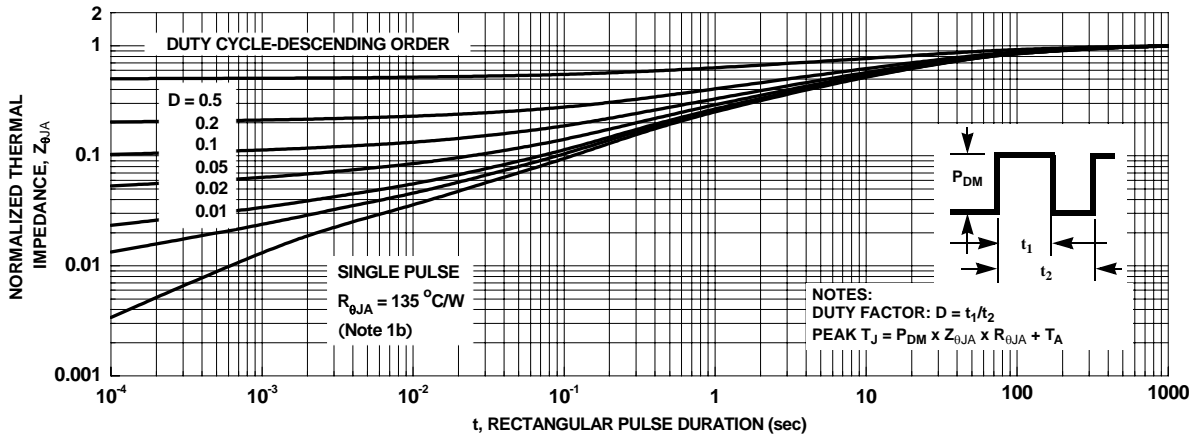


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

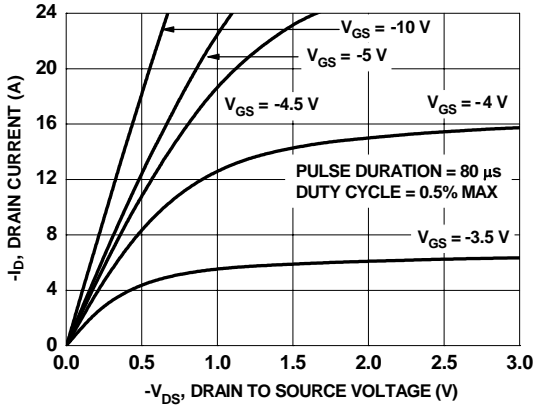


Figure 15. On-Region Characteristics

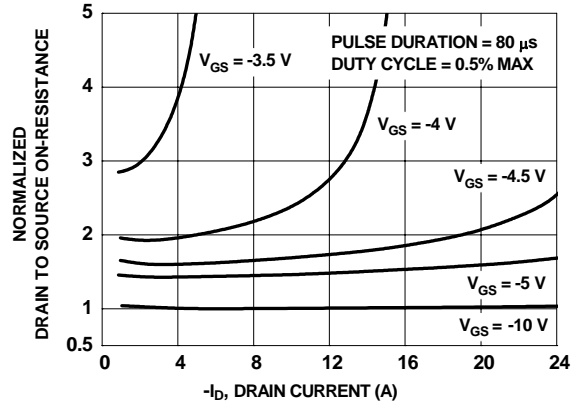


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

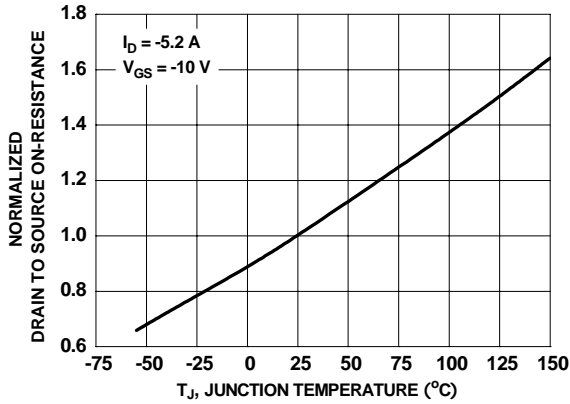


Figure 17. Normalized On-Resistance vs Junction Temperature

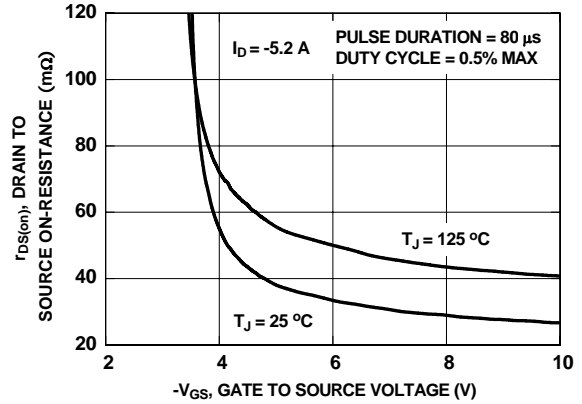


Figure 18. On-Resistance vs Gate to Source Voltage

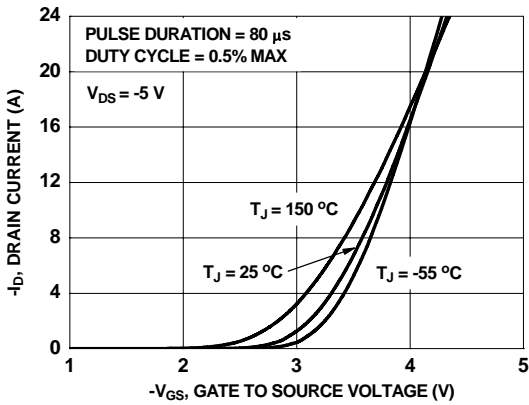


Figure 19. Transfer Characteristics

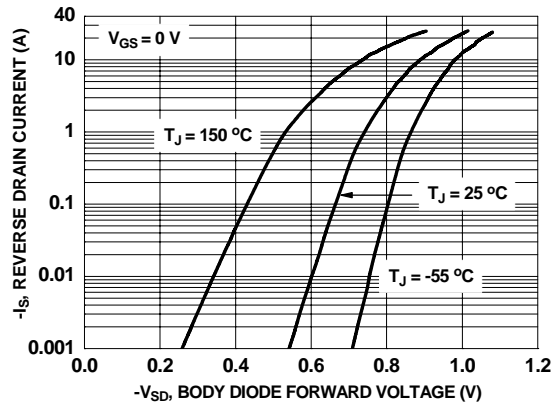


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

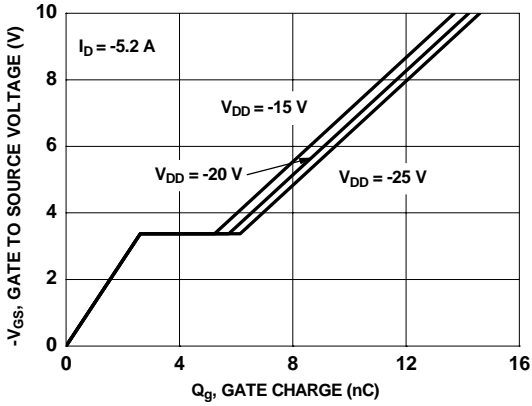


Figure 21. Gate Charge Characteristics

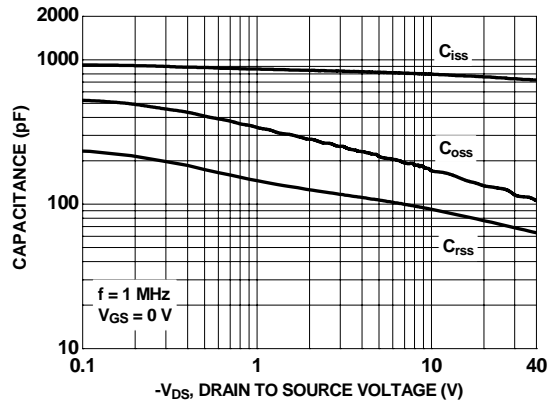


Figure 22. Capacitance vs Drain to Source Voltage

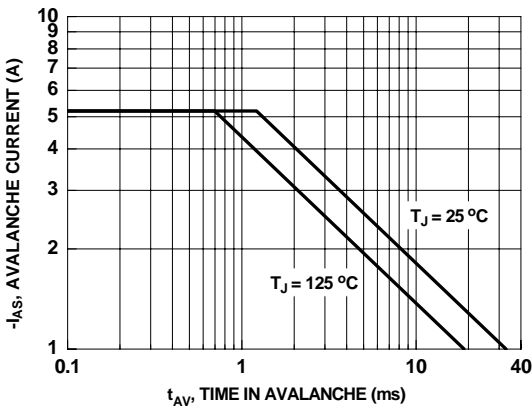


Figure 23. Unclamped Inductive Switching Capability

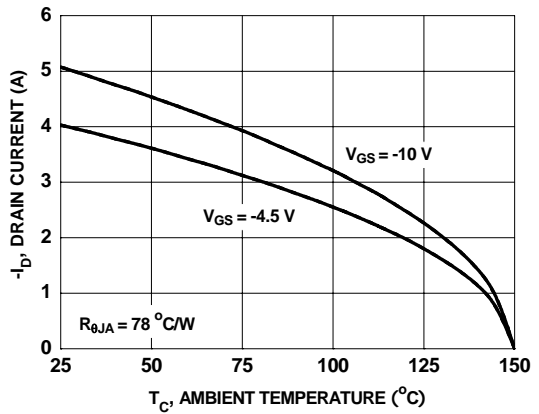


Figure 24. Maximum Continuous Drain Current vs Ambient Temperature

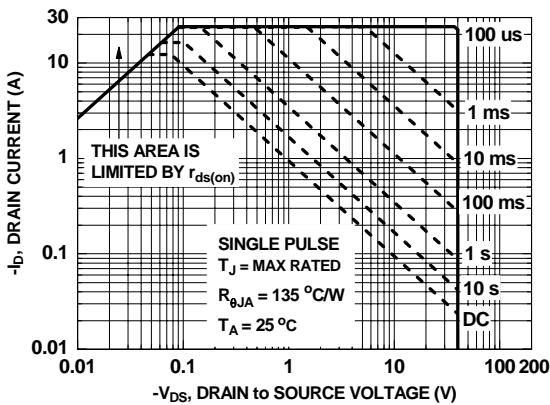


Figure 25. Forward Bias Safe Operating Area

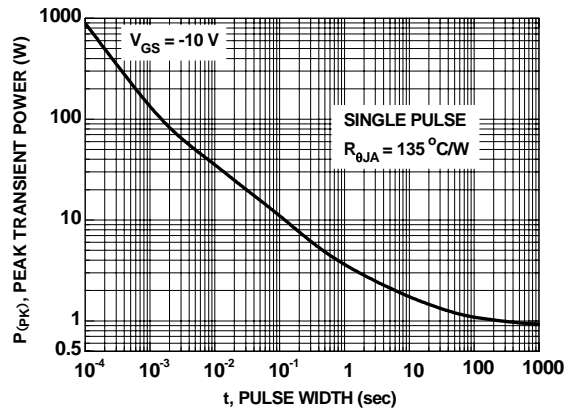


Figure 26. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

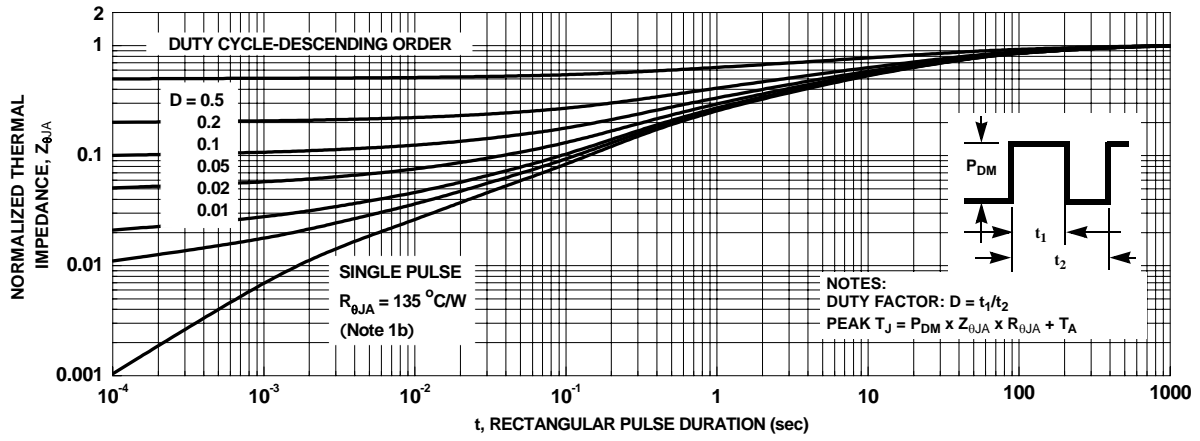


Figure 27. Junction-to-Ambient Transient Thermal Response Curve



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Definition of Terms

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