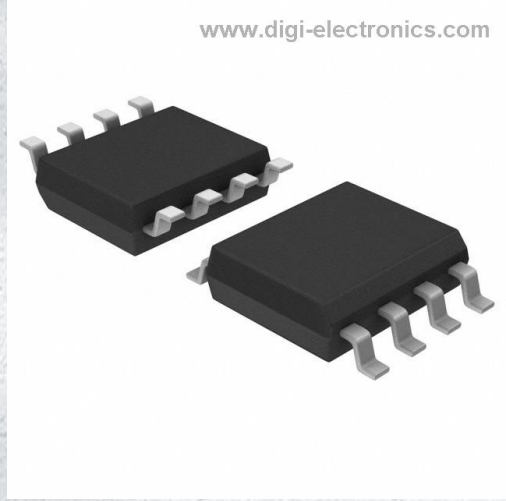
FDS7288N3 Datasheet



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DiGi Electronics Part Number	FDS7288N3-DG
Manufacturer	onsemi
Manufacturer Product Number	FDS7288N3
Description	MOSFET N-CH 30V 20A 8SO
Detailed Description	N-Channel 30 V 20A (Ta) 3W (Ta) Surface Mount 8-SO FLMP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDS7288N3	onsemi
Series:	Product Status:
PowerTrench®	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
30 V	20A (Ta)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	4.5mOhm @ 20.5A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
3V @ 250µA	69 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	3300 pF @ 15 V
FET Feature:	Power Dissipation (Max):
-	3W (Ta)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-SO FLMP	8-SOIC (0.154", 3.90mm Width) Exposed Pad
Base Product Number:	
FDS72	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

FAIRCHILD SEMICONDUCTOR®

February 2004

FDS7288N3

30V N-Channel PowerTrench® MOSFET

General Description

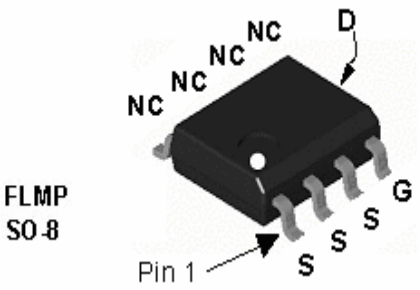
This N-Channel MOSFET in the thermally enhanced SO8 FLMP package has been designed specifically to improve the overall efficiency of DC/DC converters. Providing a balance of low $R_{DS(ON)}$ and Qg it is ideal for synchronous rectifier applications in both isolated and non-isolated topologies. It is also well suited for both high and low side switch applications in Point of Load converters.

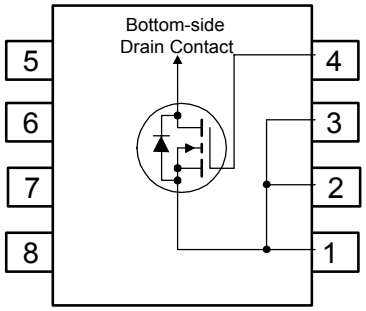
Applications

- Secondary side Synchronous rectifier
- Synchronous Buck VRM and POL Converters

Features

- 20.5 A, 30 V $R_{DS(ON)}$ = 4.5 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 5.6 mΩ @ V_{GS} = 4.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low Qg and Rg for fast switching
- SO-8 FLMP for enhanced thermal performance in an industry-standard package outline.





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	20	A
	– Pulsed		60	
P_D	Power Dissipation for Single Operation	(Note 1a)	3.0	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	0.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7288N3	FDS7288N3	13”	12mm	2500 units

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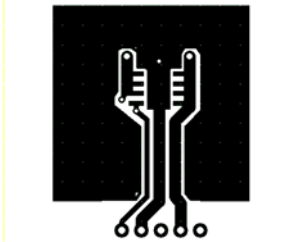
Electrical Characteristics

T_A = 25°C unless otherwise noted

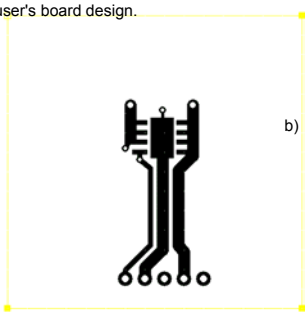
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 20 V, V_{DS} = 0 V			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 20.5 A V_{GS} = 4.5 V, I_D = 18.5 A V_{GS} = 10 V, I_D = 20.5 A, T_J = 125°C		3.8 4.6 5.2	4.5 5.6 7.6	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 20.5 A		106		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		3300		pF
C_{oss}	Output Capacitance			845		pF
C_{rss}	Reverse Transfer Capacitance			230		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.6		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			45	72	ns
t_f	Turn–Off Fall Time			32	51	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 20.5 A, V_{GS} = 10 V		49	69	nC
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 20.5 A, V_{GS} = 5 V		26	36	nC
Q_{gs}	Gate–Source Charge			8.8		nC
Q_{gd}	Gate–Drain Charge			6.7		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.70	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 20.5 A, d_{iF}/d_t = 100 A/μs		36		nS
Q_{rr}	Diode Reverse Recovery Charge			25		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a $1in^2$ pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics

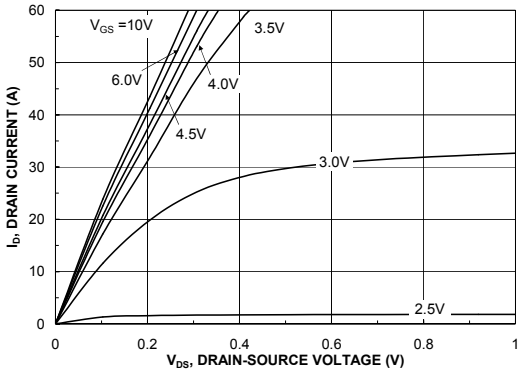


Figure 1. On-Region Characteristics.

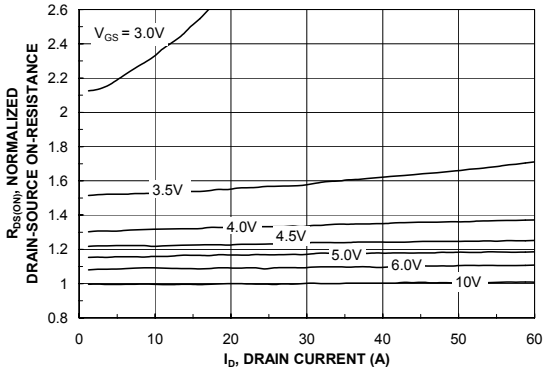


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

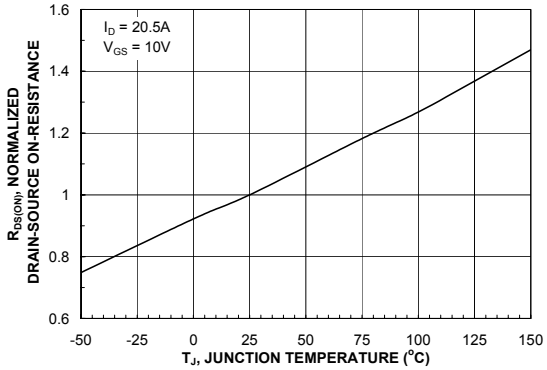


Figure 3. On-Resistance Variation withTemperature.

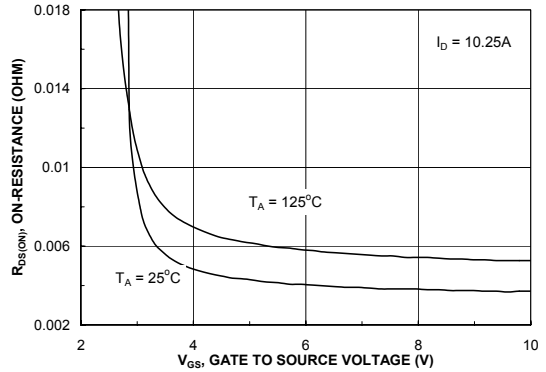


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

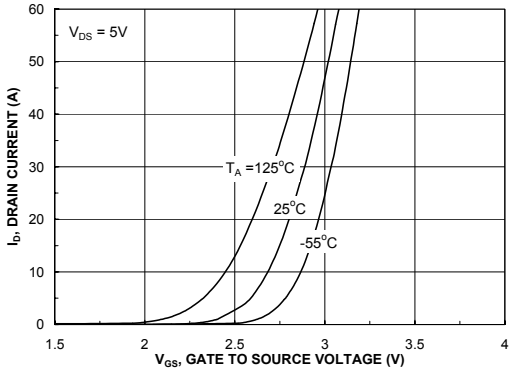


Figure 5. Transfer Characteristics.

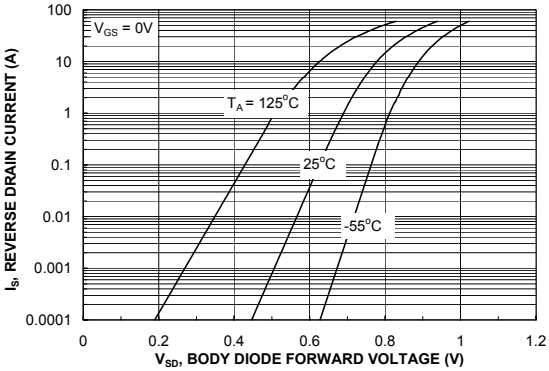


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

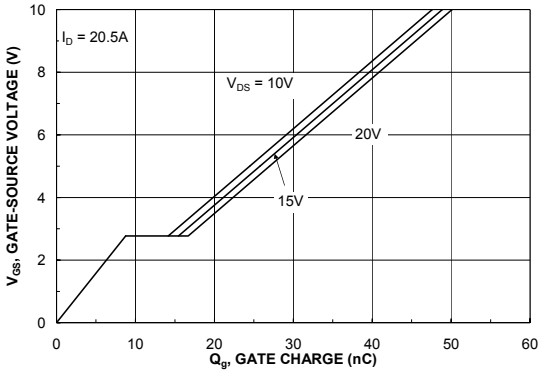


Figure 7. Gate Charge Characteristics.

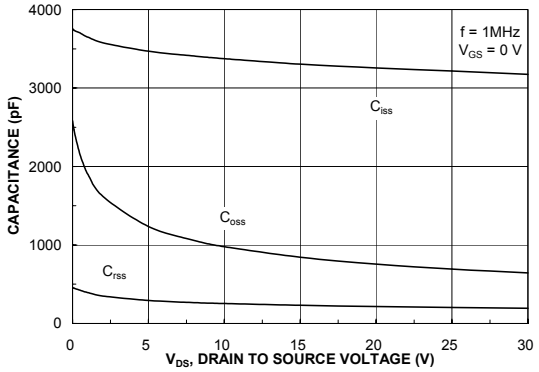


Figure 8. Capacitance Characteristics.

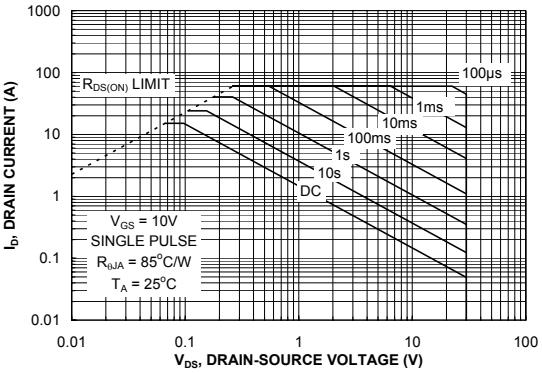


Figure 9. Maximum Safe Operating Area.

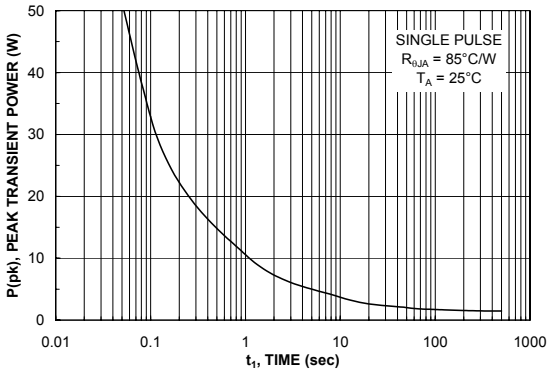


Figure 10. Single Pulse Maximum Power Dissipation.

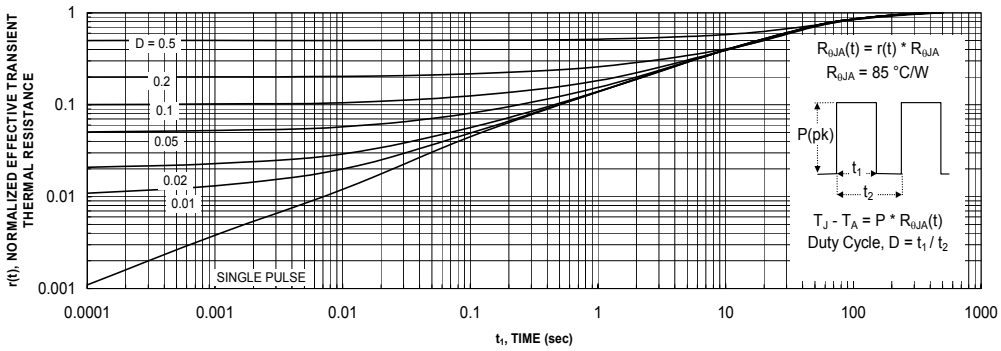
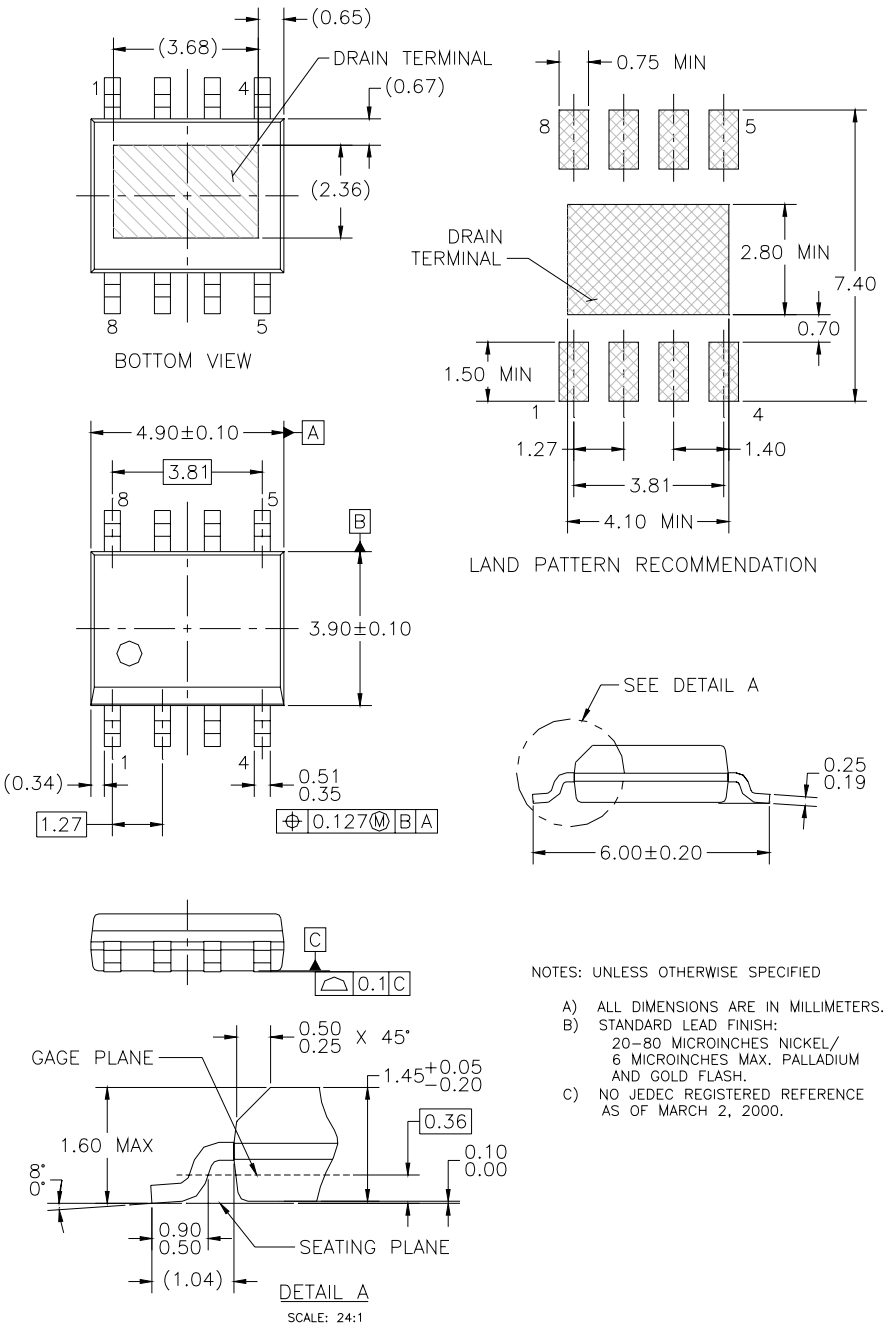


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) STANDARD LEAD FINISH:
20–80 MICROINCHES NICKEL/
6 MICROINCHES MAX. PALLADIUM
AND GOLD FLASH.
C) NO JEDEC REGISTERED REFERENCE
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CROSSVOLT™	FRFET™	MicroPak™	QFET®	SuperSOT™-8
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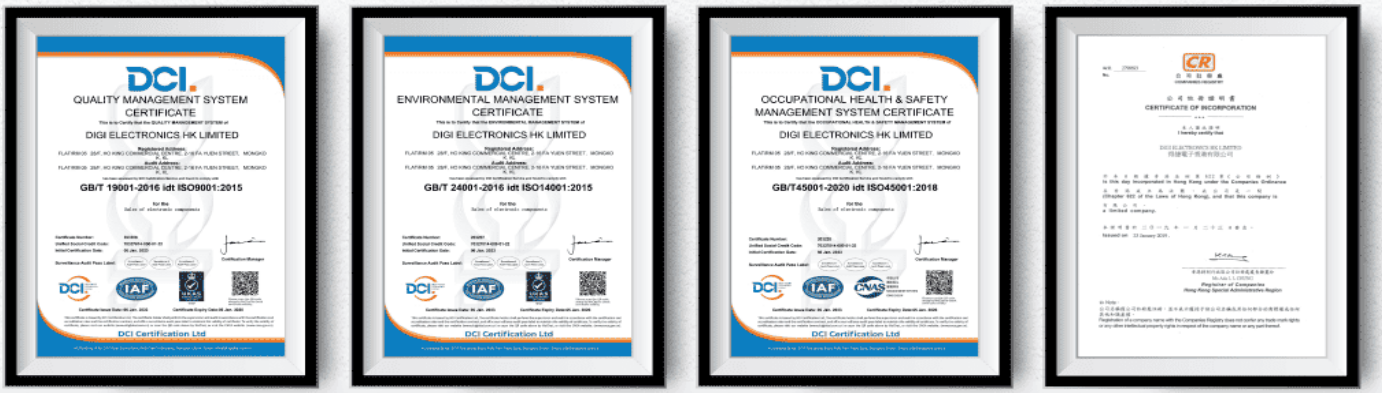

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