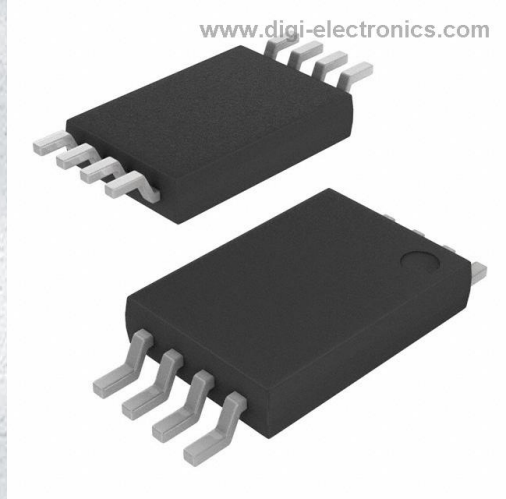
FDW2507N Datasheet



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DiGi Electronics Part Number	FDW2507N-DG
Manufacturer	onsemi
Manufacturer Product Number	FDW2507N
Description	MOSFET 2N-CH 20V 7.5A 8TSSOP
Detailed Description	Mosfet Array 20V 7.5A 1.1W Surface Mount 8-TSSOP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FDW2507N	onsemi
Series:	Product Status:
PowerTrench®	Obsolete
Technology:	Configuration:
MOSFET (Metal Oxide)	2 N-Channel (Dual)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	20V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
7.5A	19mOhm @ 7.5A, 4.5V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
1.5V @ 250µA	28nC @ 4.5V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
2152pF @ 10V	1.1W
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
8-TSSOP (0.173", 4.40mm Width)	8-TSSOP
Base Product Number:	
FDW25	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

July 2008

FDW2507N

Common Drain N-Channel 2.5V specified PowerTrench® MOSFET

General Description

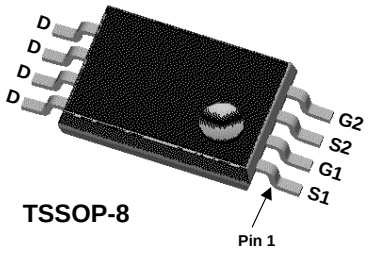
This monolithic common drain N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench process to optimize the $R_{DS(ON)}$ @ V_{GS} = 2.5v on special TSSOP-8 lead frame with all the drains on one side of the package.

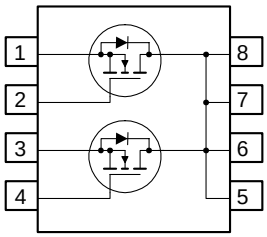
Applications

- Li-Ion Battery Pack

Features

- 7.5 A, 20 V. $R_{DS(ON)}$ = 19 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 23 mΩ @ V_{GS} = 2.5 V
- Isolated source and drain pins
- High performance trench technology for extremely low $R_{DS(ON)}$ @ V_{GS} = 2.5 V
- Low profile TSSOP-8 package





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous	(Note 1a)	7.5	A
	– Pulsed		30	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	77	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	114	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2507N	FDW2507N	13''	12mm	2500 units

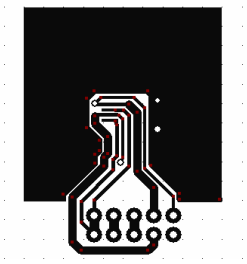
Electrical Characteristics

T_A = 25°C unless otherwise noted

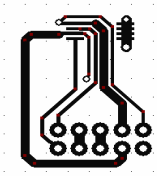
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.6	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 7.5 A V_{GS} = 2.5 V, I_D = 6.8 A V_{GS} = 4.5 V, I_D = 7.5 A, T_J=125°C		15 17 20	19 23 27	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	30			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7.5 A		31		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		2152		pF
C_{oss}	Output Capacitance			512		pF
C_{rss}	Reverse Transfer Capacitance			263		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
t_f	Turn–Off Fall Time			19	34	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 7.5 A, V_{GS} = 4.5 V		20	28	nC
Q_{gs}	Gate–Source Charge			3		nC
Q_{gd}	Gate–Drain Charge			5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.6	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 7.5A, d_{iF}/d_t = 100 A/µs (Note 2)		26		nS
Q_{rr}	Diode Reverse Recovery Charge			21		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 77°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 114°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

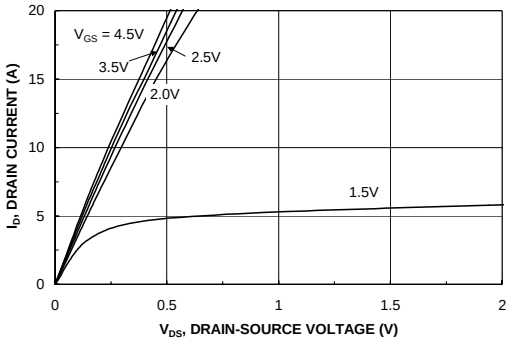


Figure 1. On-Region Characteristics.

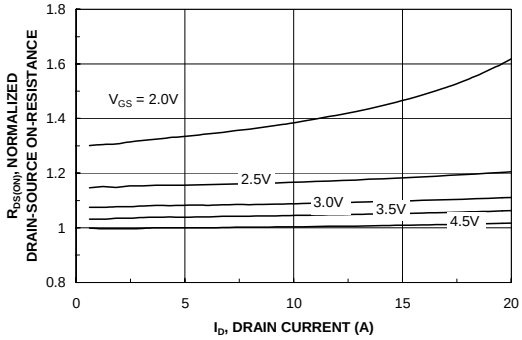


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

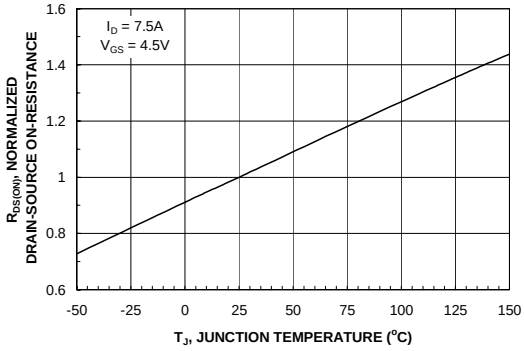


Figure 3. On-Resistance Variation with Temperature.

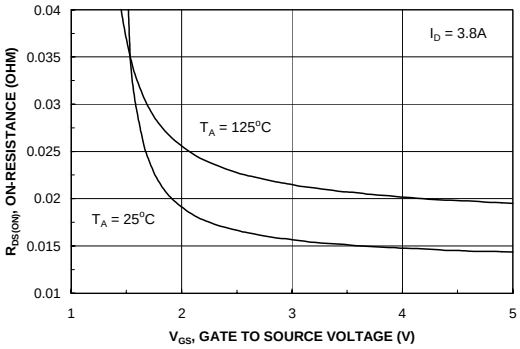


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

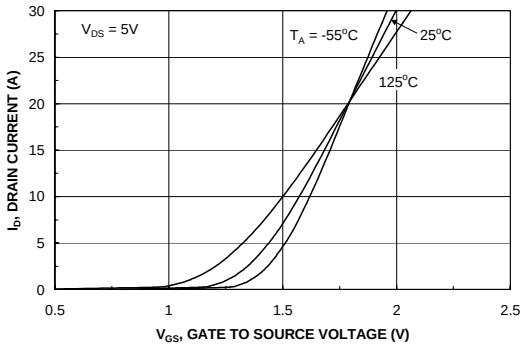


Figure 5. Transfer Characteristics.

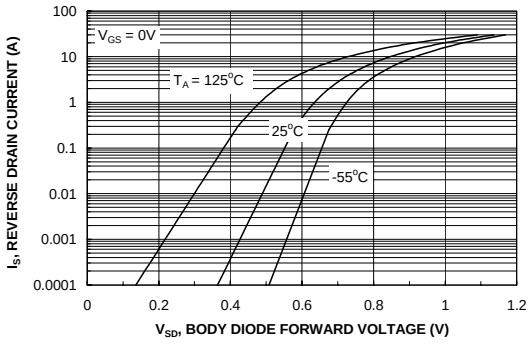


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

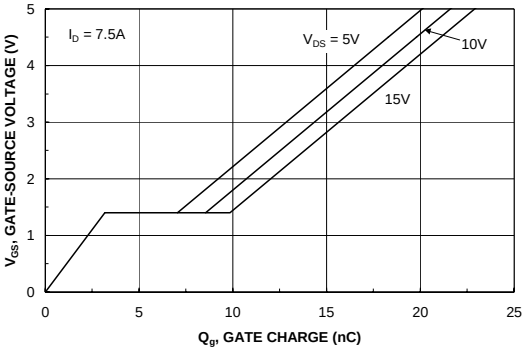


Figure 7. Gate Charge Characteristics.

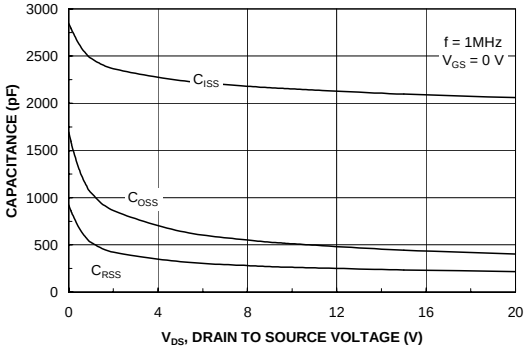


Figure 8. Capacitance Characteristics.

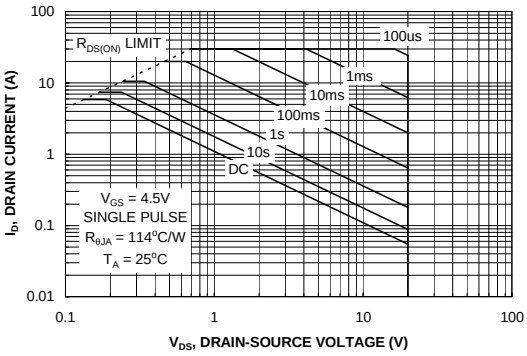


Figure 9. Maximum Safe Operating Area.

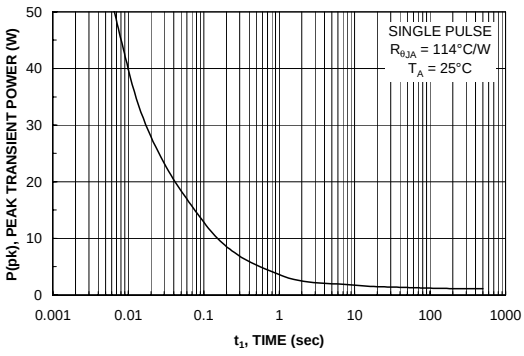


Figure 10. Single Pulse Maximum Power Dissipation.

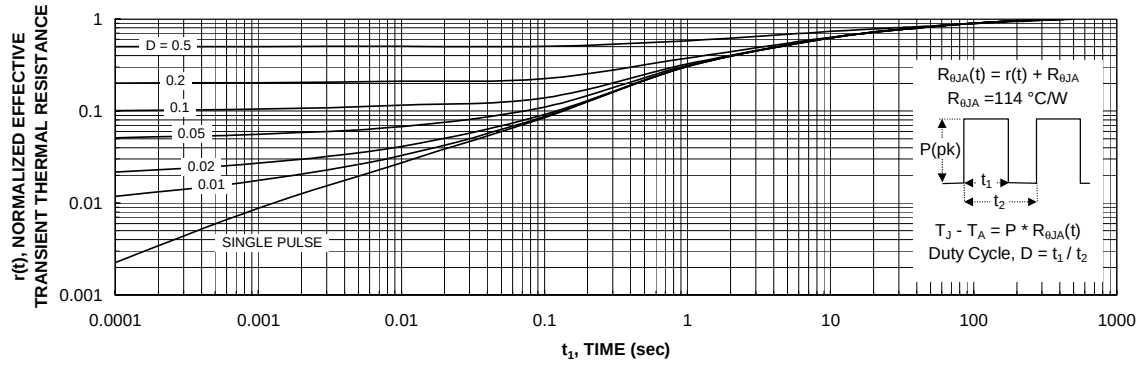


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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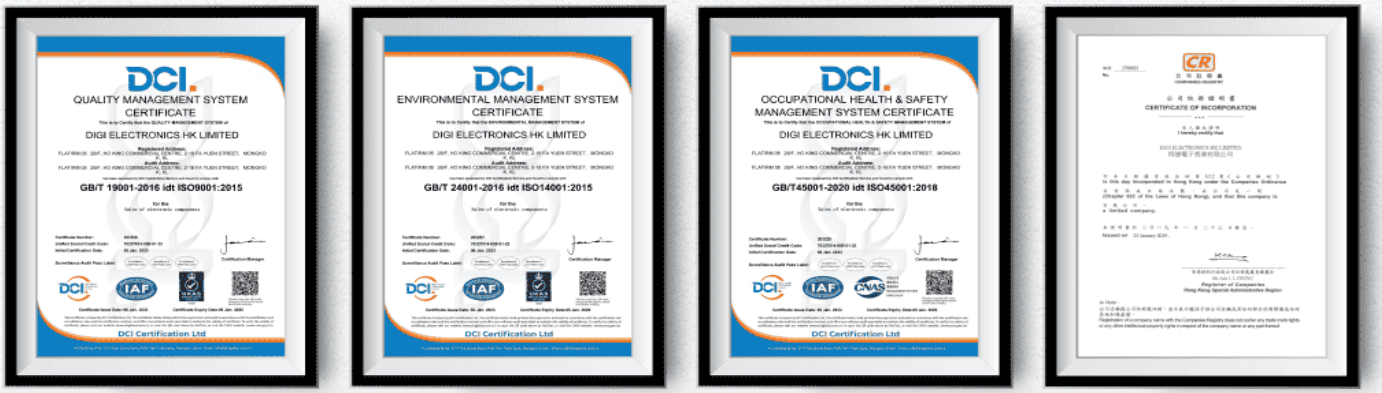

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