FQD1N60TF Datasheet

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DiGi Electronics Part Number	FQD1N60TF-DG
Manufacturer	onsemi
Manufacturer Product Number	FQD1N60TF
Description	MOSFET N-CH 600V 1A DPAK
Detailed Description	N-Channel 600 V 1A (Tc) 2.5W (Ta), 30W (Tc) Surface Mount TO-252AA

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FQD1N60TF	onsemi
Series:	Product Status:
QFET®	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
600 V	1A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	11.5Ohm @ 500mA, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
5V @ 250µA	6 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±30V	150 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	2.5W (Ta), 30W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
TO-252AA	TO-252-3, DPAK (2 Leads + Tab), SC-63
Base Product Number:	
FQD1	

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

FAIRCHILD SEMICONDUCTOR™

April 2000

QFET™

FQD1N60 / FQU1N60

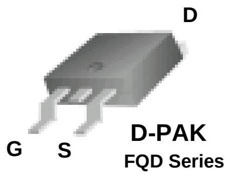
600V N-Channel MOSFET

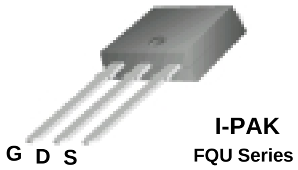
General Description

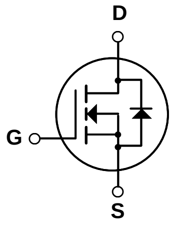
These N-Channel enhancement mode power field effect transistors are produced using Fairchild’s proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

Features

- 1.0A, 600V, $R_{DS(on)} = 11.5\Omega$ @$V_{GS} = 10$ V
- Low gate charge (typical 5.0 nC)
- Low Crss (typical 3.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability







Absolute Maximum Ratings

$T_C = 25°C$ unless otherwise noted

Symbol	Parameter		FQD1N60 / FQU1N60	Units
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous ($T_C = 25°C$)		1.0	A
	- Continuous ($T_C = 100°C$)		0.63	A
I_{DM}	Drain Current - Pulsed	(Note 1)	4.0	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	50	mJ
I_{AR}	Avalanche Current	(Note 1)	1.0	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25°C$) *		2.5	W
	Power Dissipation ($T_C = 25°C$)		30	W
	- Derate above 25°C		0.24	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.17	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	600	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.4	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 480 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.5 A	--	9.3	11.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 0.5 A (Note 4)	--	0.83	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	120	150	pF
C_{oss}	Output Capacitance		--	20	25	pF
C_{rss}	Reverse Transfer Capacitance		--	3	4	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 1.2 A, R_G = 25 Ω (Note 4, 5)	--	5	20	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	7	25	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 1.2 A, V_{GS} = 10 V (Note 4, 5)	--	5	6	nC
Q_{gs}	Gate-Source Charge		--	1	--	nC
Q_{gd}	Gate-Drain Charge		--	2.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	4.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 1.2 A, dI_F / dt = 100 A/µs (Note 4)	--	160	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.3	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 92mH, I_{AS} = 1.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 1.2A, di/dt ≤ 200A/µs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

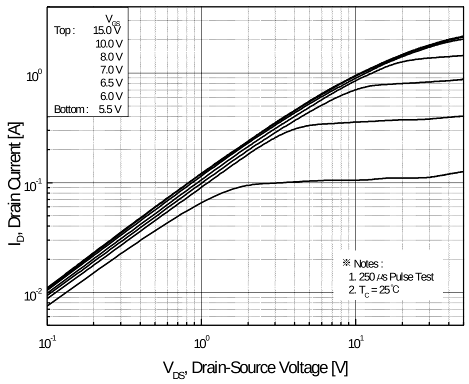


Figure 1. On-Region Characteristics

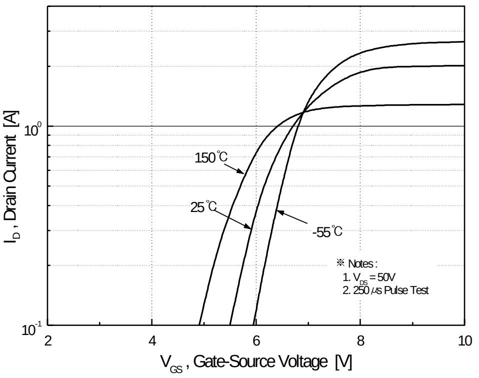


Figure 2. Transfer Characteristics

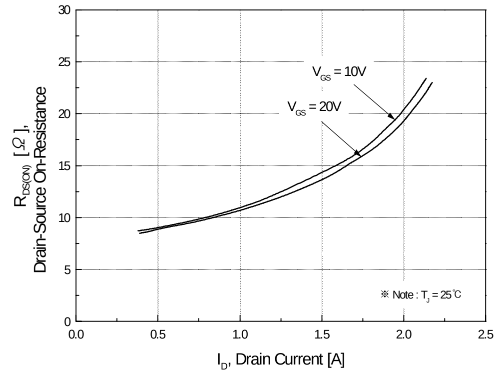


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

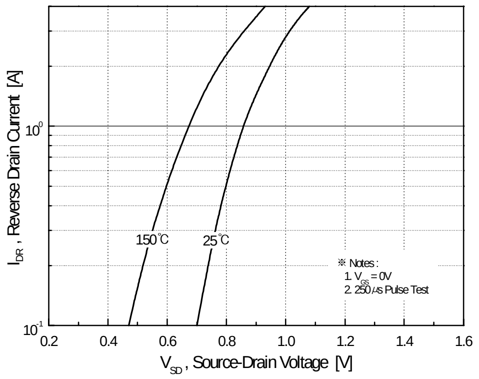


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

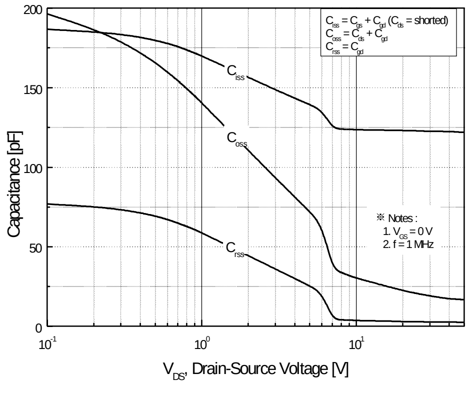


Figure 5. Capacitance Characteristics

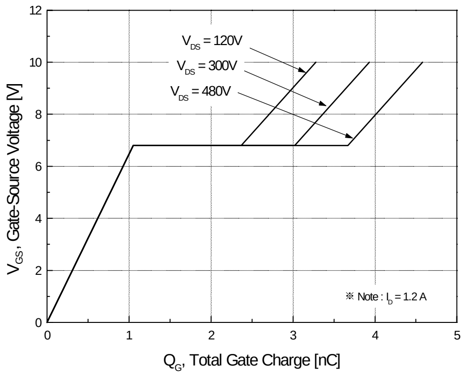


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

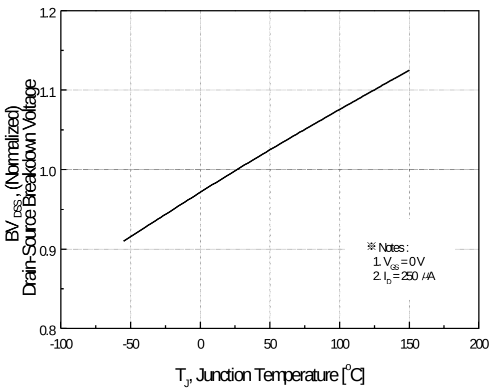


Figure 7. Breakdown Voltage Variation vs. Temperature

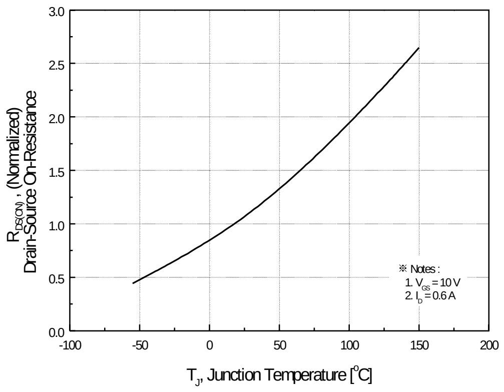


Figure 8. On-Resistance Variation vs. Temperature

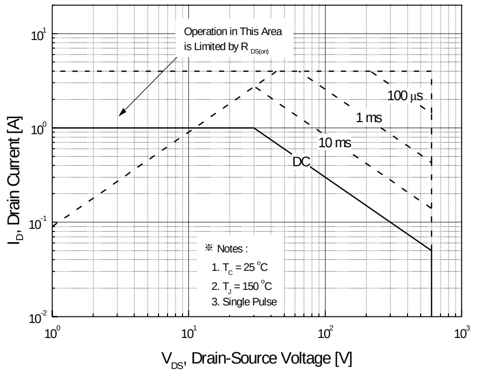


Figure 9. Maximum Safe Operating Area

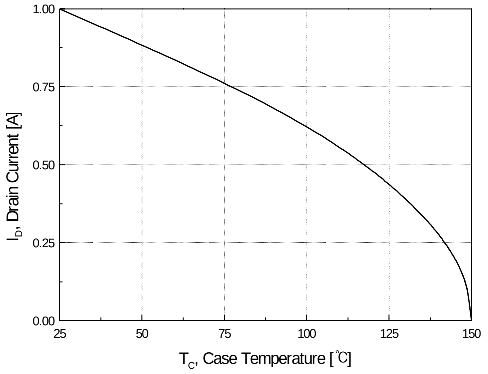


Figure 10. Maximum Drain Current vs. Case Temperature

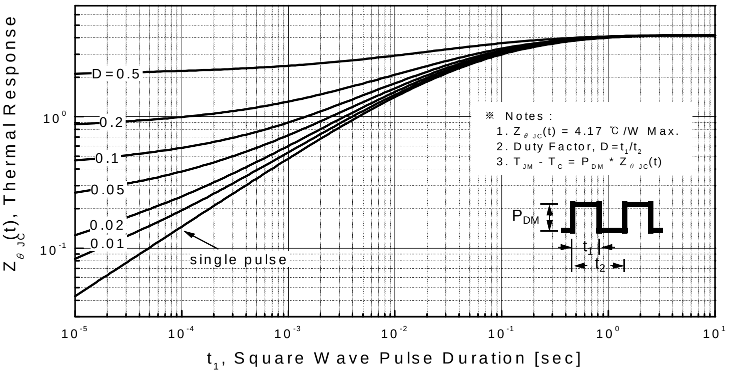
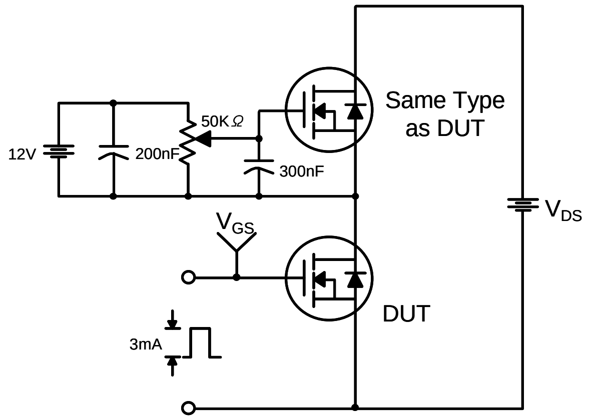
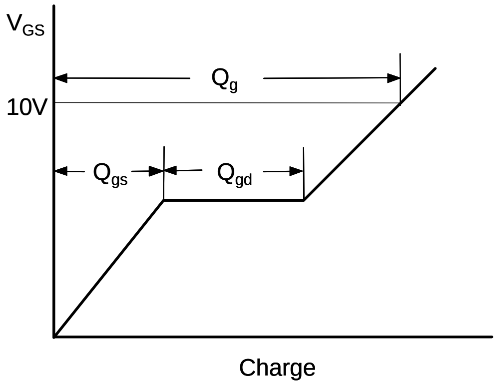


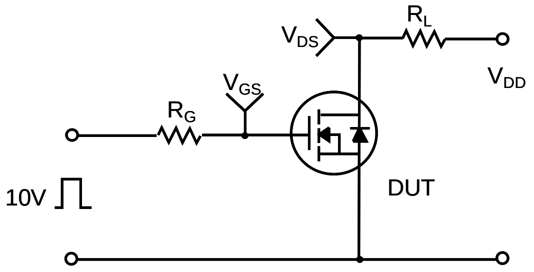
Figure 11. Transient Thermal Response Curve

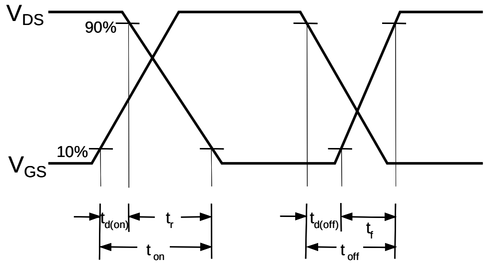
Gate Charge Test Circuit & Waveform



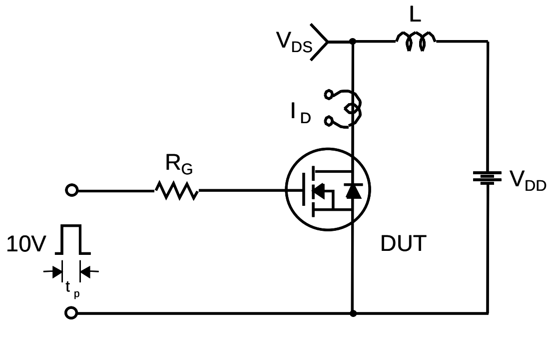


Resistive Switching Test Circuit & Waveforms

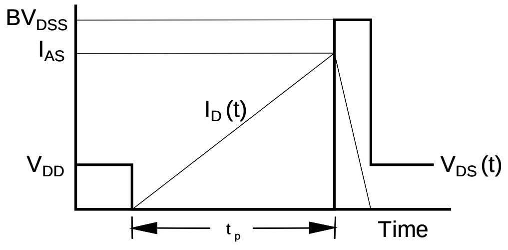




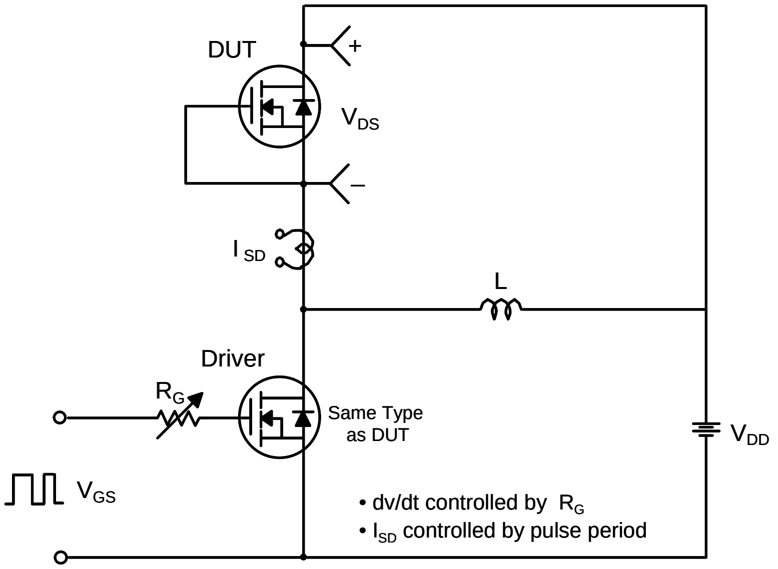
Unclamped Inductive Switching Test Circuit & Waveforms



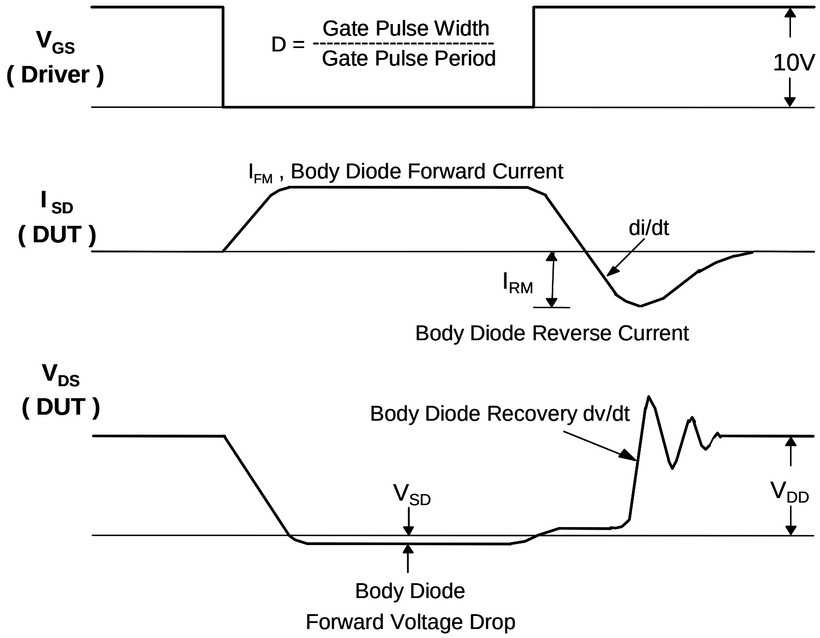
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms

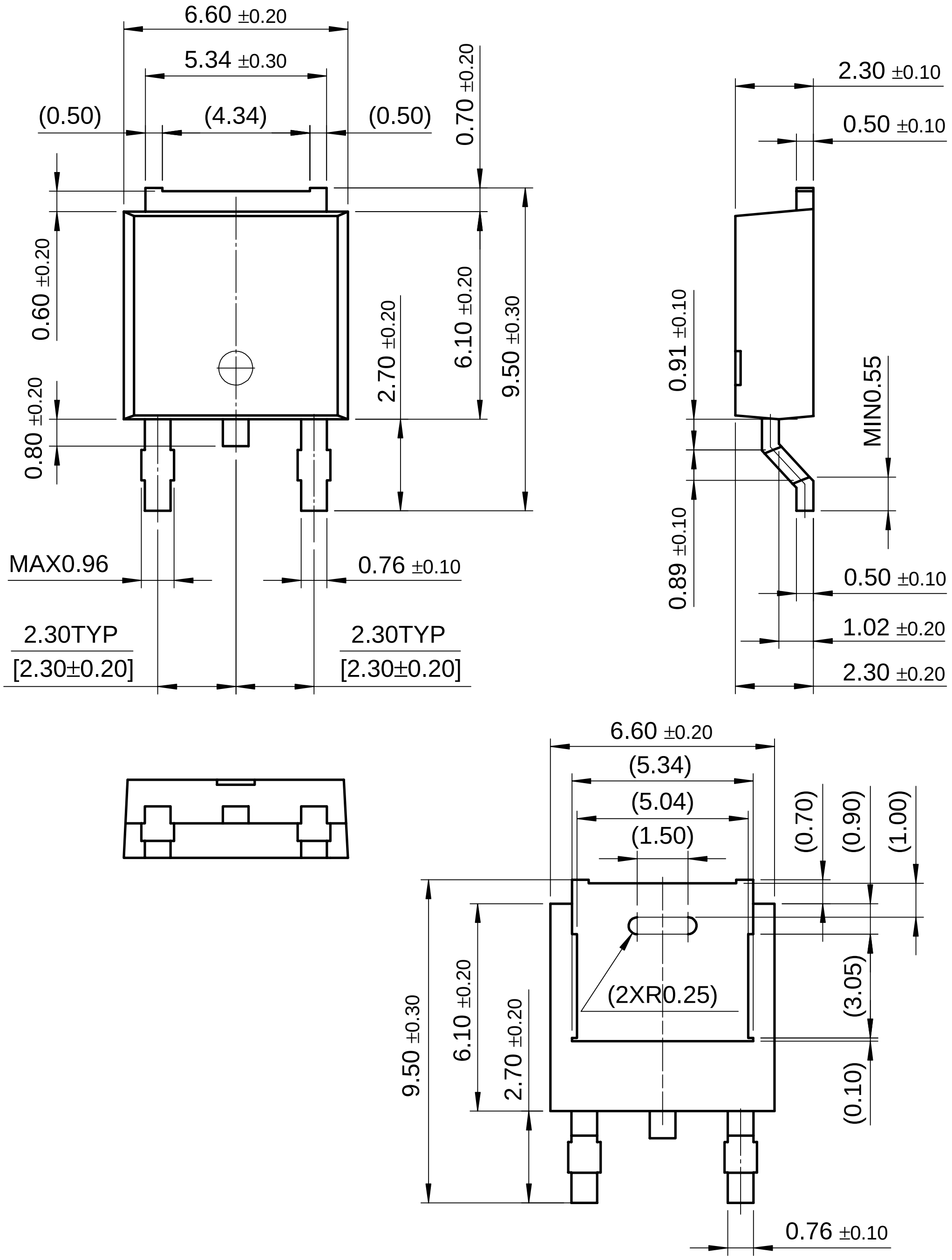


- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



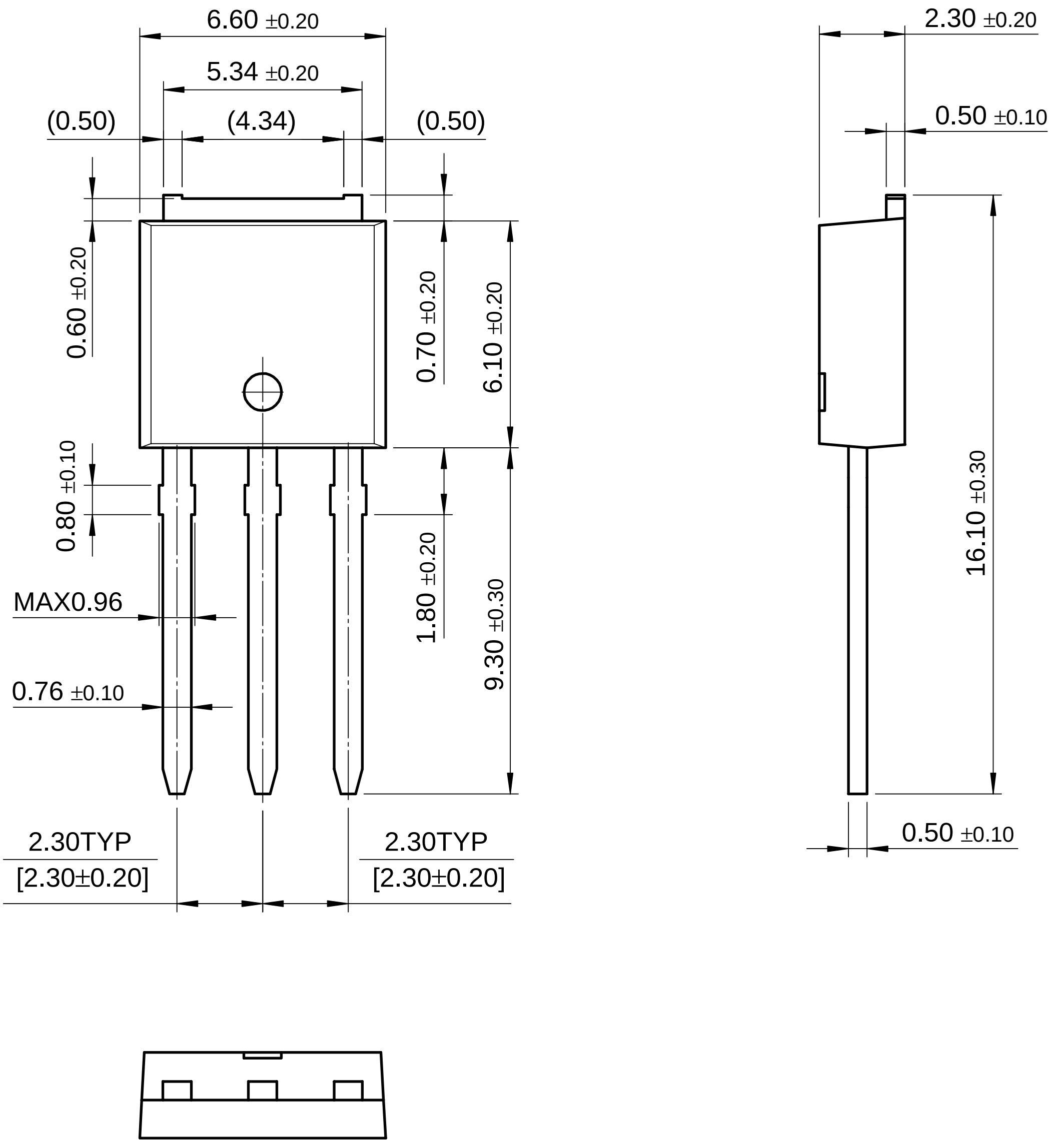
Package Dimensions

DPAK



Package Dimensions (Continued)

IPAK



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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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