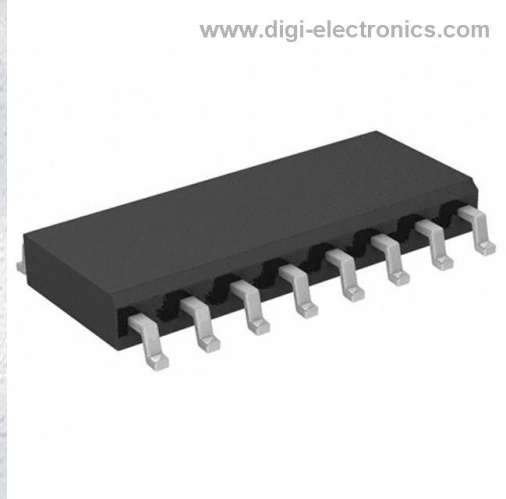
FS6131-01I-XTD Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	FS6131-01I-XTD-DG
Manufacturer	onsemi
Manufacturer Product Number	FS6131-01I-XTD
Description	IC PLL CLOCK GENERATOR 16SOIC
Detailed Description	PLL Clock Generator IC 230MHz 1 16-SOIC (0.154", 3 .90mm Width)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
FS6131-01I-XTD	onsemi
Series:	Product Status:
-	Discontinued at Digi-Key
DiGi-Electronics Programmable:	Type:
Not Verified	PLL Clock Generator
PLL:	Input:
Yes	Crystal
Output:	Number of Circuits:
CMOS, PECL	1
Ratio - Input:Output:	Differential - Input:Output:
1:1	No/Yes
Frequency - Max:	Divider/Multiplier:
230MHz	Yes/No
Voltage - Supply:	Operating Temperature:
4.5V ~ 5.5V	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
16-SOIC	FS6131

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	2 (1 Year)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

ON Semiconductor®

FS6131

Programmable Line Lock Clock Generator IC

1.0 Key Features

- Complete programmable control via I²C™-bus
- Selectable CMOS or PECL compatible outputs
- External feedback loop capability allows genlocking
- Tunable VCXO loop for jitter attenuation

2.0 General Description

The FS6131-01 is a monolithic CMOS clock generator/regenerator IC designed to minimize cost and component count in a variety of electronic systems. Via the I²C-bus interface, the FS6131-01 can be adapted to many clock generation requirements.

The ability to tune the on-board voltage-controlled crystal oscillator (VCXO), the length of the reference and feed-back dividers, their granularity, and the flexibility of the post divider make the FS6131-01 the most flexible stand-alone phase-locked loop (PLL) clock generator available.

3.0 Applications

- Frequency synthesis
- Line-locked and genlock applications
- Clock multiplication
- Telecom jitter attenuation

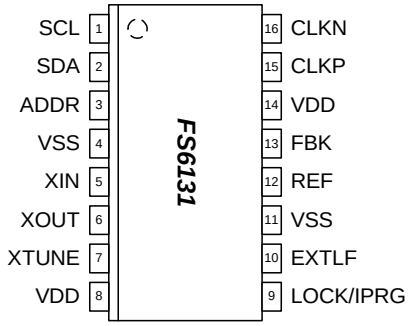


Figure 1: Pin Configuration

May 2008 – Rev. 4

Publication Order Number:
FS6131/D

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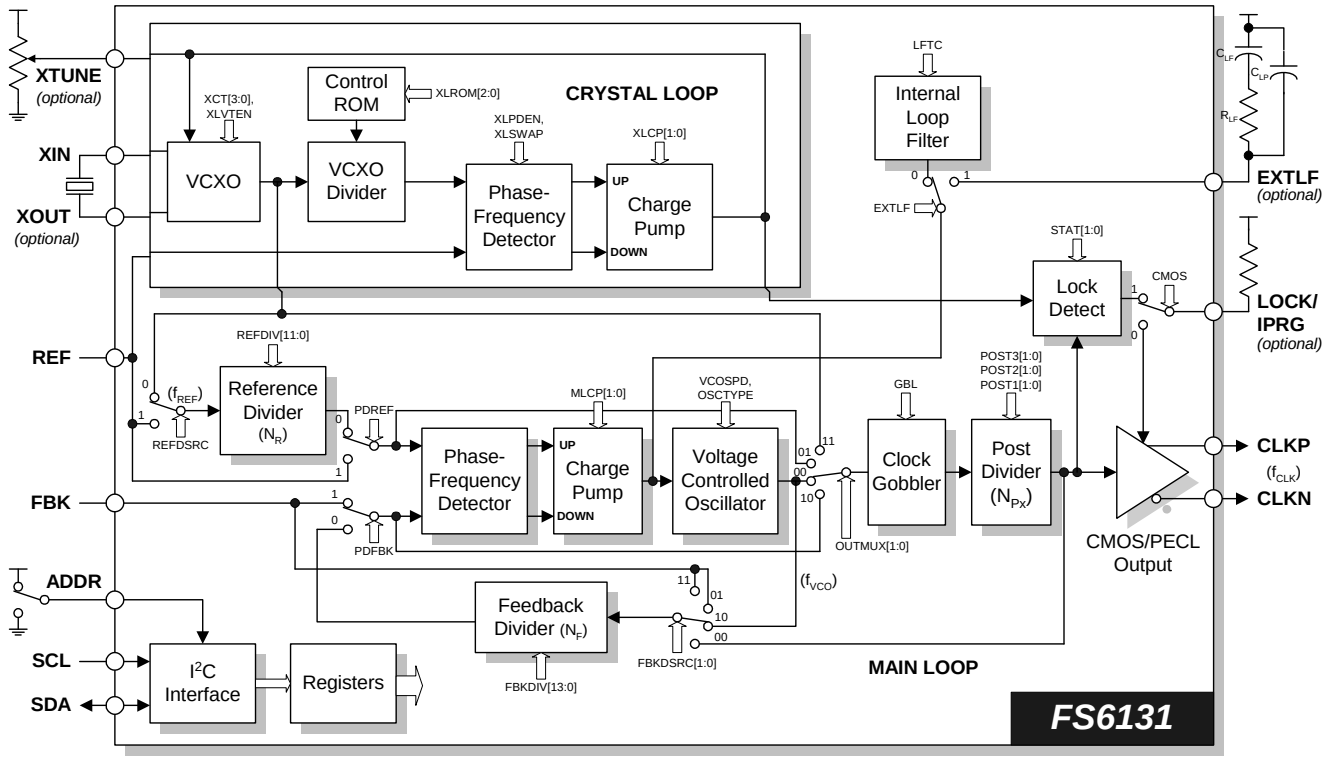

Figure 2: Block Diagram

Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

Pin	Type	Name	Description
1	DI	SCL	Serial interface clock (requires an external pull-up)
2	DIO	SDA	Serial interface data input/output (requires an external pull-up)
3	DI	ADDR	Address select bit (see Section 5.2.1)
4	P	VSS	Ground
5	AI	XIN	VCXO feedback
6	AO	XOUT	VCXO drive
7	AI	XTUNE	VCXO tune
8	P	VDD	Power supply (+5V)
9	DIO	LOCK/IPRG	Lock indicator / PECL current drive programming
10	AI	EXTLF	External loop filter
11	P	VSS	Ground
12	DI	REF	Reference frequency input
13	DI	FBK	Feedback input
14	P	VDD	Power supply (+5V)
15	DO	CLKP	Differential clock output (+)
16	DO	CLKN	Differential clock output (-)

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4.0 Functional Block Description

4.1 Main Loop PLL

The main loop phase locked loop (ML-PLL) is a standard phase- and frequency- locked loop architecture. As shown in **Error! Reference source not found.**, the ML-PLL consists of a reference divider, a phase-frequency detector (PFD), a charge pump, an internal loop filter, a voltage-controlled oscillator (VCO), a feedback divider, and a post divider.

During operation, the reference frequency (f_{REF}), generated by either the on-board crystal oscillator or an external frequency source, is first reduced by the reference divider. The integer value that the frequency is divided by is called the modulus, and is denoted as N_R for the reference divider. The divided reference is then fed into the PFD.

The PFD controls the frequency of the VCO (f_{VCO}) through the charge pump and loop filter. The VCO provides a high-speed, low noise, continuously variable frequency clock source for the ML-PLL. The output of the VCO is fed back to the PFD through the feedback divider (the modulus is denoted by N_F) to close the loop.

The PFD will drive the VCO up or down in frequency until the divided reference frequency and the divided VCO frequency appearing at the inputs of the PFD are equal. The input/output relationship between the reference frequency and the VCO frequency is

$$\frac{f_{VCO}}{N_F} = \frac{f_{REF}}{N_R}$$

If the VCO frequency is used as the PLL output frequency (f_{CLK}) then the basic PLL equation can be rewritten as

$$f_{CLK} = f_{REF}\left(\frac{N_F}{N_R}\right)$$

4.1.1. Reference Divider

The reference divider is designed for low phase jitter. The divider accepts either the output of either the crystal loop (the VCXO output) or an external reference frequency, and provides a divided-down frequency to the PFD. The reference divider is a 12-bit divider, and can be programmed for any modulus from 1 to 4095. See both Table 3 and Table 8 for additional programming information.

4.1.2. Feedback Divider

The feedback divider is based on a dual-modulus pre-scaler technique. The technique allows the same granularity as a fully programmable feedback divider, while still allowing the programmable portion to operate at low speed. A high-speed pre-divider (also called a prescaler) is placed between the VCO and the programmable feedback divider because of the high speeds at which the VCO can operate. The dual-modulus technique insures reliable operation at any speed that the VCO can achieve and reduces the overall power consumption of the divider.

For example, a fixed divide-by-eight could be used in the feedback divider. Unfortunately, a divide-by-eight would limit the effective modulus of the feedback divider path to multiples of eight. The limitation would restrict the ability of the PLL to achieve a desired input-frequency-to-output frequency ratio without making both the reference and feedback divider values comparatively large. Large divider moduli are generally undesirable due to increased phase jitter.

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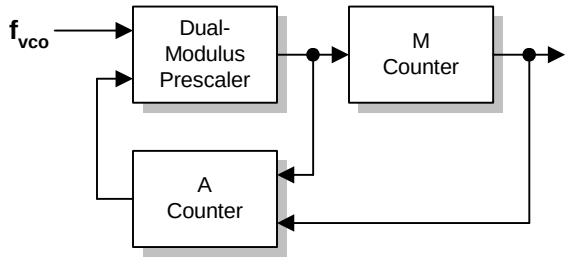

Figure 3: Feedback Divider

To understand the operation, refer to **Error! Reference source not found.**. The M-counter (with a modulus of M) is cascaded with the dual-modulus pre-scaler. If the prescaler modulus were fixed at N, the overall modulus of the feedback divider chain would be MXN. However, the A-counter causes the pre-scaler modulus to be altered to N+1 for the first A outputs of the pre-scaler. The A-counter then causes the dual-modulus prescaler to revert to a modulus of N until the M-counter reaches its terminal state and resets the entire divider. The overall modulus can be expressed as

$$A(N+1)+N(M-A)$$

where M ≥ A, which simplifies to

$$M \times N + A$$

4.1.3. Feedback Divider Programming

The requirement that M ≥ A means that the feedback divider can only be programmed for certain values below a divider modulus of 56. The selection of divider values is listed in Table 2.

If the desired feedback divider is less than 56, find the divider value in the table. Follow the column up to find the A-counter program value. Follow the row to the left to find the M-counter value.

Above a modulus of 56, the feedback divider can be programmed to any value up to 16383. See both Table 3 and Table 8 for additional programming information.

Table 2: Feedback Modulus Below 56

M-Counter: FBKDIV[13:3]	A-counter: FBKDIV[2:0]							
	000	001	010	011	100	101	110	111
00000000001	8	9	-	-	-	-	-	-
00000000010	16	17	18	-	-	-	-	-
00000000011	24	25	26	27	-	-	-	-
00000000100	32	33	34	35	36	-	-	-
00000000101	40	41	42	43	44	45	-	-
00000000110	48	49	50	51	52	53	54	-
00000000111	56	57	58	59	60	61	62	63
	Feedback Divider Modulus							

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4.1.4. Post Divider

The post divider consists of three individually programmable dividers, as shown in **Error! Reference source not found.**.

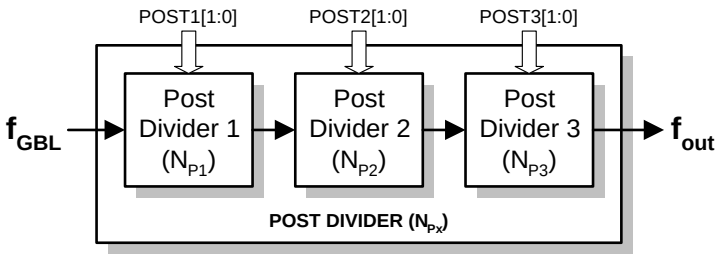

Figure 4: Post Divider

The moduli of the individual dividers are denoted as N_{P1}, N_{P2}, and N_{P3}, and together they make up the array modulus N_{Px}.

$$N_{Px} = N_{P1} \times N_{P2} \times N_{P3}$$

The post divider performs several useful functions. First, it allows the VCO to be operated in a narrower range of speeds compared to the variety of output clock speeds that the device is required to generate. Second, it changes the basic PLL equation to

$$f_{CLK} = f_{REF}\left(\frac{N_F}{N_R}\right)\left(\frac{1}{N_{Px}}\right)$$

The extra integer in the denominator permits more flexibility in the programming of the loop for many applications where frequencies must be achieved exactly.

Note that a nominal 50/50 duty factor is preserved for selections which have an odd modulus.

4.2 Phase Adjust and Sampling

In line-locked or genlocked applications, it is necessary to know the exact phase relation of the output clock relative to the input clock. Since the VCO is included within the feedback loop in a simple PLL structure, the VCO output is exactly phase aligned with the input clock. Every cycle of the input clock equals N_R/N_F cycles of the VCO clock.

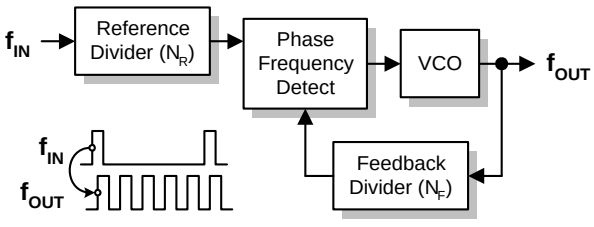

Figure 5: Simple PLL

The addition of a post divider, while adding flexibility, makes the phase relation between the input and output clock unknown because the post divider is outside the feedback loop.

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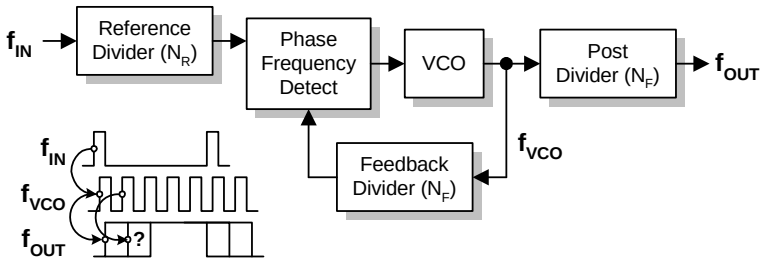

Figure 6: PLL with Post Divider

4.2.1. Clock Gobbler (Phase Adjust)

The clock gobbler circuit takes advantage of the unknown relationship between input and output clocks to permit the adjustment of the CLKP/CLKN output clock phase relative to the REF input. The clock gobbler circuit removes a VCO clock pulse before the pulse clocks the post divider. In this way, the phase of the output clock can be slipped until the output phase is aligned with the input clock phase.

To adjust the phase relationship, switch the feedback divider source to the post divider input via the FBKDSRC bit, and toggle the GBL register bit. The clock gobbler output clock is delayed by one VCO clock period for each transition of the GBL bit from zero to one.

4.2.2. Phase Alignment

To maintain a fixed phase relation between input and output clocks, the post divider must be placed inside the feedback loop. The source for the feedback divider is obtained from the output of the post divider via the FBKDSRC switch. In addition, the feedback divider must be dividing at a multiple of the post divider.

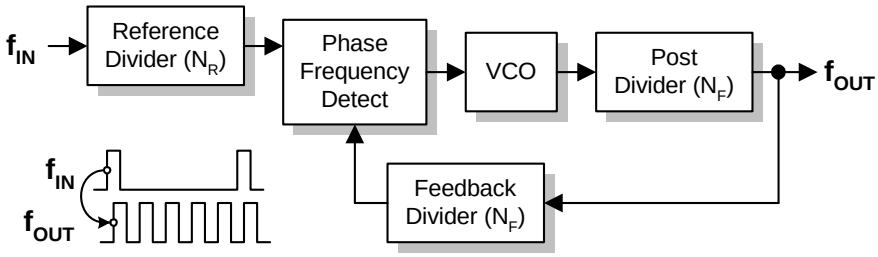

Figure 7: Aligned I/O Phase

4.2.3. Phase Sampling and Initial Alignment

However, the ability to adjust the phase is useless without knowing the initial relation between output and input phase. To aid in the initial synchronization of the output phase to input phase, a phase align "flag" makes a transition (zero to one or one to zero) when the output clock phase becomes aligned with the feedback source phase. The feedback source clock is, by definition, locked to the input clock phase.

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First, the FS6131 is used to sample the output clock with the feedback source clock and set/clear the phase align flag when the two clocks match to within a feedback source clock period. Then, the clock gobbler is used to delay the output phase relative to the input phase one VCO clock at a time until a transition on the flag occurs. When a transition occurs, the output and input clocks are phase aligned.

To enter this mode, set STAT[1] to one and clear STAT[0] to zero. If the CMOS bit is set to one, the LOCK/IPRG pin can display the flag. The flag is always available under software control by reading back the STAT[1] bit, which will be overwritten by the flag in this mode.

4.2.4. Feedback Divider Monitoring

The feedback divider clock can be brought out the LOCK/IPRG pin independent of the output clock to allow monitoring of the feedback divider clock. To enter this mode, set both the STAT[1] and STAT[0] bits to one. The CMOS bit must also be set to one to enable the LOCK/IPRG pin as an output.

4.3 Loop Gain Analysis

For applications where an external loop filter is required, the following analysis example can be used to determine loop gain and stability.

The loop gain of a PLL is the product of all of the gains within the loop.

Set the charge pump current:	$I_{chgpump} = 10\mu A$
Set the loop filter values:	$R_{LF} = 15k\Omega$ $C_1 = 0.015\mu F$ $C_2 = 220pF$
Set the VCO gain (VCOSPD):	$A_{VCO} = 230MHz/V$
Set the feedback divider:	$N_F = 3500$
Set the reference frequency (at the input to the phase detector):	$f_{REF} = 20kHz$

The transfer function of the phase detector and charge pump combination is (in A/rad):

$$K_{PD} = \frac{I_{chgpump}}{2\pi}$$

The transfer function of the loop filter is (in V/A):

$$K_{LF}(s) = \frac{1}{sC_2 + \left(\frac{1}{R_{LF} + \left(1/sC_1 \right)} \right)}$$

The VCO transfer function (in rad/s, and accounting for the phase integration that occurs in the VCO) is:

$$K_{VCO}(s) = 2\pi A_{VCO} \frac{1}{s}$$

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The transfer function of the feedback divider is:

$$K_F = \frac{1}{N_F}$$

Finally, the sampling effect that occurs in the phase detector is accounted for by:

$$K_{SAMP}(s) = \left(\frac{1 - e^{-\left(s / f_{REF} \right)}}{s} \right) f_{REF}$$

The loop gain of the PLL is:

$$K_{LOOP}(s) = K_{PD} K_{LF}(s) K_{VCO}(s) K_F K_{SAMP}(s)$$

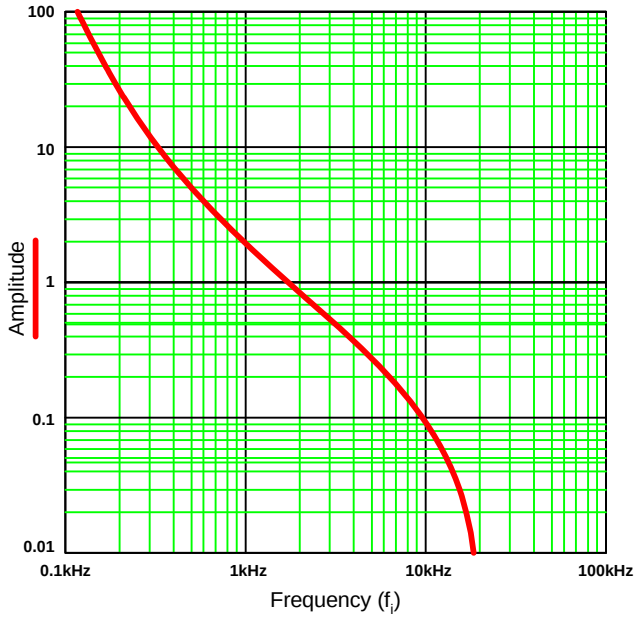

Figure 8: Loop Gain vs. Frequency

The loop phase angle is:

$$\Theta_i = \arg\left[K_{LOOP}(j 2\pi f_{i)} \right]$$

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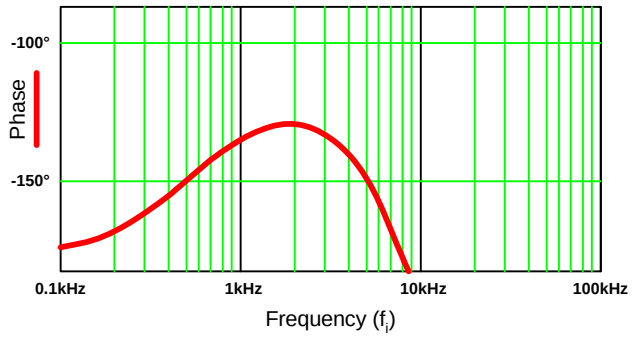

Figure 9: Loop Nyquist Plot

A Nyquist plot of gain vs. amplitude is shown below.

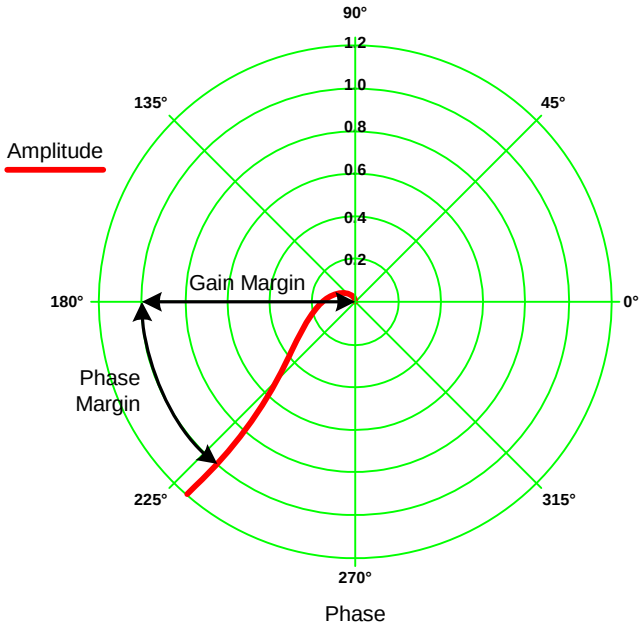

Figure 10: Loop Nyquist Plot

4.4 Voltage-Controlled Crystal Oscillator

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6131 system components. Loading capacitance for the crystal is internal to the device. No external components (other than the resonator itself) are required for operation of the VCXO.

The resonator loading capacitance is adjustable under register control. This feature permits factory coarse tuning of inexpensive resonators to the necessary precision for digital video applications. Continuous fine-tuning of the VCXO frequency is accomplished by

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varying the voltage on the XTUNE pin. The total change (from one extreme to the other) in effective loading capacitance is 1.5pF nominal, and the effect is shown in **Error! Reference source not found.**. The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the "pulling" of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

The motional capacitance of the crystal (usually referred to by crystal manufacturers as C_1), the static capacitance of the crystal (C_0) and the load capacitance (C_L) of the oscillator determine the warping capability of the crystal in the oscillator circuit. A simple formula to determine the total warping capability of a crystal is

$$\Delta f\,(ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where C_{L1} and C_{L2} are the two extremes of the applied load capacitance obtained from Table 11.

Example: A crystal with the following parameters is used with the FS6131. The total coarse tuning range is:

C_1=0.02pF, C_0=5.0pF, C_{L1}=10.0pF, C_{L2}=22.66pF

$$\Delta f = \frac{0.02 \times (22.66 - 10) \times 10^6}{2 \times (5 + 22.66) \times (5 + 10)} = 305\,ppm$$

4.4.1. VCXO Tuning

The VCXO may be coarse tuned by a programmable adjustment of the crystal load capacitance via the XCT[3:0] control bits. See Table 11 for the control code and the associated loading capacitance.

The actual amount of frequency warping caused by the tuning capacitance will depend on the crystal used. The VCXO tuning capacitance includes an external 6pF load capacitance (12pF from the XIN pin to ground and 12pF from the XOUT pin to ground). The fine tuning capability of the VCXO can be enabled by setting the XLVTEN bit to a one, or disabled by setting it to a zero.

Error! Reference source not found. shows the typical effect of the coarse and fine tuning mechanisms. The total coarse tune range is about 350ppm. The difference in VCXO frequency in parts per million (ppm) is shown as the fine tuning voltage on the XTUNE pin varies from 0V to 5V. Note that as the crystal load capacitance is increased the VCXO frequency is pulled somewhat less with each coarse step, and the fine tuning range decreases. The fine tuning range always overlaps a few coarse tuning ranges, eliminating the possibility of holes in the VCXO response. The different crystal warping characteristics may change the scaling on the Y-axis, but not the overall characteristic of the curves.

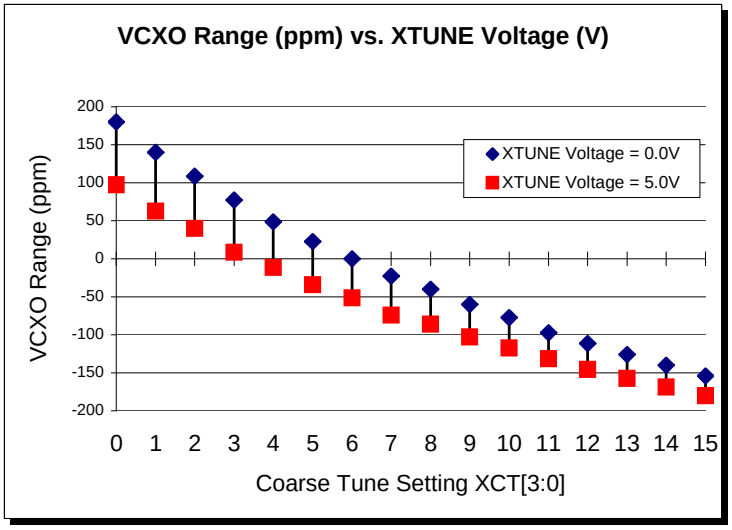

Figure 11: VCXO Course and Fine Tuning

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4.5 Crystal Loop

The crystal loop is designed to attenuate the jitter on a highly jittered, low-Q, low frequency reference. The crystal loop can also maintain a constant frequency output into the main loop if the low frequency reference is intermittent.

The crystal loop consists of a voltage-controllable crystal oscillator (VCXO), a divider, a PFD, and a charge pump that tunes the VCXO to a frequency reference. The frequency reference is phase-locked to the divided frequency of an external, high-Q, jitter-free crystal, thereby locking the VCXO to the reference frequency. The VCXO can continue to run off the crystal even if the frequency reference becomes intermittent.

4.5.1. Locking to an External Frequency Source

When the crystal loop is synchronized to an external frequency source, the FS6131 can monitor the crystal loop and detect if the loop unlocks from the external source. The crystal loop tries to drive to zero frequency if the external source is dropped, and sets a lock status error flag.

The crystal loop can also detect if the VCXO has dropped out of the fine tune range, requiring a change to the coarse tune. The lock status also latches the direction the loop went out of range (high or low) when the loop became unlocked.

4.5.1.1 Crystal Loop Lock Status Flag

To enable this mode, clear the STAT[1] and STAT[0] bits to zero. If the CMOS bit is set to one, the LOCK/IPRG pin will be low if the crystal loop becomes unlocked. The flag is always available under software control by reading back the STAT[1] bit, which is overwritten with the status flag (low = unlocked) in this mode (see Table 6).

4.5.1.2 Out-Of-Range High/Low

The direction the loop has gone out-of-range can be determined by clearing STAT[1] to zero and setting STAT[0] bit to one. If the CMOS bit is set to one, the LOCK/IPRG pin will go high if the crystal loop went out of range high. If the pin goes to a logic-low, the loop went out of range low.

The out-of-range information is also available under software control by reading back the STAT[1] bit, which is overwritten by the flag (high = outof-range high, low = out-of-range low) in this mode. The bit is set or cleared only if the crystal loop loses lock (see Table 6).

4.5.1.3 Crystal Loop Disable

The crystal loop is disabled by setting the XLPDEN bit to a logic-high (1). The bit disables the charge pump circuit in the loop.

Setting the XLPDEN bit low (0) permits the crystal loop to operate as a control loop.

4.6 Connecting the FS6131 to an External Reference Frequency

If a crystal oscillator is not used, tie XIN to ground and shut down the crystal oscillator by setting XLROM[2:0]=1.

The REF and FBK pins do not have pull-up or pull-down current, but do have a small amount of hysteresis to reduce the possibility of extra edges. Signals may be AC-coupled into these inputs with an external DC-bias circuit to generate a DC-bias of 2.5V. Any reference or feedback signal should be square for best results, and the signals should be rail-to-rail. Unused inputs should be grounded to avoid unwanted signal injection.

4.7 Differential Output Stage

The differential output stage supports both CMOS and pseudo-ECL (PECL) signals. The desired output interface is chosen via the program registers (see Table 4).

If a PECL interface is used, the transmission line is usually terminated using a Thévenin termination. The output stage can only sink current in the PECL mode, and the amount of sink current is set by a programming resistor on the LOCK/IPRG pin. The ratio of IPRG current to output drive current is shown in Figure 12. Source current is provided by the pull-up resistor that is part of the Thévenin termination.

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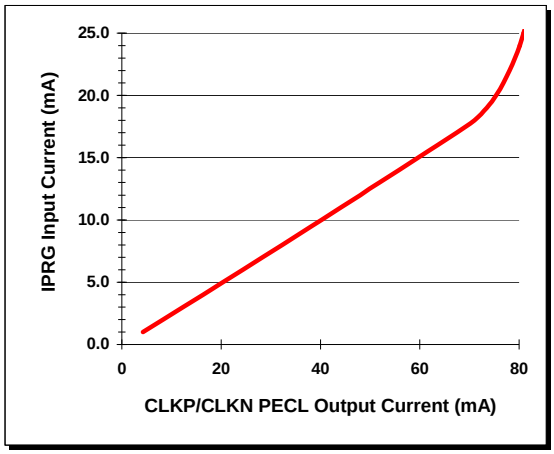

Figure 12: IPRG to CLKP/CLKN Current

5.0 I²C-bus Control Interface

This device is a read/write slave device meeting all Philips I₂C-bus specifications except a "general call." The bus has to be controlled by a master device that generates the serial clock SCL, controls bus access and generates the START and STOP conditions while the device works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated. A device that sends data onto the bus is defined as the transmitter, and a device receiving data as the receiver. I₂C-bus logic levels noted herein are based on a percentage of the power supply (V_{DD}). A logic-one corresponds to a nominal voltage of V_{DD}, while a logic-zero corresponds to ground (V_{SS}).

5.1 Bus Conditions

Data transfer on the bus can only be initiated when the bus is not busy. During the data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line while the clock line is high will be interpreted by the device as a START or STOP condition. The following bus conditions are defined by the I₂C-bus protocol.

5.1.1. Not Busy

Both the data (SDA) and clock (SCL) lines remain high to indicate the bus is not busy.

5.1.2. START Data Transfer

A high to low transition of the SDA line while the SCL in-put is high indicates a START condition. All commands to the device must be preceded by a START condition.

5.1.3. STOP Data Transfer

A low to high transition of the SDA line while SCL is held high indicates a STOP condition. All commands to the device must be followed by a STOP condition.

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5.1.4. Data Valid

The state of the SDA line represents valid data if the SDA line is stable for the duration of the high period of the SCL line after a START condition occurs. The data on the SDA line must be changed only during the low period of the SCL signal. There is one clock pulse per data bit.

Each data transfer is initiated by a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is determined by the master device, and can continue indefinitely. However, data that is overwritten to the device after the first eight bytes will overflow into the first register, then the second, and so on, in a first-in, first-overwritten fashion.

5.1.5. Acknowledge

When addressed, the receiving device is required to generate an acknowledge after each byte is received. The master device must generate an extra clock pulse to coincide with the acknowledge bit. The acknowledging device must pull the SDA line low during the high period of the master acknowledge clock pulse. Setup and hold times must be taken into account.

The master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been read (clocked) out of the slave. In this case, the slave must leave the SDA line high to enable the master to generate a STOP condition.

5.2 I²C-bus Operation

All programmable registers can be accessed randomly or sequentially via this bi-directional two wire digital interface. The crystal oscillator does not have to run for communication to occur.

The device accepts the following I₂C-bus commands.

5.2.1. Slave Address

After generating a START condition, the bus master broadcasts a seven-bit slave address followed by a R/W bit. The address of the device is:

A6	A5	A4	A3	A2	A1	A0
1	0	1	1	X	0	0

where X is controlled by the logic level at the ADDR pin. The variable ADDR bit allows two different FS6131 devices to exist on the same bus. Note that every device on an I₂C-bus must have a unique address to avoid bus conflicts. The default address sets A2 to 0 via the pull-down on the ADDR pin.

5.2.2. Random Register Write Procedure

Random write operations allow the master to directly write to any register. To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write eight bits of data into the addressed register. A final acknowledge is returned by the device, and the master generates a STOP condition.

If either a STOP or a repeated START condition occurs during a register write, the data that has been transferred is ignored.

5.2.3. Random Register Read Procedure

Random read operations allow the master to directly read from any register. To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits the eight-bit word. The master does not acknowledge the transfer but does generate a STOP condition.

5.2.4. Sequential Register Write Procedure

Sequential write operations allow the master to write to each register in order. The register pointer is automatically incremented after each write. This procedure is more efficient than the random register write if several registers must be written.

To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write up to eight bytes of data into the addressed register before the register address pointer overflows back to the beginning address. An acknowledge by the device between each byte of data must occur before the next data byte is sent.

Registers are updated every time the device sends an acknowledge to the host. The register update does not wait for the STOP condition to occur. Registers are therefore updated at different times during a sequential register write.

5.2.5. Sequential Register Read Procedure

Sequential read operations allow the master to read from each register in order. The register pointer is automatically incremented by one after each read. This procedure is more efficient than the random register read if several registers must be read.

To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the register write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits all eight bytes of data starting with the initial addressed register. The register address pointer will overflow if the initial register address is larger than zero. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

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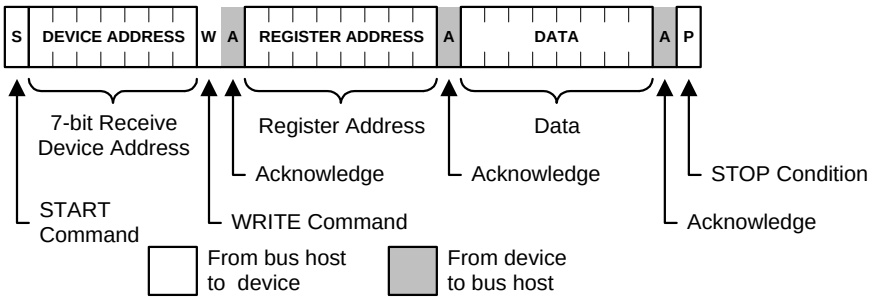

Figure 13: Random Register Write Procedure

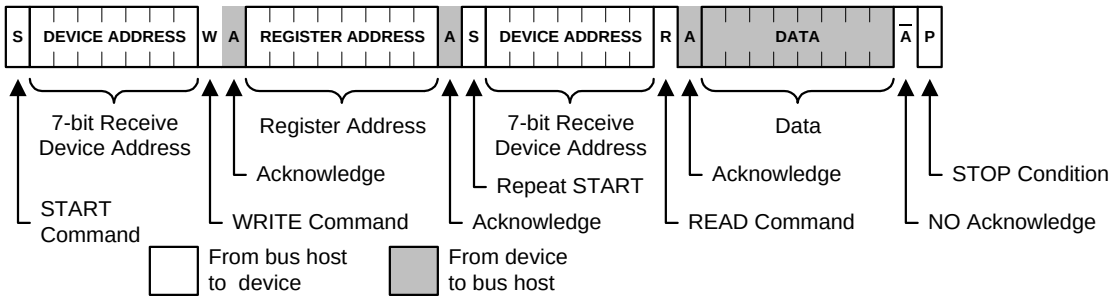

Figure 14: Sequential Register Write Procedure

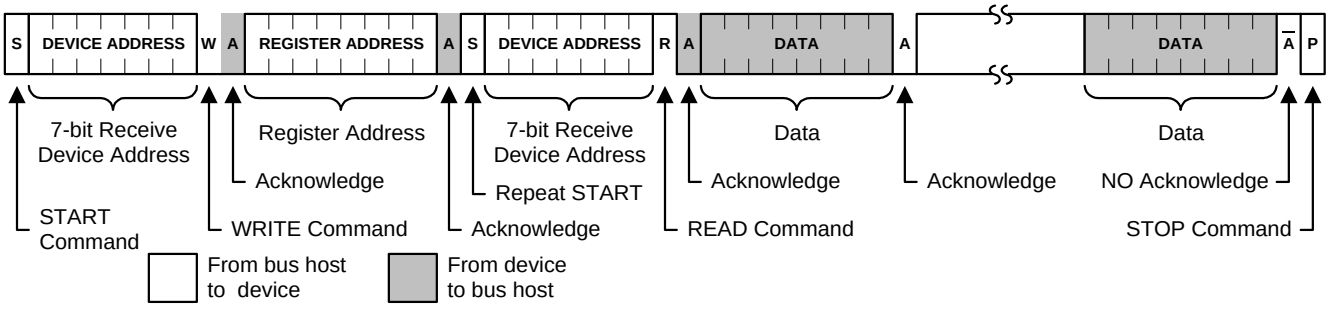

Figure 15: Sequential Register Read Procedure

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6.0 Programming Information

All register bits are cleared to zero on power-up. All register bits may be read back as written except STAT[1] (Bit 63).

Table 3: Register Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 7	STAT[1] (Bit 63)	STAT[0] (Bit 62)	XLVTEN (Bit 61)	CMOS (Bit 60)	XCT[3] (Bit 59)	XCT[2] (Bit 58)	XCT[1] (Bit 57)	XCT[0] (Bit 56)
	00 = Crystal Loop – Lock Status		*0 = Fine Tune Inactive*	*0 = PECL*	*VCXO Coarse Tune See Table 11*			
	01 = Crystal Loop – Out of Range							
	10 = Main Loop – Phase Status		*1 = Fine Tune Active*	*1 = CMOS, Lock Status*				
	11 = Feedback Divider Output							
Byte 6	XLPDEN (Bit 55)	XLSWAP (Bit 54)	XLCP[1] (Bit 53)	XLCP[0] (Bit 52)	XLROM[2] (Bit 51)	XLROM[1] (Bit 50)	XLROM[0] (Bit 49)	GBL (Bit 48)
	0 = Crystal Loop Operates	*0 = Use with External VCXO*	*00 = 1.5µA*		*Crystal Loop Control See Table 10*			*0 = No Clock Phase Adjust*
			01 = 5µA					
	1 = Crystal Loop Powered Down	*1 = Use with Internal VCXO*	*10 = 8µA*					*1 = Clock Phase Delay*
			11 = 24µA					
Byte 5	OUTMUX[1] (Bit 47)	OUTMUX[0] (Bit 46)	OSCTYPE (Bit 45)	VCOSPD (Bit 44)	LFTC (Bit 43)	EXTLF (Bit 42)	MLCP[1] (Bit 41)	MLCP[0] (Bit 40)
	00 = VCO Output		*0 = Low Phase Jitter Oscillator*	*0 = High Speed Range*	*0 = Short Time Constant*	*0 = Internal Loop Filter*	*00 = 1.5µA*	
	01 = Reference Divider Output						*01 = 5µA*	
	10 = Phase Detector Input		*1 = FS6031 Oscillator*	*1 = Low Speed Range*	*1 = Long Time Constant*	*1 = External Loop Filter*	*10 = 8µA*	
	11 = VCXO Output						*11 = 24µA*	
Byte 4	FBKDSRC[1] (Bit 39)	FBKDSRC[0] (Bit 38)	FBKDIV[13] (Bit 37)	FBKDIV[12] (Bit 36)	FBKDIV[11] (Bit 35)	FBKDIV[10] (Bit 34)	FBKDIV[9] (Bit 33)	FBKDIV[8] (Bit 32)
	00 = Post Divider Output		*8192*	*4096*	*2048*	*1024*	*512*	*256*
	01 = FBK Pin							
	10 = Post Divider Input		*M Counter*					
	11 = FBK Pin							
Byte 3	FBKDIV[7] (Bit 31)	FBKDIV[6] (Bit 30)	FBKDIV[5] (Bit 29)	FBKDIV[4] (Bit 28)	FBKDIV[3] (Bit 27)	FBKDIV[2] (Bit 26)	FBKDIV[1] (Bit 25)	FBKDIV[0] (Bit 24)
	128	*64*	*32*	*16*	*8*	*4*	*2*	*1*
	M Counter					*A Counter – See Table 2*		
Byte 2	Reserved (0)	Reserved (0)	POST3[1] (Bit 21)	POST3[1] (Bit 20)	POST2[1] (Bit 19)	POST2[0] (Bit 18)	POST1[1] (Bit 17)	POST1[0] (Bit 16)
			00 = Divide by 1		*00 = Divide by 1*		*00 = Divide by 1*	
			01 = Divide by 3		*01 = Divide by 3*		*01 = Divide by 2*	
			10 = Divide by 5		*10 = Divide by 5*		*10 = Divide by 4*	
			11 = Divide by 4		*11 = Divide by 4*		*11 = Divide by 8*	
Byte 1	PDFBK (Bit 15)	PDREF (Bit 14)	SHUT (Bit 13)	REFDSRC (Bit 12)	REFDIV[11] (Bit 11)	REFDIV[10] (Bit 10)	REFDIV[9] (Bit 9)	REFDIV[8] (Bit 8)
	0 = Feedback Divider	*0 = Reference Divider*	*0 = Main Loop Operates*	*0 = VCXO*	*2048*	*1024*	*512*	*256*
	1 = FBK Pin	*1 = REF Pin*	*1 = Main Loop Powered Down*	*1 = Ref Pin*				
Byte 0	REFDIV[7] (Bit 7)	REFDIV[6] (Bit 6)	REFDIV[5] (Bit 5)	REFDIV[4] (Bit 4)	REFDIV[3] (Bit 3)	REFDIV[2] (Bit 2)	REFDIV[1] (Bit 1)	REFDIV[0] (Bit 0)
	128	*64*	*32*	*16*	*8*	*4*	*2*	*1*

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Table 4: Device Configuration Bits

Name	Description	
REFDSRC (Bit 12)	**REFerence Divider SouRCe**	
	Bit = 0	Crystal Oscillator (VCXO)
	Bit = 1	REF pin
SHUT (Bit 13)	**main loop SHUT down select**	
	Bit = 0	Disabled (main loop operates)
	Bit = 1	Enabled (main loop shuts down)
PDREF (Bit 14)	**Phase Detector REFerence source**	
	Bit = 0	Reference Divider
	Bit = 1	REF pin
PDFBK (Bit 15)	**Phase Detector FeedBacK source**	
	Bit = 0	Feedback Divider
	Bit = 1	FBK pin
FBKDSRC[1:0] (Bits 39-38)	**FeedBacK Divider SouRCe**	
	Bit 39 = 0 Bit 38 = 0	Post Divider Output
	Bit 39 = 0 Bit 38 = 1	FBK pin
	Bit 39 = 1 Bit 38 = 0	VCO Output (Post Divider Input)
	Bit 39 = 1 Bit 38 = 1	FBK pin
EXTLF (Bit 42)	**EXTernal Loop Filter select**	
	Bit = 0	Internal Loop Filter
	Bit = 1	EXTLF pin
OSCTYPE (Bit 45)	**OSCillator TYPe**	
	Bit = 0	Low Phase Jitter Oscillator
	Bit = 1	FS6031 Compatible Oscillator
OUTMUX[1:0] (Bits 47-46)	**OUTput MUltipleXer select**	
	Bit 47 = 0 Bit 46 = 0	Main Loop PLL (VCO Output)
	Bit 47 = 0 Bit 46 = 1	Reference Divider Output
	Bit 47 = 1 Bit 46 = 0	Phase Detector Input
	Bit 47 = 1 Bit 46 = 1	VCXO Output
GBL (Bit 48)	**clock GobBLer control**	
	Bit = 0	No Clock Phase Adjust
	Bit = 1	Clock Phase Delay
CMOS (Bit 60)	**CLKP/CLKN output mode**	
	Bit = 0	PECL Output (positive-ECL output drive)
	Bit = 1	CMOS Output / Lock Status Indicator

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Table 5: LOCK/IPRG Pin Configuration Bits

Name	Description	
STAT[1:0] (Bits 63-62)	**Crystal Loop Lock STATus Mode / Main Loop Phase Align STATus mode** (see also Table 6)	
	Bit 63 = 0 Bit 62 = 0	Crystal Loop Lock status: Locked or Unlocked
	Bit 63 = 0 Bit 62 = 1	Crystal Loop Lock status: Out of Range High or Low
	Bit 63 = 1 Bit 62 = 0	Main Loop Phase Align status
	Bit 63 = 1 Bit 62 = 1	Feedback Divider output

Table 6: Lock Status

CMOS	STAT [1]	STAT [0]	LOCK / IPRG PIN	STAT[1] Read	Status
1	0	0	1	1	Locked
			0	0	Unlocked
1	0	1	0	0	Out-of-Range: Low
			1	1	Out-of-Range: High

Table 7: Main Loop Tuning Bits

Name	Description	
VCOSPD (Bit 44)	**VCO SPeeD range select** (see Table 16)	
	Bit = 0	High Speed Range
	Bit = 1	Low Speed Range
MLCP[1:0] (Bits 41-40)	**Main Loop Charge Pump current**	
	Bit 41 = 0 Bit 40 = 0	Current = 1.5μA
	Bit 41 = 0 Bit 40 = 1	Current = 5μA
	Bit 41 = 1 Bit 40 = 0	Current = 8μA
	Bit 41 = 1 Bit 40 = 1	Current = 24μA
LFTC (Bit 43)	**Loop Filter Time Constant** (internal)	
	Bit = 0	Short Time Constant: 13.5μs
	Bit = 1	Long Time Constant: 135μs

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Table 8: Divider Control Bits

Name	Description	
REFDIV[11:0] (Bits 11-0)	**REFerence DIVider (N_R)**	
FBKDIV[13:0] (Bits 37-24)	**FeedBacK DIVider (N_F)**	
	FBKDIV[2:0]	A-Counter Value
	FBKDIV[13:3]	M-Counter Value
POST1[1:0] (Bits 17-16)	**POST Divider #1 (N_{P1})**	
	Bit 17 = 0 Bit 16 = 0	Divide by 1
	Bit 17 = 0 Bit 16 = 1	Divide by 2
	Bit 17 = 1 Bit 16 = 0	Divide by 4
	Bit 17 = 1 Bit 16 = 1	Divide by 8
POST2[1:0] (Bits 19-18)	**POST Divider #2 (N_{P2})**	
	Bit 19 = 0 Bit 18 = 0	Divide by 1
	Bit 19 = 0 Bit 18 = 1	Divide by 3
	Bit 19 = 1 Bit 18 = 0	Divide by 5
	Bit 19 = 1 Bit 18 = 1	Divide by 4
POST3[1:0] (Bits 21-20)	**POST Divider #3 (N_{P3})**	
	Bit 21 = 0 Bit 20 = 0	Divide by 1
	Bit 21 = 0 Bit 20 = 1	Divide by 3
	Bit 21 = 1 Bit 20 = 0	Divide by 5
	Bit 21 = 1 Bit 20 = 1	Divide by 4
Reserved (0) (Bits 23-22)	Set these reserved bits to 0	

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Table 9: Crystal Loop Tuning Bits

Name	Description	
XLCP[1:0] (Bits 53-52)	**Crystal Loop Charge Pump current**	
	Bit 53 = 0 Bit 52 = 0	Current = 1.5µA
	Bit 53 = 0 Bit 52 = 1	Current = 5µA
	Bit 53 = 1 Bit 52 = 0	Current = 8µA
	Bit 53 = 1 Bit 52 = 1	Current = 24µA
XLROM[2:0] (Bits 51-49)	**Crystal Loop Divider ROM select and Crystal Oscillator Power-Down** (see **Error! Reference source not found.**)	
XLVTEN (Bit 61)	**Crystal Loop Voltage fine Tune ENable**	
	Bit = 0	Disabled (fine tune is inactive)
	Bit = 1	Enabled (fine tune is active)
XLSWAP (Bit 54)	**Crystal Loop SWAP polarity**	
	Bit = 0	Use with an external VCXO that *increases* in frequency in response to an *increasing* voltage at the XTUNE pin.
	Bit = 1	Use with a VCXO that *increases* in frequency in response to a *decreasing* voltage at the XTUNE pin. **Use this setting for Internal VCXO**
XLPDEN (Bit 55)	**Crystal Loop Power Down Enable**	
	Bit = 0	Disabled (crystal loop operates)
	Bit = 1	Enabled (crystal loop is powered down)
XCT[3:0] (Bits 59-56)	**Crystal Coarse Tune** (see Table 11)	

Table 10: Crystal Loop Control ROM

XLROM [2]	XLROM [1]	XLROM [0]	VCXO Divider	Crystal Frequency (MHz)
0	0	0	1	-
0	0	1	3072	24.576
0	1	0	3156	25.248
0	1	1	2430	19.44
1	0	0	2500	20.00
1	0	1	4000	32.00
1	1	0	3375	27.00
1	1	1	Crystal oscillator power-down	

6.1 VCXO Coarse Tune

The VCXO may be coarse tuned by a programmable adjustment of the crystal load capacitance via XCT[3:0]. The actual amount of frequency warping caused by the tuning capacitance will depend on the crystal used. The VCXO tuning capacitance includes an external 6pF load capacitance (12pF from the XIN pin to ground and 12pF from the XOUT pin to ground). The fine tuning capability of the VCXO can be enabled by setting the XLVTEN bit to a logic-one, or disabled by setting the bit to a logic-zero.

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Table 11: VCXO Coarse Running Capacitance

XCT[3]	XCT[2]	XCT[1]	XCT[0]	VCXO Tuning Capacitance (pf)
0	0	0	0	10.00
0	0	0	1	10.84
0	0	1	0	11.69
0	0	1	1	12.53
0	1	0	0	13.38
0	1	0	1	14.22
0	1	1	0	15.06
0	1	1	1	15.91
1	0	0	0	16.75
1	0	0	1	17.59
1	0	1	0	18.43
1	0	1	1	19.28
1	1	0	0	20.13
1	1	0	1	20.97
1	1	1	0	21.81
1	1	1	1	22.66

7.0 Electrical Specifications

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, dc (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

CAUTION: ELECTROSTATIC SENSITIVE DEVICE
Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

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Table 13: Operating Conditions

Parameter	Symbol	Conditions/Descriptions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	5V ± 10%	4.5	5	5.5	V
Ambient Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XIN}		19.44	27	28	MHz
Crystal Resonator Load Capacitance	C_{XL}	Parallel resonant, AT cut		18		pF
Crystal Resonator Motional Capacitance	C_{XM}	Parallel resonant, AT cut		25		fF
Serial Data Transfer Rate		Standard mode	10	100	400	kb/s
PECL Mode Programming Current (LOCK/IPRG Pin High-Level Input Current)	I_{IH}	PECL Mode			15	mA
Output Driver Load Capacitance	C_L				15	pF

Table 14: DC Electrical Specifications

Parameter	Symbol	Conditions/Description	Min.	Typ.	Max.	Units
Overall						
Supply Current, Dynamic, (with Loaded Outputs)	I_{DD}	f_{CLK} = 66MHz ; CMOS Mode, V_{DD} = 5.5V		100		mA
Supply Current, Static	I_{DDL}	SHUT = 1, XLROM[2:0] = 7, XLPDEN = 1 V_{DD} = 5.5V		12		mA
Serial Communication I/O (SDA, SCL)						
High-Level Input Voltage	V_{IH}	Outputs off	3.5		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	Outputs off	V_{SS}-0.3		1.5	V
Hysteresis Voltage *	V_{hys}	Outputs off		2		V
Input Leakage Current	I_I		-1		1	µA
Low-Level Output Sink Current (SDA)	I_{OL}	V_{OL} = 0.4V	20	32		mA
Tristate Output Current	I_Z		-10		10	µA
Address Select Input (ADDR)						
High-Level Input Voltage	V_{IH}		2.4		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current (pull-down)	I_{IH}	V_{IH} = V_{DD} = 5.5V	5	16	30	µA
Low-Level Input Current	I_{IL}		-2		2	µA
Reference Frequency Input (REF, FBK)						
High-Level Input Voltage	V_{IH}		3.5		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		1.5	V
Hysteresis Voltage	V_{hys}		500			mV
Input Leakage Current	I_I		-1		1	µA

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Table 14: DC Electrical Specifications (Continued)

Parameter	Symbol	Conditions/Description	Min.	Type.	Max.	Units
Loop Filter Input (EXTLF)						
Input Leakage Current	I_I	EXTLF = 0	-1		1	µA
High-Level Output Source Current	I_{OH}	V_O = 0.8V; EXTLF =1, MLCP[1:0] = 0		-1.5		µA
		V_O = 0.8V; EXTLF =1, MLCP[1:0] = 1		-5		
		V_O = 0.8V; EXTLF =1, MLCP[1:0] = 2		-8		
		V_O = 0.8V; EXTLF =1, MLCP[1:0] = 3		-24		
Low-Level Output Sink Current	I_{OL}	V_O = 4.2V; EXTLF =1, MLCP[1:0] = 0		1.5		µA
		V_O = 4.2V; EXTLF =1, MLCP[1:0] = 1		5		
		V_O = 4.2V; EXTLF =1, MLCP[1:0] = 2		8		
		V_O = 4.2V; EXTLF =1, MLCP[1:0] = 3		25		
Crystal Oscillator Input (XIN)						
Threshold Bias Voltage	V_{TH}		1.5	2.2	3.5	V
High-Level Input Current	I_{IH}	Outputs off; V_{IH} = 5V	10	24	30	mA
Low-Level Input Current	I_{IL}	Outputs off; V_{IL} = 0V	-10	-19	-30	mA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT; VCXO tuning disabled		10		pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XOUT; XIN unconnected; VCXO disabled		20		pF
Crystal Oscillator Output (XOUT)						
High-Level Output Source Current	I_{OH}	V_O = 0V, float XIN	-20	-30	-50	mA
Low-Level Output Sink Current	I_{OL}	V_O = 5V, float XIN	-20	-40	-50	mA
VCXO Tuning I/O (XTUNE)						
High-Level Input Voltage	V_{IH}	Lock Status: Out of Range HIGH	3.2		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	Lock Status: Out of Range LOW	V_{SS}-0.3		0.3	V
Hysteresis Voltage	V_{hys}		1.0			V
Input Leakage Current	I_I	XLPDEN = 0	-1		1	µA
High-Level Output Source Current	I_{OH}	V_O = 0.8V; XLCP[1:0] = 0		-1.5		µA
		V_O = 0.8V; XLCP[1:0] = 1		-5		
		V_O = 0.8V; XLCP[1:0] = 2		-8		
		V_O = 0.8V; XLCP[1:0] = 3		-24		
Low-Level Output Sink Current	I_{OL}	V_O = 4.2V; XLCP[1:0] = 0		1.5		µA
		V_O = 4.2V; XLCP[1:0] = 1		5		
		V_O = 4.2V; XLCP[1:0] = 2		8		
		V_O = 4.2V; XLCP[1:0] = 3		25		
Lock Indicator / PECL Current Program I/O (LOCK/IPRG)						
Low-Level Input Current	I_{IL}	PECL Mode	-1		1	µA
High-Level Output Source Current	I_{OH}	CMOS Mode; V_O = 2.4V	-25	-38		mA
Low-Level Output Sink Current	I_{OL}	CMOS Mode; V_O = 0.4V	5	9		mA
Output Impedance *	z_{OH}	V_O = 0.5V_{DD}; output driving high		66		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		76		
Short Circuit Source Current *	I_{SCH}	V_O = 0V; shorted for 30s, max.		-47		mA
Short Circuit Sink Current *	I_{SCL}	V_O = 5V; shorted for 30s, max.		47		mA

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Table 14: DC Electrical Specifications (Continued)

Parameter	Symbol	Conditions/Description	Min.	Typ.	Max.	Units
Clock Outputs, CMOS Mode (CLKN, CLKP)						
High-Level Output Source Current	I_{OH}	V_O = 2.4V	-45	-68		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V	15	20		mA
Output Impedance *	z_{OH}	$V_O = 0.5V_{DD}$; output driving high		28		Ω
	z_{OL}	$V_O = 0.5V_{DD}$; output driving low		33		
Short Circuit Source Current *	I_{SCH}	V_O = 0V; shorted for 30s, max.		-100		mA
Short Circuit Sink Current *	I_{SCL}	V_O = 5V; shorted for 30s, max.		100		mA
Clock Outputs, PECL Mode (CLKN, CLKP)						
IPRG Current to Output Current Ratio				1:4		
Low-Level Output Sink Current	I_{OL}	IPRG input current = 15mA		60		mA
Tristate Output Current	I_Z		-10		10	µA

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

Table 15: AC Timing Specifications

Parameter	Symbol	Conditions/Description	Clock (MHz)	Min.	Typ.	Max.	Units
Overall							
Output Frequency *	$f_{O(max)}$	CMOS Outputs				130	MHz
		PECL Outputs				230	
VCO Frequency *	f_{VCO}	Low Phase Jitter Oscillator (OSCTYPE = 0)					MHz
		VCOSPD = 0		40		160	
		VCOSPD = 1		40		100	
		FS6031 Compatible Oscillator (OSCTYPE = 1)					
		VCOSPD = 0		40		230	
		VCOSPD = 1		40		140	
VCO Gain *	A_{VCO}	Low Phase Jitter Oscillator (OSCTYPE = 0)					MHz/V
		VCOSPD = 0			125		
		VCOSPD = 1			75		
		FS6031 Compatible Oscillator (OSCTYPE = 1)					
		VCOSPD = 0			130		
		VCOSPD = 1			78		
Loop Filter Time Constant *		LFTC = 0			13.5		µs
		LFTC = 1			135		
Rise Time *	t_r	CMOS Outputs, V_O = 0.5V to 4.5V; C_L = 15pF			1.1		ns
Fall Time *	t_f	CMOS Outputs, V_O = 4.5V to 0.5V; C_L = 15pF			0.8		ns
Lock Time (Main Loop) *		Frequency Synthesis			200		µs
		Line Locked Modes (8kHz reference)			10		ms
Disable Time *		From falling edge of SCL for the last data bit (SHUT = 1 to 0) to output locked			10		µs

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Table 15: AC Specifications (Continued)

Parameter	Symbol	Conditions/Description	Clock (MHz)	Min.	Typ.	Max.	Units
Divider Modulus							
Feedback Divider	N_F	FBKDIV[13:0] (See also Table 2)		8		16383	
Reference Divider	N_R	REFDIV[11:0]		1		4095	
Post Divider	N_{P1}	POST1[1:0] (See also Table 8)		1		8	
	N_{P2}	POST2[1:0] (See also Table 8)		1		5	
	N_{P3}	POST3[1:0] (See also Table 8)		1		5	
Clock Output (CLKP, CLKN)							
Duty Cycle *		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	47		54	%
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	Rising edges 50ms apart at 2.5V, relative to an ideal clock, C_L=15pF, f_{REF}=8kHz, N_R=1, N_F=193, N_{Px}=64, C_{LF}=0.054µF, R_{LF}=15.7kΩ, C_{LP}=1800pF, OSCTYPE=0, MLCP=3, XLROM=7	1.544		270		ps
		Rising edges 50ms apart at 2.5V, relative to an ideal clock, C_L=15pF, f_{REF}=15kHz, N_R=1, N_F=800, N_{Px}=10, C_{LF}=0.0246µF, R_{LF}=15.7kΩ, C_{LP}=820pF, OSCTYPE=0, MLCP=3, XLROM=7	12.00		160		
		On rising edges 5ms apart at 2.5V relative to an ideal clock, C_L=15pF, f_{REF}=31.5kHz, N_R=1, N_F=799, N_{Px}=4, C_{LF}=0.015µF, R_{LF}=15.7kΩ, C_{LP}=470pF, OSCTYPE=0, MLCP=3, XLROM=7	25.175		100		
		On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, CMOS mode, f_{XIN}=27MHz, N_F=200, N_R=27, N_{Px}=2	100		30		
		On rising edges 500µs apart at 2.5V relative to an ideal clock, C_L=15pF, PECL mode, f_{XIN}=27MHz, N_F=200, N_R=27, N_{Px}=1	200		30		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at 2.5V, C_L=15pF, f_{REF}=8kHz, N_R=1, N_F=193, N_{Px}=64, C_{LF}=0.054µF, R_{LF}=15.7kΩ, C_{LP}=1800pF, OSCTYPE=0, MLCP=3, XLROM=7	1.544		140		ps
		From rising edge to next rising edge at 2.5V, C_L=15pF, f_{REF}=15kHz, N_R=1, N_F=800, N_{Px}=10, C_{LF}=0.0246µF, R_{LF}=15.7kΩ, C_{LP}=820pF, OSCTYPE=0, MLCP=3, XLROM=7	12.00		130		
		From rising edge to next rising edge at 2.5V, C_L=15pF, f_{REF}=31.5kHz, N_R=1, N_F=799, N_{Px}=4, C_{LF}=0.015µF, R_{LF}=15.7kΩ, C_{LP}=470pF, OSCTYPE=0, MLCP=3, XLROM=7	25.175		105		
		From rising edge to next rising edge at 2.5V, C_L=15pF, CMOS mode, f_{XIN}=27MHz, N_F=200, N_R=27, N_{Px}=2	100		340		
		From rising edge to next rising edge at 2.5V, C_L=15pF, PECL mode, f_{XIN}=27MHz, N_F=200, N_R=27, N_{Px}=1	200		270		

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data at T_A = 27°C and are not production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

Table 16: Serial Interface Timing Specifications

Parameter	Symbol	Conditions/Description	Min.	Max.	Units
Clock frequency	f_{SCL}	SCL	0	400	kHz
Bus free time between STOP and START	t_{BUF}		4.7		µs
Set up time, START (repeated)	$t_{su:STA}$		4.7		µs
Hold time, START	$t_{hd:STA}$		4.0		µs
Set up time, data input	$t_{su:DAT}$	SDA	250		ns
Hold time, data input	$t_{hd:DAT}$	SDA	0		µs
Output data valid from clock	t_{AA}	Minimum delay to bridge undefined region of the falling edge of SCL to avoid unintended START or STOP		3.5	µs
Rise time, data and clock	t_R	SDA, SCL		1000	ns
Fall time, data and clock	t_F	SDA, SCL		300	ns
High time, clock	t_{HI}	SCL	4.0		µs
Low time, clock	t_{LO}	SCL	4.7		µs
Set up time, STOP	$t_{su:STO}$		4.0		µs

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

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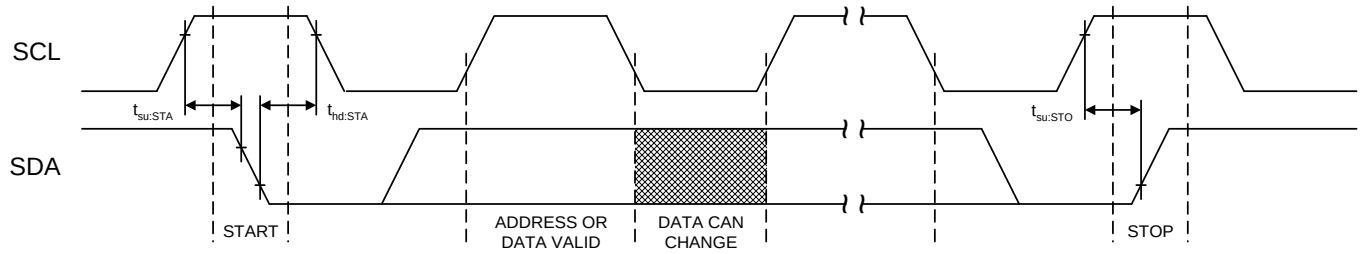

Figure 16: Bus Timing Data

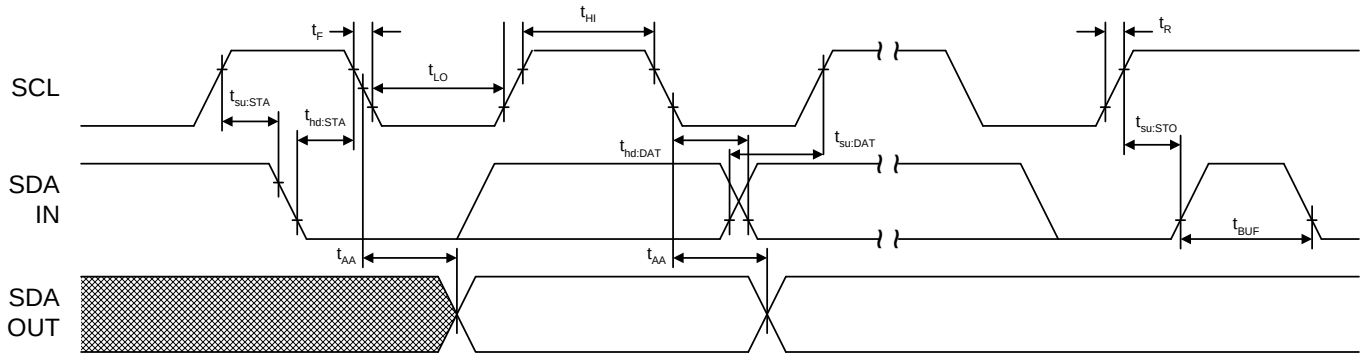

Figure 17: Data Transfer Sequence

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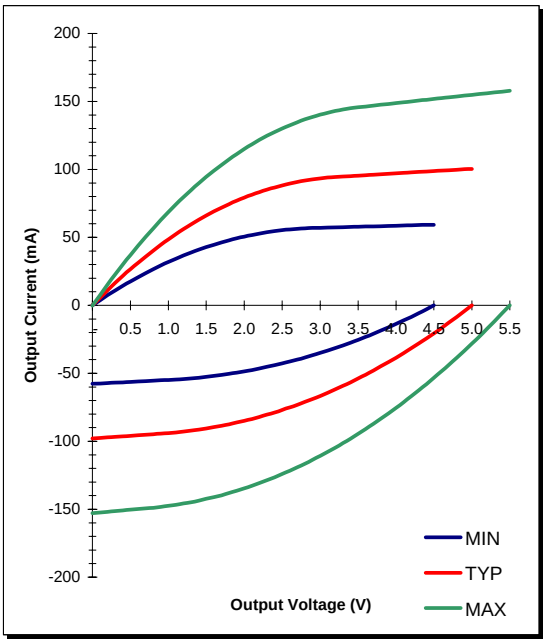
Table 17: CLKP, CLKN Clock Outputs (CMOS Mode)

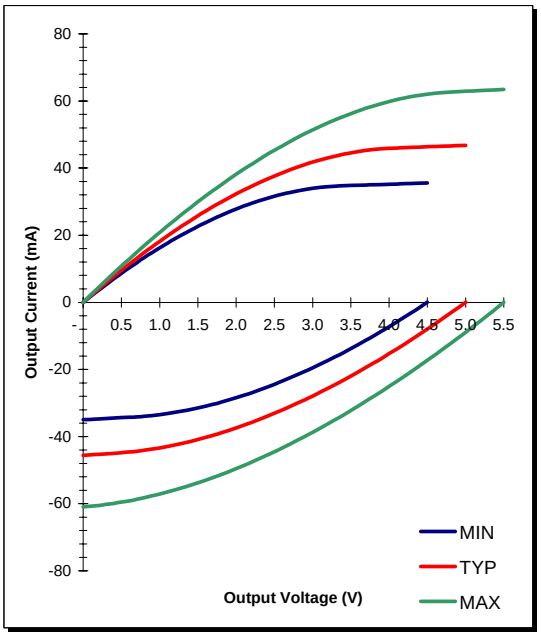
Voltage (V)	Low Drive Current (mA)			Voltage (V)	High Drive Current (mA)		
	Min.	Typ.	Max.		Min.	Typ.	Max.
0	0	0	0	0	-58	-98	-153
0.2	7	11	15	0.5	-56	-96	-150
0.5	18	27	37	1	-55	-94	-148
0.7	24	36	50	1.5	-53	-91	-142
1	32	49	69	2	-49	-85	-135
1.2	37	56	80	2.5	-43	-77	-124
1.5	43	66	95	2.7	-40	-73	-119
1.7	46	72	103	3	-35	-67	-111
2	51	79	115	3.2	-31	-62	-105
2.2	53	83	122	3.5	-25	-54	-95
2.5	55	88	130	3.7	-21	-48	-87
2.7	56	91	135	4	-14	-39	-75
3	57	93	140	4.2	-8	-32	-67
3.5	58	95	146	4.5	0	-21	-53
4	59	97	149	4.7		-13	-44
4.5	59	99	152	5		0	-28
5		100	155	5.2			-17
5.5			158	5.5			0



The data in this table represents nominal characterization data only.

Table 18: LOCK/IPRG Clock Output (CMOS Mode)

Voltage (V)	Low Drive Current (mA)			Voltage (V)	High Drive Current (mA)		
	Min.	Typ.	Max.		Min.	Typ.	Max.
0	0	0	0	0	-35	-46	-61
0.2	4	4	4	0.5	-34	-45	-60
0.5	9	10	11	1	-33	-43	-57
0.7	12	13	15	1.5	-31	-41	-54
1	16	18	21	2	-28	-37	-50
1.2	19	21	25	2.5	-24	-33	-45
1.5	23	26	30	2.7	-23	-31	-42
1.7	25	29	33	3	-20	-28	-39
2	28	32	38	3.2	-17	-26	-36
2.2	29	35	41	3.5	-14	-22	-32
2.5	32	38	45	3.7	-11	-19	-29
2.7	33	39	48	4	-7	-15	-25
3	34	42	51	4.2	-4	-12	-22
3.5	35	45	56	4.5	0	-8	-17
4	35	46	60	4.7		-5	-14
4.5	36	46	62	5		0	-9
5		47	63	5.2			-5
5.5			63	5.5			0



The data in this table represents nominal characterization data only.

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8.0 Package Information for Both ‘Green’/’ROHS’ and ‘Non-Green’

Table 19: 16-pin SOIC (0.150") Package Dimensions

	Dimension			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

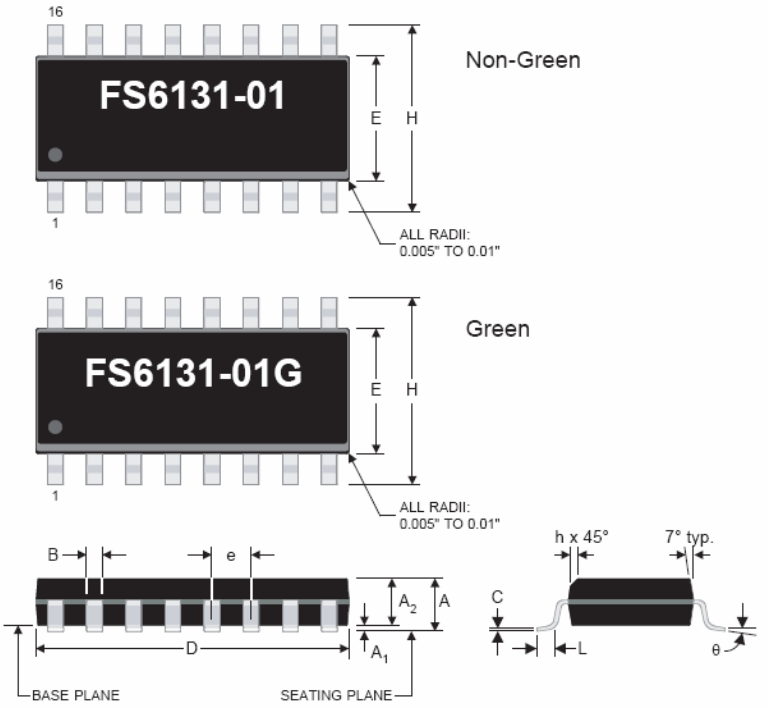

Table 20: 16-pin SOIC (0.150") Package Characteristics

Parameter	Symbol	Conditions/Description	Typ.	Units
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 ft./min.	108	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

9.0 Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range
FS6131-01G-XTD	16-pin (0.150”) SOIC (green, ROHS or lead free packaging)	Tube/Tray	0° C to 70° C (Commercial)
FS6131-01G-XTP	16-pin (0.150”) SOIC (green, ROHS or lead free packaging)	Tape & Reel	0° C to 70° C (Commercial)
FS6131-01i-XTD	16-pin (0.150”) SOIC (small outline package)	Tube/Tray	-40° C to 85° C (Industrial)
FS6131-01i-XTP	16-pin (0.150”) SOIC (small outline package)	Tape & Reel	-40° C to 85° C (Industrial)

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10.0 Demonstration Software

MS Windows® based software is available from ON SEMICONDUCTOR that illustrates the capabilities of the FS6131.

10.1 Software Requirements

• PC running MS Windows 95, 98, 98SE, ME, NT4, 2000, XP Home or Professional Editions.
• 2.0MB available space on hard drive C:

10.2 Demo Program Operation

Run the fs6131.exe program. A warning message will appear stating that the hardware is not connected. Click “Ignore”.

The FS6131 demonstration hardware is no longer supported by ON SEMICONDUCTOR.

The opening screen is shown in Figure 18.

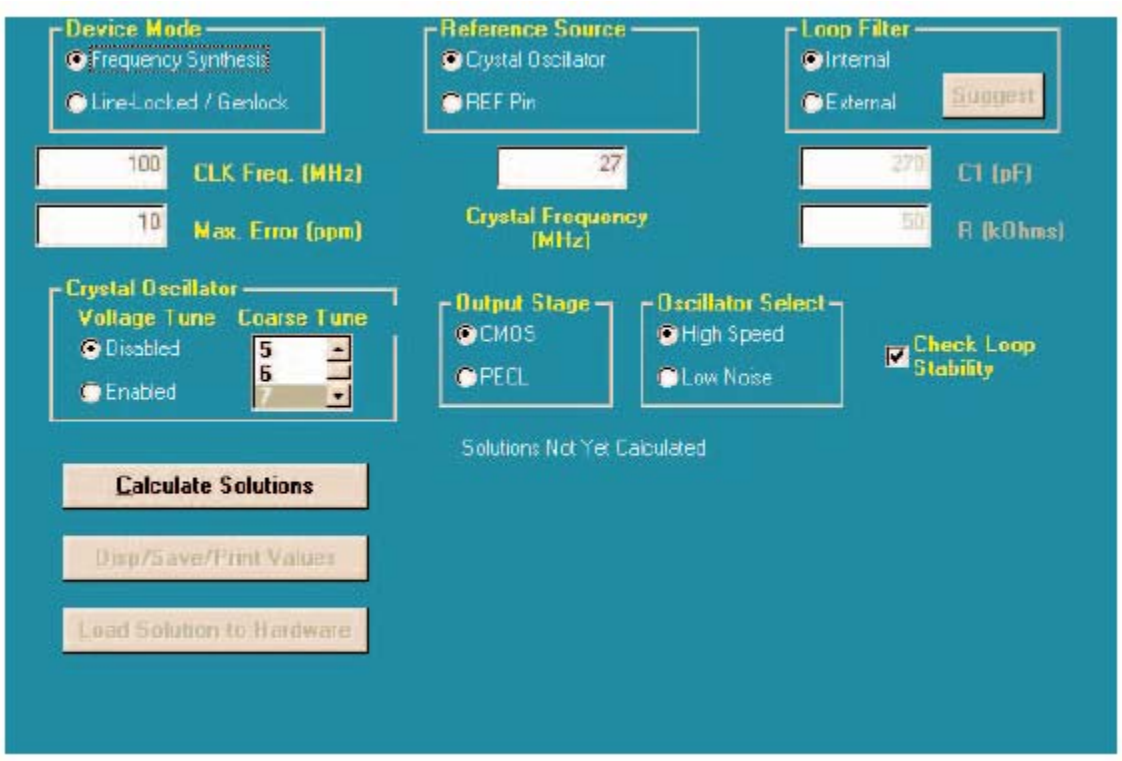

Figure 18: Opening Screen

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10.2.1. Device Mode

The device mode block presets the demo program to program the FS6131 either as a frequency synthesizer (a stand alone clock generator) or as a line-locked or genlock clock generator.

Frequency Synthesis: For use as a stand alone clock generator. Note that the reference source is the on-chip crystal oscillator, the expected crystal frequency is 27MHz, and the voltage tune in the crystal oscillator (i.e. the VCXO) is disabled. The default output frequency (CLK freq.) requested is 100MHz, with a maximum error of 10ppm, or about 100Hz. The output stage defaults to CMOS mode.

Line-Locked/Genlock: For use in a line-lock or genlock application. Note that the reference source is the REF pin, and that the expected reference frequency is 8kHz. The default output frequency requested is a 100x multiple of the reference frequency.

10.2.2. Example: Frequency Synthesizer Mode

By default the demo program assumes the FS6131 is configured as a stand alone clock generator. Note that the reference source defaults to the on-chip crystal oscillator, the expected crystal frequency is 27MHz, and the voltage tune in the **Crystal Oscillator** block (i.e. the VCXO) is disabled. The default output frequency (CLK freq.) requested is 100MHz, with a maximum error of 10ppm, or about 100Hz. The **Output Stage** defaults to CMOS mode. The **Loop Filter** block is set to internal, and the **Check Loop Stability** switch is on.

As an exercise, click on **Calculate Solutions**. The program takes into account all of the screen settings and calculates all possible combinations of reference, feedback and post divider values that will generate the output frequency (100MHz) from the input frequency (27MHz) within the desired tolerance (10ppm).

A box will momentarily appear: "Calculating Solutions: Press cancel to stop with the solutions calculated so far." A number in the box will increment for every unique solution that is found. This example will create seven unique solutions, which are then displayed in a window in the lower right portion of the program screen.

The best PLL performance is obtained by running the VCO at as high a speed as possible. The last three solutions show a VCO speed of 200MHz. Furthermore, good PLL performance is obtained with the smallest dividers possible, which means solution #4 should provide the best results.

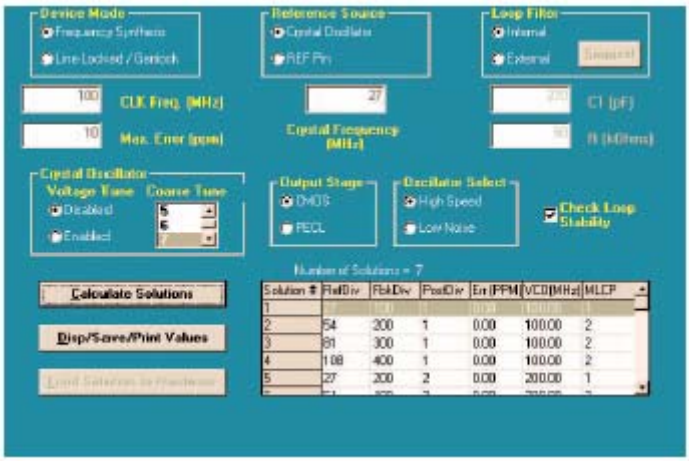

Figure 19: Frequency Synthesizer Screen

Clicking on Solution #4 highlights the row, and clicking on **Disp/Save Register Values** provides a window with the final values of key settings. A click on OK then displays a second window containing register information per the register map. If the solutions are to be saved to a file, two formats are available: a text format for viewing, and a data format for loading into the FS6131.

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Note: As an update to this data sheet, the FS6131 hardware is no longer available from ON SEMICONDUCTOR.

10.2.3. Example: Line-Locked Mode

Selecting the line-locked/genlock option in the **Device Mode** block changes the program default settings. The **Reference Source** changes to the REF pin input, and a block appears to permit entry of the REF input frequency in MHz. A **Desired Multiple** block allows entry of the reference frequency multiplying factor used to generate the output frequency.

Exercise: Change the ref pin frequency to 0.0315MHz, and alter the desired multiple to 800. Change the loop filter block to external, but leave the values for C1 and R alone.

Click on **Calculate Solutions**. The program takes into account all of the current screen settings and calculates all possible combinations of reference, feedback and post divider values that will generate an output frequency from the input frequency (31.5kHz) multiplied by the desired multiple of 800.

A box will appear: "No solutions were found! Do you want to retry calculations with the check loop stability option turned off?" Choose **Yes**.

Another box may momentarily appear: "Calculating Solutions: Press cancel to stop with the solutions calculated so far." A number in the box will increment for every unique solution that is found. This example will create eight unique solutions, which are then displayed in a window in the lower right portion of the program screen.

For best results, try to keep the PostDiv value multiplied by the FbkDiv value from getting larger than 5000 while running the VCO as much above 70MHz as possible. If a tradeoff must be made, it is better to run the VCO faster and allow the divider values to get large. Solution #3 provides a PostDiv value of 4 and a FbkDiv value of 800 for a combined value of 3200. The VCO is running at about 100MHz.

Click on Solution #3 to highlight the row, then click on **Suggest** in the **Loop Filter** box to have the program choose loop filter values. Suggested values for an external loop filter are 4700pF and 47kW.

Now reselect the **Check Loop Stability** box to turn this feature on. Clicking on **Calculate Solutions** regenerates the same solutions provided earlier, only this time the new loop filter values were used.

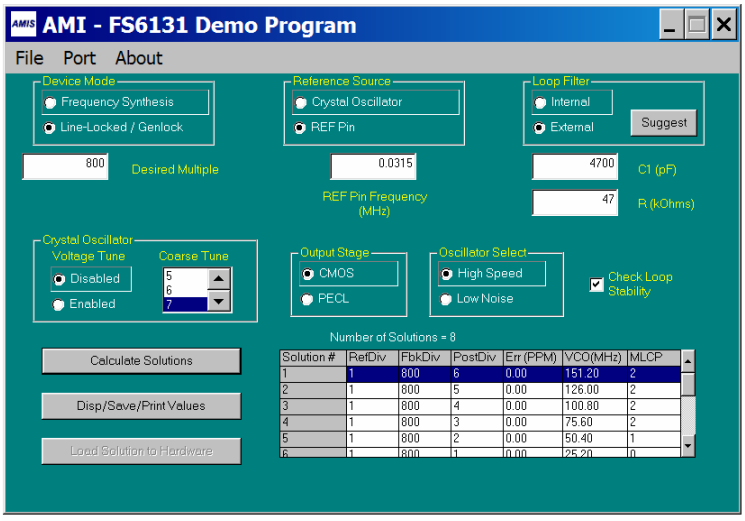

Figure 20: Line-Locked Screen

Clicking on Solution #3 highlights the row, and clicking on **Disp/Save Register Values** provides a window with the final values of key settings. A click on OK then displays a second window containing register information per the register map. If the solutions are to be saved to a file, two formats are available: a text format for viewing and a data format for loading into the FS6131.

Table 21: Sample Text Output

```
ON SEMICONDUCTOR - FS6131 Solution Text File
Created: Today's Date, Today's Time

Line-Locked / Genlock Mode
Desired Multiple = 800
Source = 0.0315MHz Reference Pin
External Loop Filter C1 = 4700pF  R = 47kOhms
Crystal Oscillator Voltage Tune Disabled
Output Stage = CMOS

Reference Divider  =  1
Feedback Divider   =  800
Post Divider       =  4
Charge Pump (uA)   =  10
EXTLF              =  1
XLVTEN             =  0
XCT                =  7
CMOS               =  1

Register 0  = 1H (1)
Register 1  = 40H (64)
Register 2  = 2H (2)
Register 3  = 20H (32)
Register 4  = 3H (3)
Register 5  = 26H (38)
Register 6  = 0H (0)
Register 7  = 17H (23)
```

11.0 Applications Information

A signal reflection will occur at any point on a PC-board trace where impedance mismatches exist. Reflections cause several undesirable effects in high-speed applications, such as an increase in clock jitter and a rise in electromagnetic emissions from the board. Using a properly designed series termination on each high-speed line can alleviate these problems by eliminating signal reflections.

11.1 PECL Output Mode

If a PECL interface is desired, the transmission line must be terminated using a Thévenin, or dual, termination. The output stage can only sink current in the PECL mode, and the amount of sink current is set by a programming resistor on the LOCK/IPRG pin. Source current is provided by the pull-up resistor that is part of the Thévenin termination.

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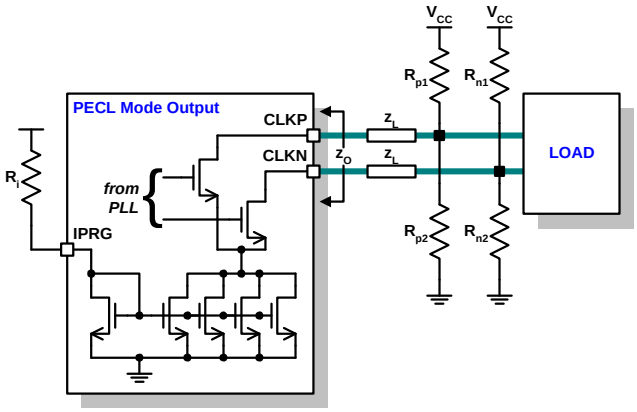

Figure 21: Thévenin Termination (PECL)

11.1.1. Example Calculation

In PECL mode, the output driver does not source current, so the V_{IH} value is determined by the ratios of the terminating resistors using the equation

$$V_{NMH} = V_{CC} \times \frac{R_{p1}}{R_{p1} + R_{p2}}$$

where R_{p1} is the pull-up resistor, R_{p2} is the pull-down resistor and V_{NMH} is the desired noise margin, and

$$V_{IH} = V_{CC} - V_{NMH}$$

The resistor ratio must also match the line impedance via the equation

$$z_L = \frac{R_{p1} R_{p2}}{R_{p1} + R_{p2}}$$

where z_L is the line impedance.

Combining these equations, and solving for R_{p1} gives

$$R_{p1} = z_L + z_L \left(\frac{V_{NMH}}{V_{CC} - V_{NMH}} \right)$$

If the load's $V_{IH(min)} = V_{CC} - 0.6$, choose a $V_{NMH} = 0.45V$. If the line impedance is 75W, then R_{p1} is about 82W. Substituting into the equation for line impedance and solving for R_{p2} gives a value of 880W (choose 910W).

To solve for the load's V_{IL}, an output sink current must be programmed via the IPRG pin. If the desired $V_{IH} = V_{CC} - 1.6$, choose $V_{CC} - 2.0$ for some extra margin. A sink current of 25mA through the 82W resistor generates a 2.05V drop. The sink current is programmed via the IPRG pin, where the ratio of IPRG current to output sink current is 1:4. An IPRG programming resistor of 750W at $V_{DD} = 5V$ generates 6.6mA, or about 27mA output sink current.

11.2 CMOS Output Mode

If a CMOS interface is desired, a transmission line is typically terminated using a series termination. Series termination adds no dc loading to the driver, and requires less power than other resistive termination methods. In addition, no extra impedance exists from the signal line to a reference voltage, such as ground.

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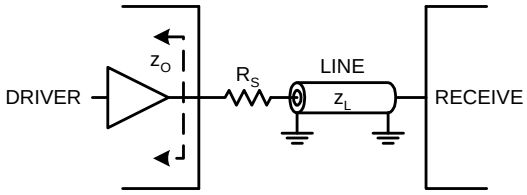

Figure 22: Series Termination (CMOS)

As shown in Figure 22, the sum of the driver's output impedance (z_O) and the series termination resistance (R_S) must equal the line impedance (z_L). That is,

$$R_S = z_L - z_O$$

When the source impedance (z_O+R_S) is matched to the line impedance, then by voltage division the incident wave amplitude is one-half of the full signal amplitude.

$$V_i = V \frac{(z_O + R_S)}{(z_O + R_S) + z_L} = \frac{V}{2}$$

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However, the full signal amplitude may take up to twice as long as the propagation delay of the line to develop, reducing noise immunity during the half-amplitude period. Note that the voltage at the receive end must add up to a signal amplitude that meets the receiver switching thresholds. The slew rate of the signal may be reduced due to the additional RC delay of the load capacitance and the line impedance. Also, note that the output driver impedance will vary slightly with the output logic state (high or low).

11.3 Serial Communications

Connection of devices to a standard-mode implementation of the I2C-bus is similar to that shown in Figure 23. Selection of the pull-up resistors (R_P) and the optional series resistors (R_S) on the SDA and SCL lines depends on the supply voltage, the bus capacitance and the number of connected devices with their associated input currents.

Control of the clock and data lines is done through open drain/collector current-sink outputs, and thus requires external pull-up resistors on both lines.

A guideline is

$$R_P < \frac{t_r}{2 \times C_{bus}}$$

where t_r is the maximum rise time (minus some margin) and C_{bus} is the total bus capacitance. Assuming an I2C controller and eight to ten other devices on the bus, including this one, results in values in the 5kW to 7kW range. Use of a series resistor to provide protection against high voltage spikes on the bus will alter the values for R_P.

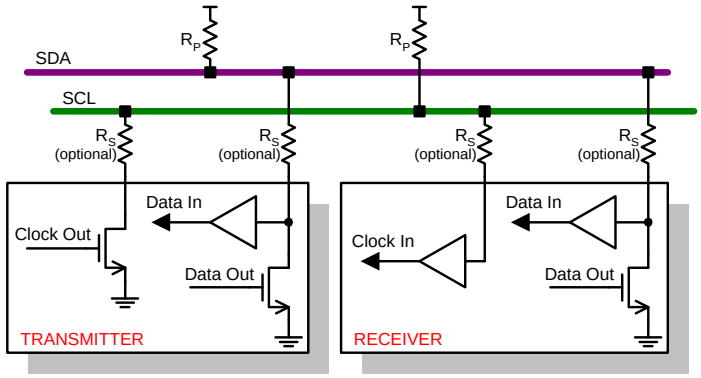

Figure 23: Connections to the Serial Bus

11.3.1. For More Information

More information on the I2C -bus can be found in the document The I2C-bus And How To Use It (Including Specifications), available from Philips Semiconductors at http://www-us2.semiconductors.philips.com.

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12.0 Device Application: Stand-Alone Clock Generation

The length of the reference and feedback dividers, their granularity and the flexibility of the post divider make the FS6131 the most flexible monolithic stand-alone PLL clock generation device available. The effective block diagram of the FS6131 when programmed for stand-alone mode is shown in Figure 24.

The source of the feedback divider in the stand-alone mode is the output of the VCO. By dividing the input reference frequency down by reference divider (N_R), then multiplying it up in the main loop through the feedback divider (N_F), and finally dividing the main loop output frequency by the post divider (N_{Px}), we have the defining relationship for this mode. The equation for the output clock frequency (f_{CLK}) can be written as

$$f_{CLK} = f_{REF}\left(\frac{N_F}{N_R}\right)\left(\frac{1}{N_{Px}}\right)$$

where the reference source frequency (f_{REF}) can be either supplied by the VCXO or applied to the REF pin.

Great flexibility is permitted in the programming of the FS6131 to achieve exact desired output frequencies since three integers are involved in the computation.

12.1 Example Calculation

A Visual BASIC program is available to completely program the FS6131 based on the given parameters.

Suppose that the reference source frequency is 14.318MHz and the desired output frequency is 100MHz.

First, factor the 14.318MHz reference frequency (which is four times the NTSC television color sub-carrier) into prime numbers. The exact expression is

$$f_{REF} = 14318181.\overline{81} = \frac{2^5 \times 3^2 \times 5^7 \times 7^1}{11}$$

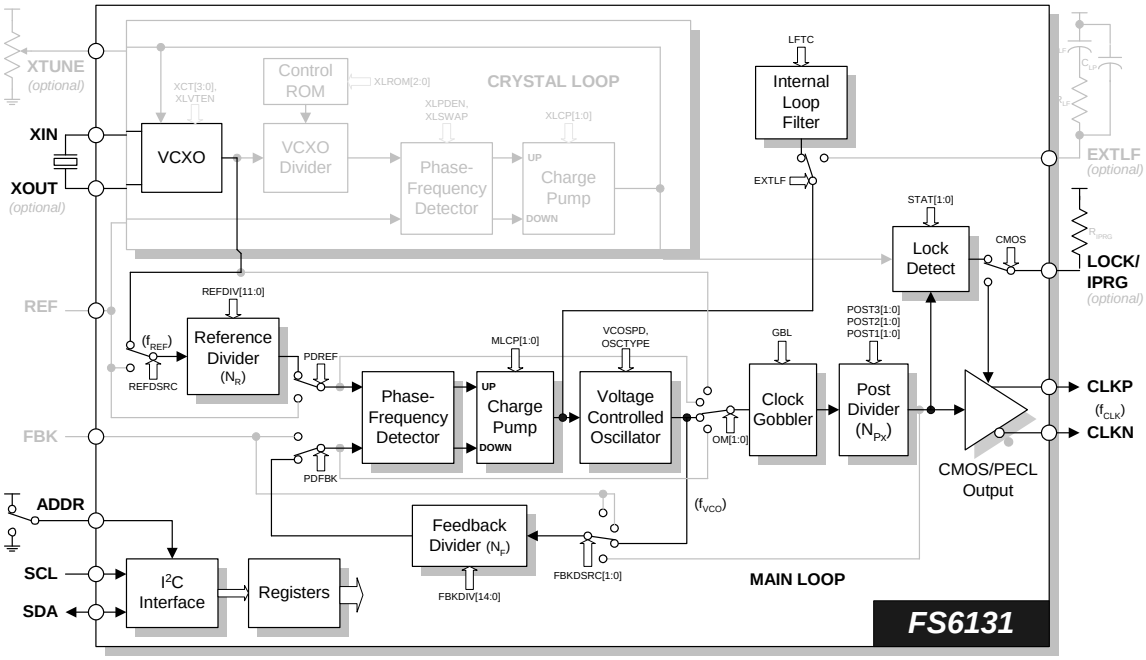

Figure 24: Block Diagram: Stand-Alone Clock Generation

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Next, express the output and input frequencies as a ratio of f_{CLK} to f_{REF}, where f_{CLK} has also been converted to a product of prime numbers.

$$\frac{f_{CLK}}{f_{REF}} = \frac{100000000.00}{14318181.\overline{81}} = \frac{\left(2^8 \times 5^8\right)}{\left(\frac{2^5 \times 3^2 \times 5^7 \times 7^1}{11}\right)}$$

Simplifying the above equation yields

$$\frac{f_{CLK}}{f_{REF}} = \frac{\left(2^3 \times 5^1 \times 11\right)}{\left(3^2 \times 7\right)}$$

Deciding how to apportion the denominator integers between the reference divider and the post divider is an iterative process. To obtain the best performance, the VCO should be operated at the highest frequency possible without exceeding its upper limit of 230MHz. (see Table 15). The VCO frequency (f_{VCO}) can be calculated by

$$f_{VCO} = f_{REF} \times \frac{N_F}{N_R}$$

Recall that the reference divider can have a value between 1 and 4096, but the post divider is limited to values derived from

$$N_{Px} = N_{P1} \times N_{P2} \times N_{P3}$$

where the values N_{P1}, N_{P2} and N_{P3} are found in Table 8.

In this example, the smallest integer that can be removed from the denominator of Eqn. 2 is three. Set the post divider at N_{Px}=3, and the ratio of f_{CLK} to f_{REF} becomes (from Eqn. 1)

$$\frac{f_{CLK}}{f_{REF}} = \frac{\left(2^3 \times 5^1 \times 11\right)}{\left(3 \times 7\right)} \times \frac{1}{3}$$

Unfortunately, a post divider modulus of three requires a VCO frequency of 300MHz, which is greater than the allowable f_{VCO} noted in Table 15. For the best PLL performance, program the post divider modulus to allow the VCO to operate at a nominal frequency that is at least 70MHz but less then 230MHz. Therefore, the reference divider cannot be reduced below the modulus of 32´7 (or 63) as shown in Eqn. 2.

However, the VCO can still be operated at a frequency higher than f_{CLK}. Multiplying both the numerator and the denominator by two does not alter the output frequency, but it does increase the VCO frequency.

$$\frac{f_{CLK}}{f_{REF}} = \frac{N_F}{N_R} \times \frac{1}{N_{Px}} = \frac{\left(2^3 \times 5^1 \times 11\right) \times 2}{\left(3^2 \times 7\right)} \times \frac{1}{2} = \frac{880}{63} \times \frac{1}{2}$$

As Eqn. 3 shows, the VCO frequency can be doubled by multiplying the feedback divider by two. Set the post divider to two to return the output frequency to the desired modulus. These divider settings place the VCO frequency at 200MHz.

12.2 Example Programming

To generate 100.000MHz from 14.318MHz, program the following (refer to Figure 24):

- Set the reference divider input to select the VCXO via REFDSRC=0
- Set the PFD input to select the reference divider and the feedback divider via PDREF=0 and PDFBK=0
- Set the reference divider (N_R) to a modulus of 63 via REFDIV[11:0]
- Set the feedback divider input to select the VCO via FBKDSRC=1
- Set the feedback divider (N_F) to a modulus of 880 via FBKDIV[14:0]
- Set N_{P1}=2, N_{P2}=1 and N_{P3}=1 for a combined post divider modulus of N_{Px}=2 via POST1[1:0], POST2[1:0] and POST3[1:0].
- Select the internal loop filter via EXTLF=0
- Set XLVTEN=0 and XLPDEN=1 to disable the VCXO fine tune and the crystal loop phase frequency detector
- Set VCOSPD=0 to select the VCO high speed range

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13.0 Device Application: Line-Locked Clock Generation

Line-locked clock generation, as used here, refers to the process of synthesizing a clock frequency that is some integer multiple of the horizontal line frequency in a graphics system. The FS6131 is easily configured to perform that function, as shown in Figure 25.

A line reference signal (f_{HSYNC}) is applied to the REF input for direct application to the main loop PFD. The feedback divider (N_F) is programmed for the desired number of output clocks per line.

The source for the feedback divider is selected to be the output of the post divider (N_{Px}) so that the edges of the output clock maintain a consistent phase alignment with the line reference signal. The modulus of the post divider should be selected to maintain a VCO frequency that is comfortably within the operating range noted in Table 15.

13.1 Example Calculation

A Visual BASIC program is available to completely program the FS6131 based on the given parameters.

Suppose that we wish to reconstruct the pixel clock from a VGA source. This is a typical requirement of an LCD projection panel application.

First, establish the total number of pixel clocks desired between horizontal sync (HSYNC) pulses. The number of pixel clocks is known as the horizontal total, and the feedback divider is programmed to that value. In this example, choose the horizontal total to be 800.

Next, establish the frequency of the HSYNC pulses (f_{HSYNC}) on the line reference signal for the video mode. In this case, let f_{HSYNC}=31.5kHz. The output clock frequency f_{CLK} is calculated to be:

$$f_{CLK} = f_{HSYNC} \times N_F = 31.5\text{kHz} \times 800 = 25.175\text{MHz}$$

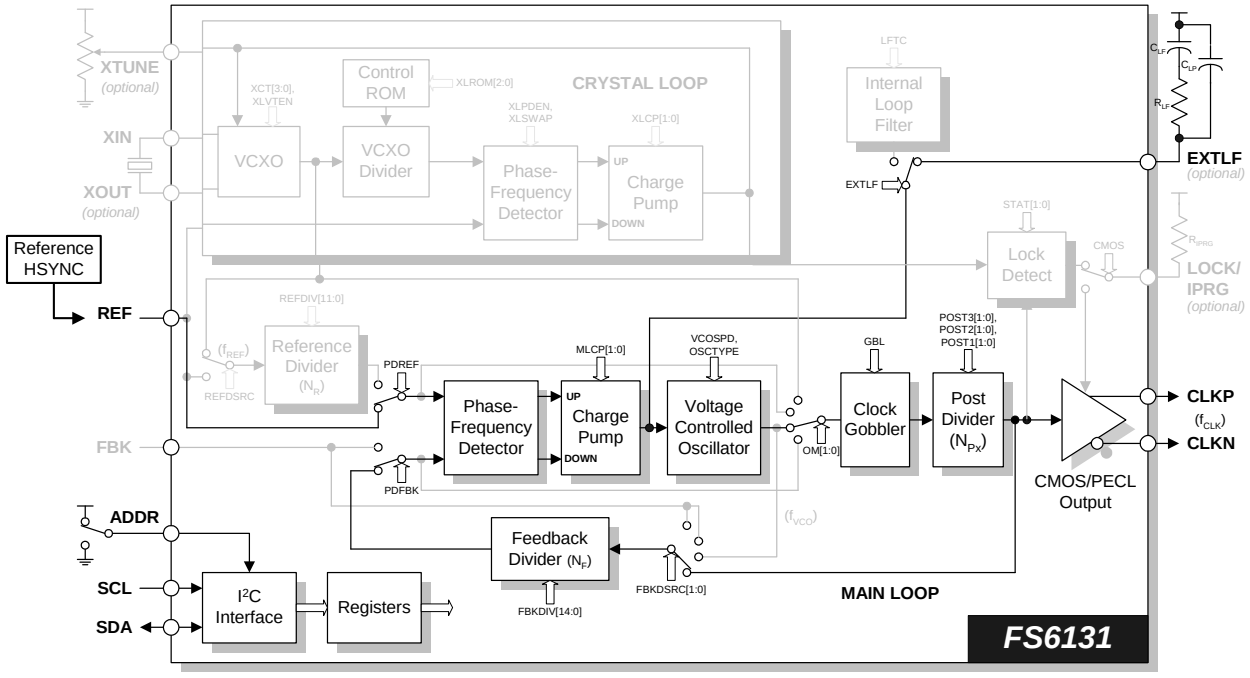

Figure 25: Block Diagram: Line-Locked Clock Generation

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However, the 31.5kHz line reference signal is too low in frequency for the internal loop filter to be used. A series combination of a 0.015mF capacitor and a 15kW resistor from power (V_{DD}) to the EXTLF pin provides an external loop filter. A 100pF to 220pF capacitor in parallel with the combination may improve the filter performance.

For the best PLL performance, program the post divider modulus to allow the VCO to operate at a nominal frequency that is at least 70MHz but less than 230MHz. The VCO frequency (f_{VCO}) can be calculated by

$$f_{VCO} = f_{HSYNC} \times N_F \times N_{Px}$$

Setting the post divider equal to four (N_{Px}=4) is a reasonable solution, although there are a number of values that will work. Try to keep

$$N_F \times N_{Px} < 5000$$

to avoid divider values from becoming too large. These settings place the VCO frequency at about 100MHz.

Calculate the ideal charge pump current (I_{pump}) as

$$I_{pump} = \sqrt{\frac{f_{HSYNC}}{15kHz}} \times \frac{2 N_F N_{Px}}{R_{lf}^2 C_{lf} A_{VCO}}$$

where R_{lf} is the external loop filter series resistor, C_{lf} is the external loop filter series capacitor and A_{VCO} is the VCO gain. The VCO gain is either:

A_{VCO}=125MHz/V if the high range is selected, or
A_{VCO}=75MHz/V if the low range is selected.

See Table 15 for more information on the VCO range. With f_{hsync}=31.5kHz, C_{lf}=0.015mF, R_{lf}=15kW, N_F=800, N_{Px}=4, and A_{VCO}=125MHz/V, the charge pump current is 39.3mA. A 220pF cap across the entire loop filter is also helpful.

13.2 Example Programming

To generate 800 pixel clocks between HSYNC pulses occurring on the line reference signal every 31.5kHz, program the following (refer to Figure 26):

- Clear the OSCTYPE bit to 0
- Turn off the crystal oscillator via XLROM=7
- Set the PFD inputs to select the REF pin and the feedback divider via PDREF=1 and PDFBK=0
- Set the feedback divider input to select the post divider via FBKDSRC=0
- Set the feedback divider (N_F) to a modulus of 800 (the desired number of pixel clocks per line) via FBKDIV[14:0]
- Set N_{P1}=4, N_{P2}=1 and N_{P3}=1 for a combined post divider modulus of N_{Px}=4 via POST1[1:0], POST2[1:0] and POST3[1:0].
- Select the external loop filter via EXTLF=1
- Set XLVTEN=0 and XLPDEN=1 to disable the VCXO fine tune and the crystal loop phase frequency detector
- Set VCOSPD=1 to select the VCO low speed range
- Set MLCP[1:0] to 3 to select the 32mA range

The output clock frequency f_{CLK} is 25.175MHz, with an internal VCO frequency of 100.8MHz. Note that the crystal loop was unused in this application.

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14.0 Device Application: Genlocking

Genlocking refers to the process of synchronizing the horizontal sync pulses (HSYNC) of a target graphics system to the HSYNC of a source graphics system. In a genlocked mode, the FS6131 increases (or decreases) the frequency of the VCO until the FBK input is frequency matched and phase-aligned to the frequency applied to the REF input. Since the feedback divider is within the graphics system and the graphics system is the source of the signal applied to the FBK input of the FS6131, the graphics system is effectively synchronized to the REF input as shown in Figure 26.

To configure the FS6131 for genlocking, the REF input (pin 12) and the FBK input (pin 13) are switched directly onto the feedback input of the PFD. The reference and feedback dividers are not used.

The output clock frequency is:

$$f_{CLK} = f_{HSYNC} \times horizontal\ total$$

The only remaining task is to select a post divider modulus (N_{Px}) that allows the VCO frequency to be within its nominal range.

14.1 Example Calculation

A Visual BASIC program is available to completely program the FS6131 based on the given parameters.

The FS6131 is being used to genlock an LCD projection panel system to a VGA card-generated HSYNC. The total number of pixel clocks generated by the VGA card, known as the horizontal total, are 800. Therefore, the LCD panel graphics system that is clocked by the FS6131 is set to divide the output clock frequency (f_{CLK}) by 800. The input HSYNC reference frequency (f_{HSYNC}) is 15kHz.

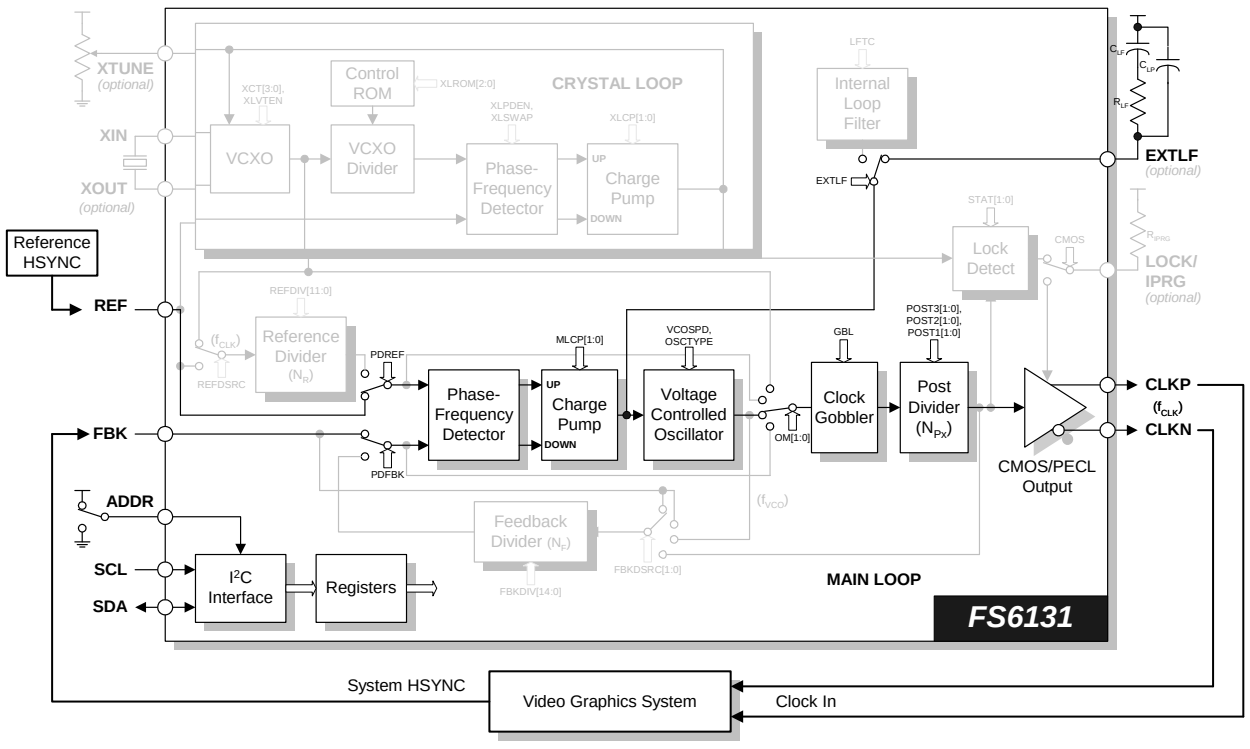

Figure 26: Block Diagram: Genlocking

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The output clock frequency is calculated as

$$f_{CLK} = 15\text{kHz} \times 800 = 12.0\text{MHz}$$

For best performance, program the post divider (N_{Px}) modulus to allow the VCO to operate at a nominal frequency that is at least 70MHz but less than 230MHz. The VCO frequency (f_{VCO}) can be calculated by

$$f_{VCO} = f_{CLK} N_{Px}$$

Selecting the post divider modulus of N_{Px}=6 is a reasonable solution, although there are a number of values that will work. Try to keep

$$N_F \times N_{Px} < 5000$$

to avoid divider values from becoming too large. The settings place the VCO frequency at about 72MHz.

Calculate the ideal charge pump current (I_{pump}) as

$$I_{pump} = \sqrt{\frac{f_{HSYNC}}{15kHz}} \times \frac{2 N_F N_{Px}}{R_{lf}^2 C_{lf} A_{VCO}}$$

where R_{lf} is the external loop filter series resistor, C_{lf} is the external loop filter series capacitor and A_{VCO} is the VCO gain. The VCO gain is either

A_{VCO}=125MHz/V if the high range is selected, or
A_{VCO}=75MHz/V if the low range is selected.

See Table 15 for more information on the VCO range. With f_{hsync}=15kHz, C_{lf}=0.015mF, R_{lf}=15kW, N_F=800, N_{Px}=6, and A_{VCO}=125MHz/V, the charge pump current is 24mA. A 220pF cap across the entire loop filter is also helpful.

14.2 Example Programming

To generate 800 pixel clocks between HSYNC pulses occurring on the line reference signal every 15kHz, program the following (refer to Figure 26):

- Clear the OSCTYPE bit to 0
- Turn off the crystal oscillator via XLROM=7
- Set the PFD inputs to select the REF and FBK pins via PDREF=1 and PDFBK=1
- Set N_{P1}=2, N_{P2}=3 and N_{P3}=1 for a combined post divider modulus of N_{Px}=6 via POST1[1:0], POST2[1:0] and POST3[1:0].
- Select the external loop filter via EXTLF=1
- Set XLVTEN=0 and XLPDEN=1 to disable the VCXO fine tune and the crystal loop phase frequency detector
- Set VCOSPD=1 to select the VCO low speed range
- Set MLCP[1:0] to 3 to select the 32mA range

The output clock frequency f_{CLK} is 12MHz, with an internal VCO frequency of 72MHz. Note that the crystal loop was unused in this application.

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15.0 Device Application: Telecom Clock Regenerator

The FS6131 can be used as a clock regenerator as shown in Figure 28. This mode uses the VCXO in its own phase-locked loop, referred to as the crystal loop. The VCXO provides a "de-jittered" multiple of the reference frequency at the REF pin (usually 8kHz in telecom applications) for use by the main loop. In essence, the crystal loop "cleans up" the reference signal for the main loop.

The control ROM for the VCXO divider is preloaded with the most common ratios to permit locking of most standard telecommunications crystals to an 8kHz signal applied to the REF pin. The de-jittered multiple of the reference frequency from the VCXO is then supplied to the reference divider in the main loop. The reference divider, along with the feedback divider, can be programmed to achieve the desired output clock frequency.

15.1 Example Calculation

A Visual BASIC program is available to completely program the FS6131 based on the given parameters.

In this example, an 8kHz reference frequency is supplied to the FS6131 and an output clock frequency of 51.84MHz is desired.

First, select the frequency at which the VCXO will operate from Table 10. The table shows the external crystal frequency options available to choose from, since the VCXO runs at the crystal frequency. While the main loop can be programmed to work with any of the frequencies in the table, the best performance will be achieved with the highest frequency at the main loop PFD.

The frequency at the main loop PFD (f_{MLpfd}) is the VCXO frequency (f_{VCXO}) divided by the main loop reference divider (N_R).

$$f_{MLpfd} = \frac{f_{VCXO}}{N_R}$$

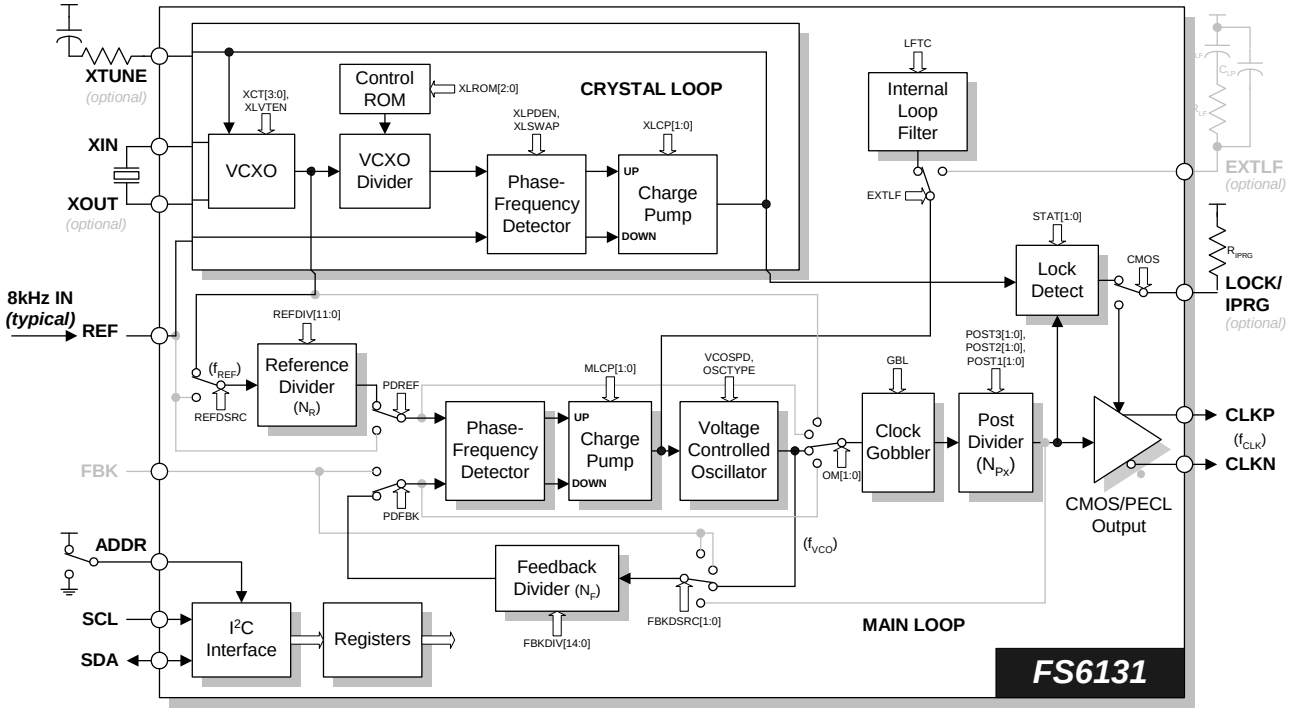

Figure 27: Block Diagram: Telecom Clock Generator

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The goal is to choose the highest crystal frequency from Table 10 that generates the smallest value of N_R.

The equation establishing the output frequency (f_{CLK}) as a function of the input VCXO frequency is

$$\frac{f_{CLK}}{f_{VCXO}} = \frac{N_F}{N_R}$$

where N_F is the feedback divider modulus.

Choose a few different crystal frequencies from Table 10 and factor both the input VCXO and output clock frequencies into prime numbers. Look for the factors that will give the smallest modulus for N_R with the largest F_{VCXO}. The output and VCXO frequencies and the reduced factors from Eqn. 1 are in Table 22.

Table 22: Clock Regenerator Example

VCXO Frequency From Table 10 (f_{VCXO}, MHz)	$\frac{f_{CLK}}{f_{VCXO}}$	$\frac{N_F}{N_R}$
20.00	$\frac{51840000}{20000000}$	$\frac{324}{125}$
19.44	$\frac{51840000}{19440000}$	$\frac{8}{3}$
25.248	$\frac{51840000}{25248000}$	$\frac{540}{263}$
24.576	$\frac{51840000}{24576000}$	$\frac{135}{64}$

A 19.44MHz crystal provides the smallest modulus for N_R (N_R=3) with the highest crystal frequency.

Finally, choose a post divider (N_{Px}) modulus that keeps the VCO frequency in its most comfortable range. The VCO frequency (f_{VCO}) can be calculated by

$$f_{VCO} = f_{CLK} N_{Px}$$

Selecting an overall modulus of N_{Px}=3 sets the VCO frequency at 155.52MHz when the loop is locked.

15.2 Example Programming

To generate a de-jittered output frequency of 51.84MHz from an 8kHz reference, program the following (refer to Figure 27):
- Program the VCXO control ROM to 3 via XLROM[2:0] to select an external 19.44MHz crystal
- Enable the VCXO fine tune via XLVTEN=1
- Enable the crystal loop PFD via XLPDEN=0 and XLSWAP=0
- Set the reference divider input to select the VCXO via REFDSRC
- Set the PFD input to select the reference divider and the feedback divider via PDREF and PDFBK
- Set the reference divider (N_R) to a modulus of 3 via REFDIV[11:0]
- Set the feedback divider input to select the VCO via FBKDSRC
- Set the feedback divider (N_F) to a modulus of 8 via FBKDIV[14:0]
- Set N_{P1}=1, N_{P2}=3 and N_{P3}=1 for a combined post divider modulus of N_{Px}=3 via POST1[1:0], POST2[1:0] and POST3[1:0].
- Select the internal loop filter via EXTLF
- Set VCOSPD=0 to select the VCO high speed range

These settings provide the highest frequency at the main loop phase frequency detector of 6.48MHz. The use of a 19.44MHz crystal requires that XLROM[2:0] be set to three as shown in Table 10.

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16.0 Revision History

Revision	Date	Modification
3	January 2008	Moving into new AMIS template
4	May 2008	Moving into ON Semiconductor template

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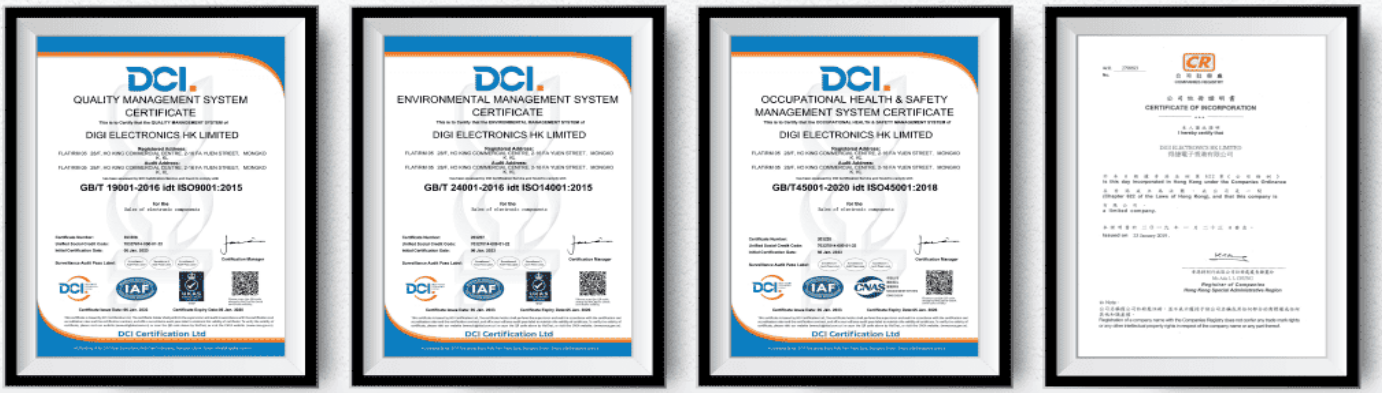

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