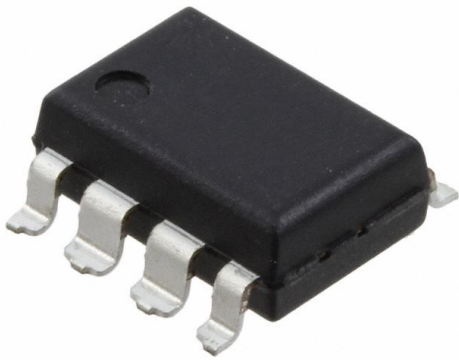


# FSDH321L Datasheet

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DiGi Electronics Part Number	FSDH321L-DG
Manufacturer	<a href="#">onsemi</a>
Manufacturer Product Number	FSDH321L
Description	IC OFFLINE SWITCH FLYBACK 8LSOP
Detailed Description	Converter Offline Flyback Topology 100kHz 8-LSOP

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## Purchase and inquiry

Manufacturer Product Number:

FSDH321L

Series:

FPS™

Output Isolation:

Isolated

Voltage - Breakdown:

650V

Voltage - Start Up:

12 V

Duty Cycle:

67%

Power (Watts):

17 W

Control Features:

-

Package / Case:

8-SMD, Gull Wing

Mounting Type:

Surface Mount

Manufacturer:

onsemi

Product Status:

Obsolete

Internal Switch(s):

Yes

Topology:

Flyback

Voltage - Supply (Vcc/Vdd):

8V ~ 20V

Frequency - Switching:

100kHz

Fault Protection:

Current Limiting, Over Load, Over Temperature, Over Voltage

Operating Temperature:

-25°C ~ 85°C (TA)

Supplier Device Package:

8-LSOP

Base Product Number:

FSDH321

## Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001



### Internal Block Diagram

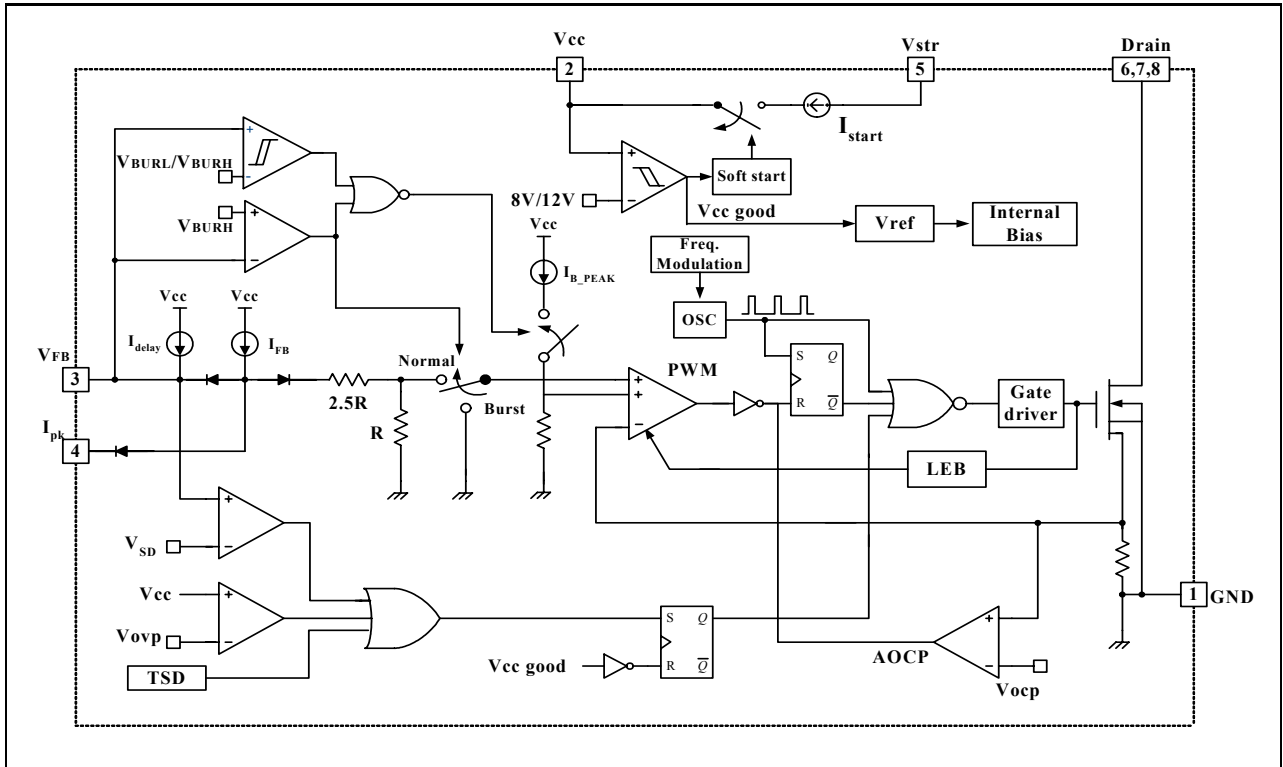


Figure 2. Functional Block Diagram of FSDx321

## Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging between 3V and 6V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	l <sub>pk</sub>	Pin to adjust the current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the current limit. If this pin is tied to Vcc or left floating, the typical current limit will be 0.7A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is disabled.
6, 7, 8	Drain	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance.

## Pin Configuration

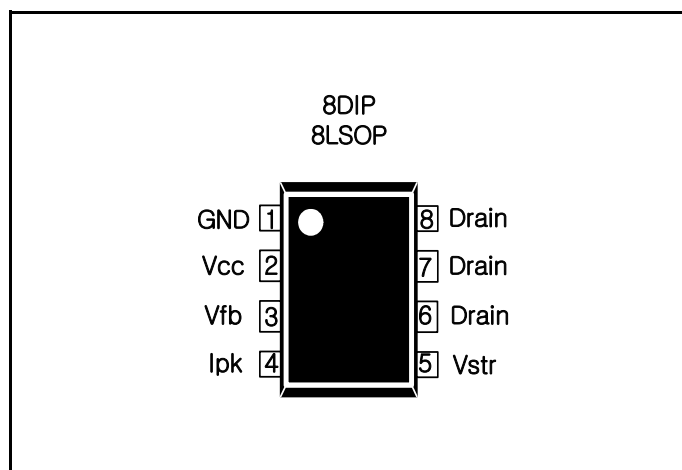


Figure 3. Pin Configuration (Top View)

FSDH321, FSDL321

## Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Vstr Pin Voltage	VSTR,MAX	650	V
Maximum Drain Pin Voltage	VDRAIN,MAX	650	V
Drain-Gate Voltage (RGS=1MΩ)	VDGR	650	V
Gate-Source (GND) Voltage	VGS	±20	V
Drain Current Pulsed <sup>(1)</sup>	IDM	1.5	ADC
Continuous Drain Current (Tc=25°C)	ID	0.7	ADC
Continuous Drain Current (Tc=100°C)	ID	0.32	ADC
Single Pulsed Avalanche Energy <sup>(2)</sup>	EAS	10	mJ
Maximum Supply Voltage	VCC,MAX	20	V
Input Voltage Range	VFB	-0.3 to VCC	V
Total Power Dissipation	PD	1.40	W
Operating Junction Temperature.	TJ	Internally limited	°C
Operating Ambient Temperature.	TA	-25 to +85	°C
Storage Temperature Range.	TSTG	-55 to +150	°C

### Note:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L = 24mH, starting Tj = 25°C

## Thermal Impedance

Parameter	Symbol	Value	Unit
<b>8DIP</b>			
Junction-to-Ambient Thermal	$\theta_{JA}^{(1)}$	88.84 <sup>(3)</sup>	°C/W
Junction-to-Case Thermal	$\theta_{JC}^{(2)}$	13.94	°C/W

### Note:

1. Free standing without heatsink.
  2. Measured on the Drain pin close to plastic interface.
  3. Without copper clad.
- \* - all items are tested with the standard JESD 51-10(DIP)

## Electrical Characteristics (Sense FET Part)

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Sense FET SECTION</b>						
Zero Gate Voltage Drain Current	IDSS	VDS=Max. Rating, VGS=0V	-	-	25	μA
		VDS=0.8Max. Rating, VGS=0V, TC=125°C	-	-	200	μA
Static Drain-Source on Resistance (Note)	RDS(ON)	VGS=10V, ID=0.5A	-	14	19	Ω
Forward Trans conductance (Note)	gfs	VDS=50V, ID=0.5A	1.0	1.3	-	S
Input Capacitance	CISS	VGS=0V, VDS=25V, f=1MHz	-	162	-	pF
Output Capacitance	COSS		-	18	-	
Reverse Transfer Capacitance	CRSS		-	3.8	-	
Turn on Delay Time	td(on)	VDD=0.5B VDSS, ID=1.0A (MOSFET switching time is essentially independent of operating temperature)	-	9.5	-	ns
Rise Time	tr		-	19	-	
Turn Off Delay Time	td(off)		-	33	-	
Fall Time	tf		-	42	-	
Total Gate Charge (Gate-Source + Gate-Drain)	Qg	VGS=10V, ID=1.0A, VDS=0.5B VDSS (MOSFET switching time is essentially independent of operating temperature)	-	7.0	-	nC
Gate-Source Charge	Qgs		-	3.1	-	
Gate-Drain (Miller) Charge	Qgd		-	0.4	-	

**Note:**

1. Pulse test: Pulse width ≤ 300μS, duty ≤ 2%

2.  $S = \frac{1}{R}$

FSDH321, FSDL321

**Electrical Characteristics (Control Part)** (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>UVLO SECTION</b>						
Start Threshold Voltage	VSTART	VFB=GND	11	12	13	V
Stop Threshold Voltage	VSTOP	VFB=GND	7	8	9	V
<b>OSCILLATOR SECTION</b>						
Initial Accuracy	FOSC	<b>FSDH321</b>	90	100	110	kHz
Frequency Modulation	FMOD		±2.5	±3	±3.5	
Initial Accuracy	FOSC	<b>FSDL321</b>	45	50	55	kHz
Frequency Modulation	FMOD		±1.0	±1.5	±2.0	
Frequency Change With Temperature <sup>(2)</sup>	ΔF/ΔT	-25°C ≤ Ta ≤ +85°C	-	±5	±10	%
Maximum Duty Cycle	Dmax	<b>FSDH321</b>	62	67	72	%
		<b>FSDL321</b>	71	77	83	%
<b>FEEDBACK SECTION</b>						
Feedback Source Current	IFB	Ta=25°C, Vfb = 0V	0.70	0.90	1.1	mA
Shutdown Feedback Voltage	VSD		5.5	6.0	6.5	V
Shutdown Delay Current	IDELAY	Ta=25°C, Vfb = 4V	3.5	5.0	6.5	μA
<b>BURST MODE SECTION</b>						
Burst Mode Voltage	VBURH	Tj = 25°C	0.4	0.5	0.6	V
	VBURL		0.25	0.35	0.45	V
	Hysteresis		-	150	-	mV
<b>CURRENT LIMIT(SELF-PROTECTION)SECTION</b>						
Peak Current Limit <sup>(3)</sup>	ILIM	Tj = 25°C	0.60	0.70	0.80	A
Current Limit Delay <sup>(1)</sup>	TCLD	Tj = 25°C	-	600	-	ns
<b>SOFT START SECTION</b>						
Soft Start Time	TSS	Vfb = 4V	10	15	20	ms
<b>PROTECTION SECTION</b>						
Thermal Shutdown Temperature <sup>(1)</sup>	TSD	-	125	145	-	°C
Over Voltage Protection	VOVP		18	19	20	V
<b>TOTAL STANDBY CURRENT SECTION</b>						
Startup Charging Current	ICH	VCC=0V	0.7	0.85	1.0	mA
Operating Supply Current (Control Part Only)	IOP	VCC = 14V, Vfb = 0V	1	3	5	mA

**Note:**

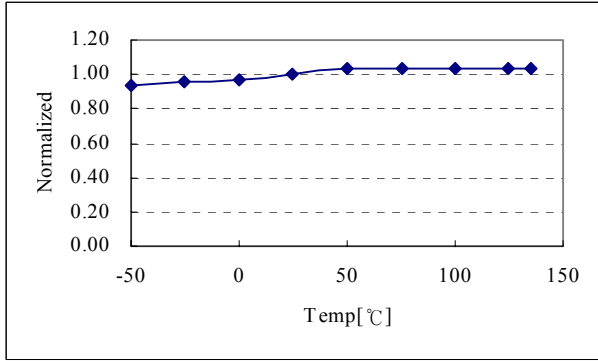
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. di/dt = 250mA/μS

## Comparison Between FSDM311 and FSDx321

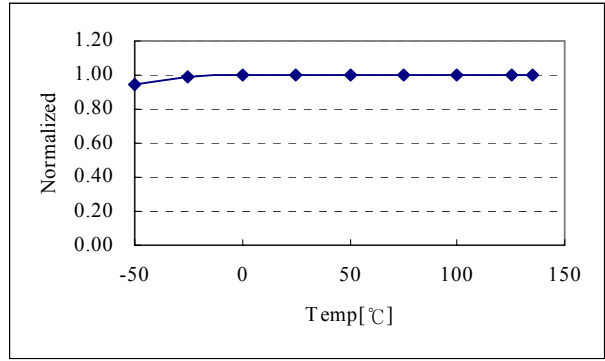
Function	FSDM311	FSDx321	FSDx321 Advantages
Soft-Start	15mS	15mS	<ul style="list-style-type: none"> <li>• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses</li> <li>• Eliminates external components used for soft-start in most applications</li> <li>• Reduces or eliminates output overshoot</li> </ul>
External Current Limit	not applicable	Programmable of default current limit	<ul style="list-style-type: none"> <li>• Smaller transformer</li> <li>• Allows power limiting (constant over-load power)</li> <li>• Allows use of larger device for lower losses and higher efficiency.</li> </ul>
Frequency Modulation	not applicable	$\pm 1.5\text{KHz @}50\text{KHz}$ $\pm 3.0\text{KHz @}100\text{KHz}$	<ul style="list-style-type: none"> <li>• Reduced conducted EMI</li> </ul>
Burst Mode Operation	Yes-built into controller	Yes-built into controller	<ul style="list-style-type: none"> <li>• Improve light load efficiency</li> <li>• Reduces no-load consumption</li> <li>• Transformer audible noise reduction</li> </ul>
Drain Creepage at Package	7.62mm	7.62mm	<ul style="list-style-type: none"> <li>• Greater immunity to arcing as a result of build-up of dust, debris and other contaminants</li> </ul>

### Typical Performance Characteristics (Control Part)

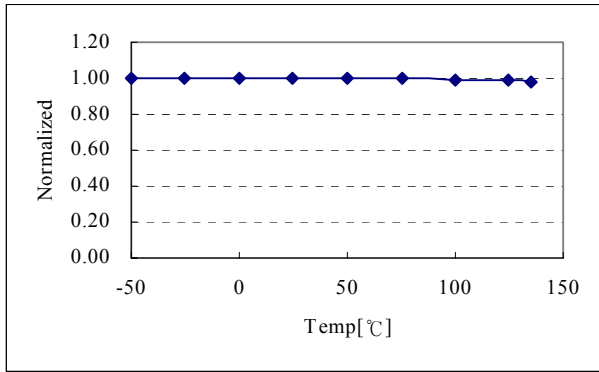
(These characteristic graphs are normalized at Ta = 25°C)



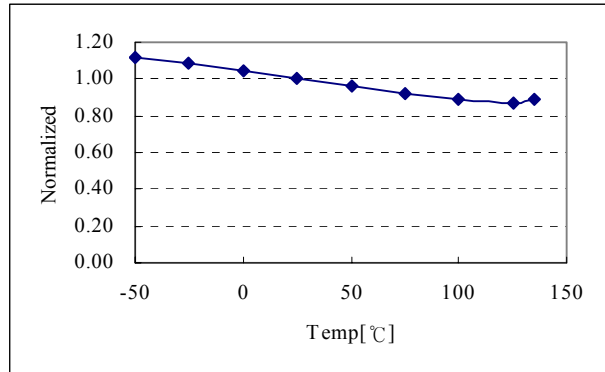
Operating Frequency (Fosc)



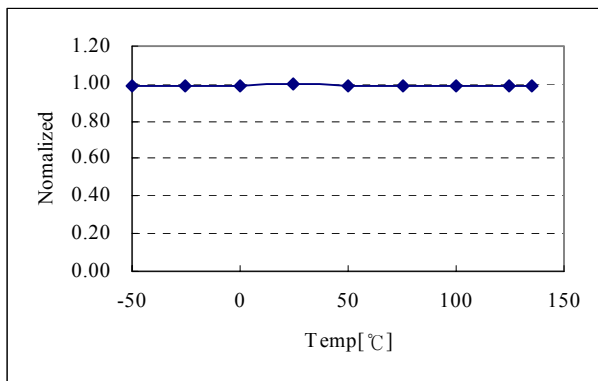
Frequency Modulation (Fmod)



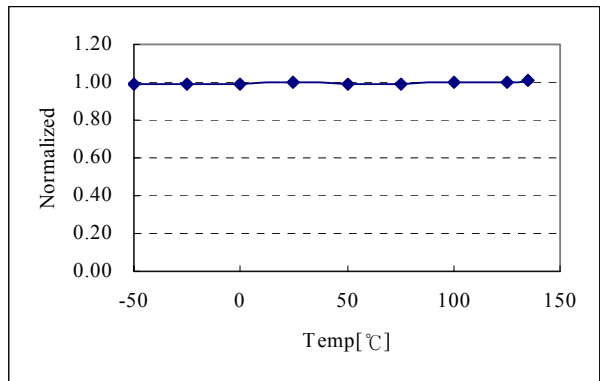
Maximum duty cycle (Dmax)



Operating supply current (Iop)

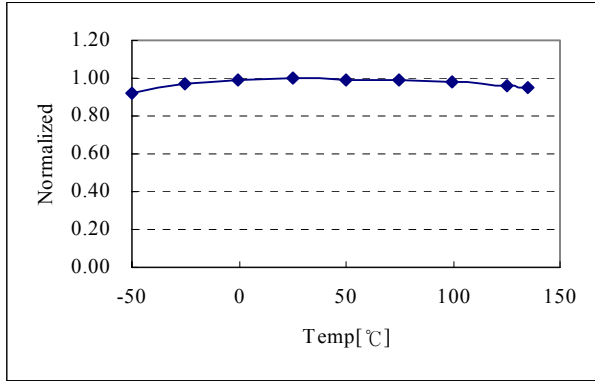


Start Threshold Voltage (Vstart)

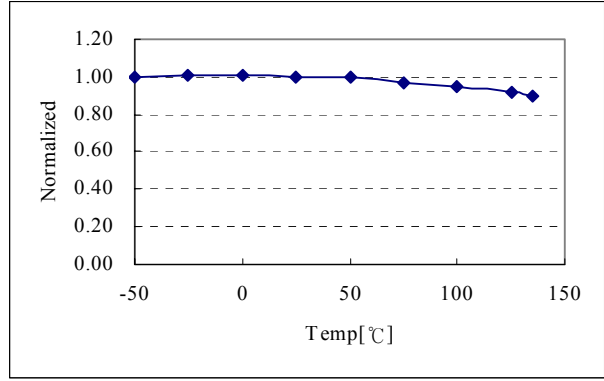


Stop Threshold Voltage (Vstop)

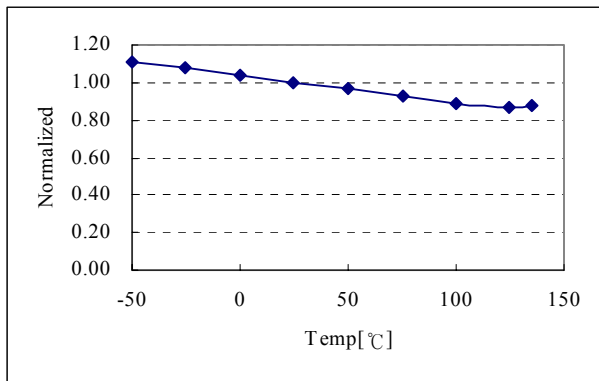
**Typical Performance Characteristics** (Continued)



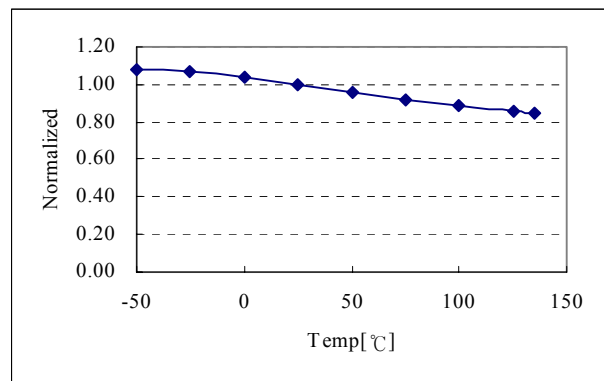
**Feedback Source Current ( $I_{fb}$ )**



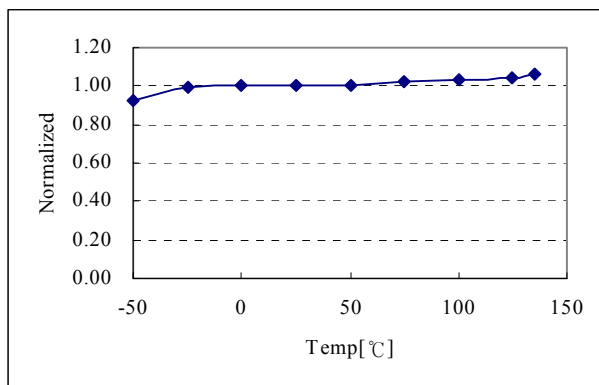
**Peak current limit ( $I_{LIM}$ )**



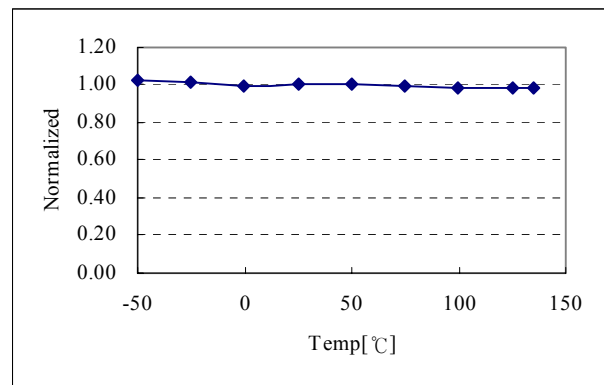
**Start up Current ( $I_{start}$ )**



**Startup Charging Current ( $I_{ch}$ )**



**Burst peak current ( $I_{burst}$ )**



**Over Voltage Protection ( $V_{ovp}$ )**



Cfb from 3V to 6V with 5uA.

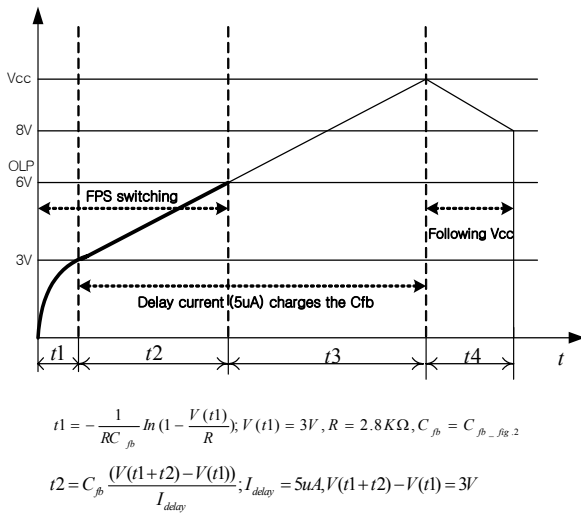


Figure 6. Over load protection

**4.2 Thermal Shutdown (TSD) :** The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

**4.3 Abnormal Over Current Protection (AOCP) :**

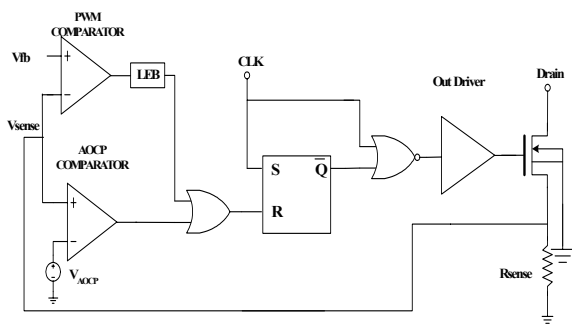


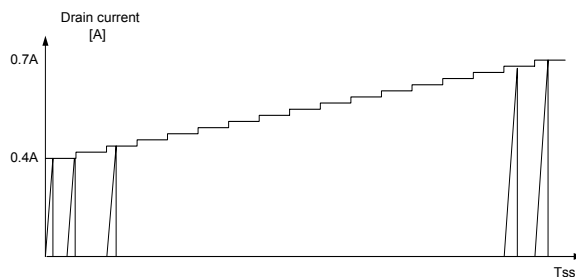
Figure 7. AOCP Function & Block

Even though the FPS<sup>TM</sup> has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPS<sup>TM</sup> when a secondary side diode short or a transformer pin short occurs. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The FPS<sup>TM</sup> has an internal AOCP (Abnormal Over Current Pro-

tection) circuit as shown in figure 7. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse by pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse by pulse AOCP stops Sense FET within 350ns after it is activated.

**4.4 Over Voltage Protection (OVP) :** In case of malfunction in the secondary side feedback circuit, or feedback loop open caused by a defect of solder, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPS<sup>TM</sup> uses Vcc instead of directly monitoring the output voltage. If Vcc exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19V.

**5. Soft Start :** The FPS<sup>TM</sup> has an internal soft start circuit that increases the feedback voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, as shown in figure 8, where progressive increments of Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.



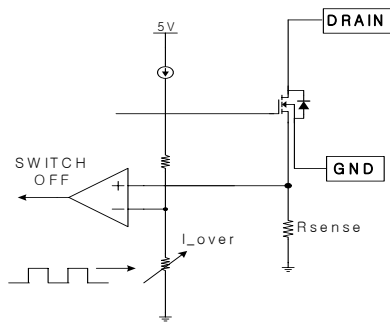


Figure 8. Soft Start Function

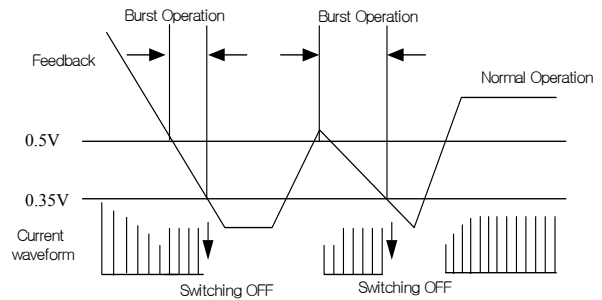


Figure 10. Circuit for Burst Operation

**6. Burst operation :** In order to minimize power dissipation in standby mode, the FPS™ enters burst mode operation.

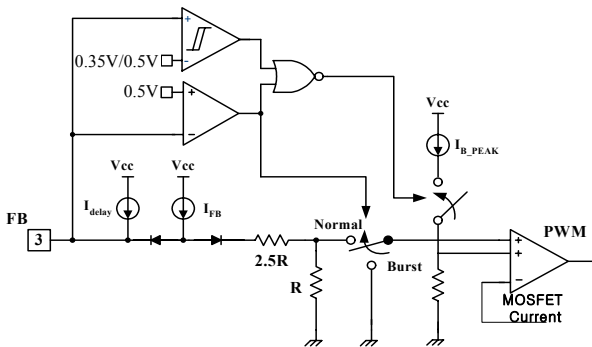


Figure 9. Circuit for Burst operation

As the load decreases, the feedback voltage decreases. As shown in figure 10, the device automatically enters burst mode when the feedback voltage drops below  $V_{BURH}$ (500mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by  $V_{fb} = V_{BURH}$  and therefore,  $V_{fb}$  is driven down further. Switching continues until the feedback voltage drops below  $V_{BURL}$ (350mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes  $V_{BURH}$ (500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

**7. Frequency Modulation :** EMI reduction can be accomplished by modulating the switching frequency of a switched power supply. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the band width measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 11, the frequency changes from 97KHz to 100KHz (from 48.5KHz to 51.5KHz for FSDL321)in 4mS for the FSDH321. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

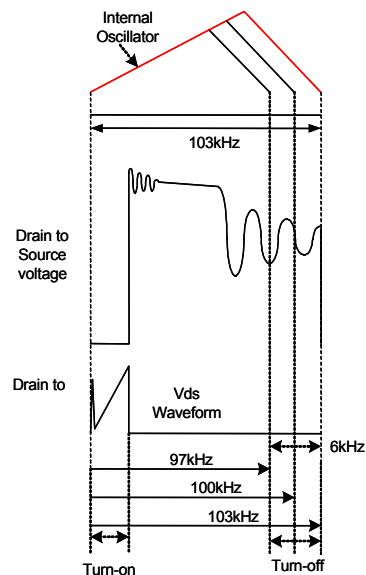
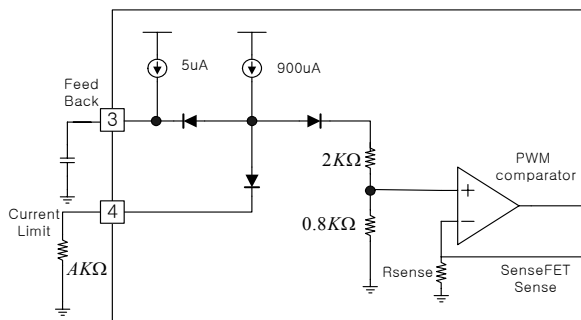


Figure 11. Frequency Modulation Waveform for FSDH321

**8. Adjusting Current limit function:** As shown in fig 12, a combined  $2.8\text{k}\Omega$  internal resistance is connected into the non-inverting lead on the PWM comparator. A external resistance of A on the current limit pin forms a parallel resistance with the  $2.8\text{k}\Omega$  when the internal diodes are biased by the main current source of  $900\mu\text{A}$ .



**Figure 12. Peak current adjustment**

For example, FSDH321 has a typical Sense FET current limit ( $I_{LIM}$ ) of  $0.7\text{A}$ . The Sense FET current can be limited to  $0.5$  by inserting a  $7\text{k}\Omega$  between the current limit pin and ground which is derived from the following equations:

$$0.7 : 0.5 = 2.8\text{k}\Omega : X\text{k}\Omega ,$$

$$X = 2\text{k}\Omega$$

Since X represents the resistance of the parallel network, A can be calculated using the following equation:

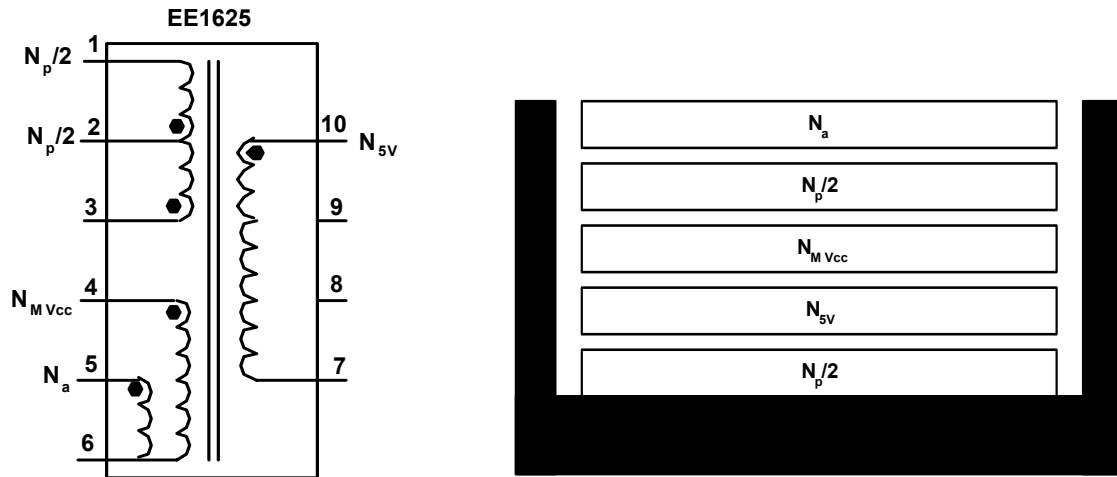
$$A = X / (1 - (X/2.8\text{k}\Omega))$$

## Layout Considerations



## 2. Transformer Specification (10W Output Power)

### 1. Schematic Diagram



### 2. Winding Specification

	Pin ( S → F )	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.15 \phi \times 1$	80	Solenoid winding
Insulation : Polyester Tape $t = 0.050\text{mm}$ , 3Layers				
$N_{5V}$	10 → 7	$0.55 \phi \times 1$	12	Solenoid winding
Insulation : Polyester Tape $t = 0.050\text{mm}$ , 3Layers				
$N_{MVCC}$	4 → 6	$0.20 \phi \times 1$	40	Solenoid winding
Insulation : Polyester Tape $t = 0.050\text{mm}$ , 3Layers				
$N_p/2$	2 → 1	$0.15 \phi \times 1$	80	Solenoid winding
Insulation : Polyester Tape $t = 0.050\text{mm}$ , 3Layers				
$N_a$	5 → 6	$0.20 \phi \times 1$	34	Solenoid winding
Outer Insulation : Polyester Tape $t = 0.050\text{mm}$ , 3Layers				

### 3. Electric Specification and Core and Bobbin

	Pin	Spec.	Remark
Inductance	1 – 3	1.8 mH	1kHz, 1V
Leakage	1 – 3	100uH	2nd side all short
Core		EE1625	
Bobbin		EE1625	

FSDH321, FSDL321

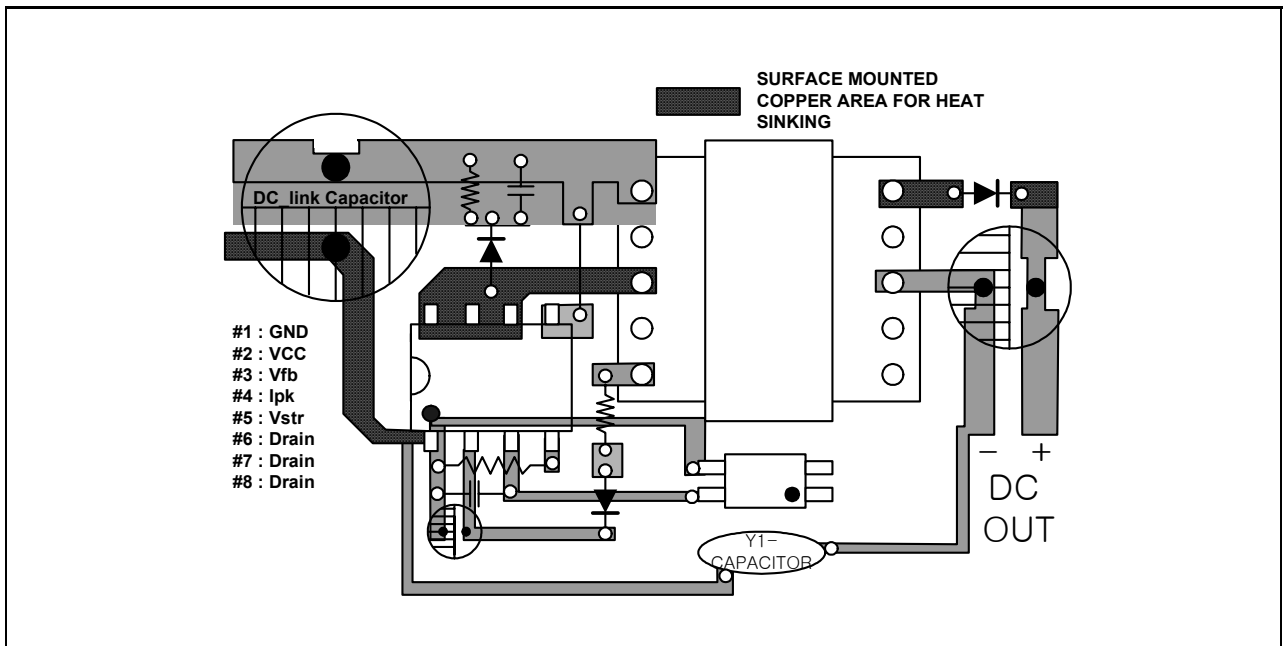
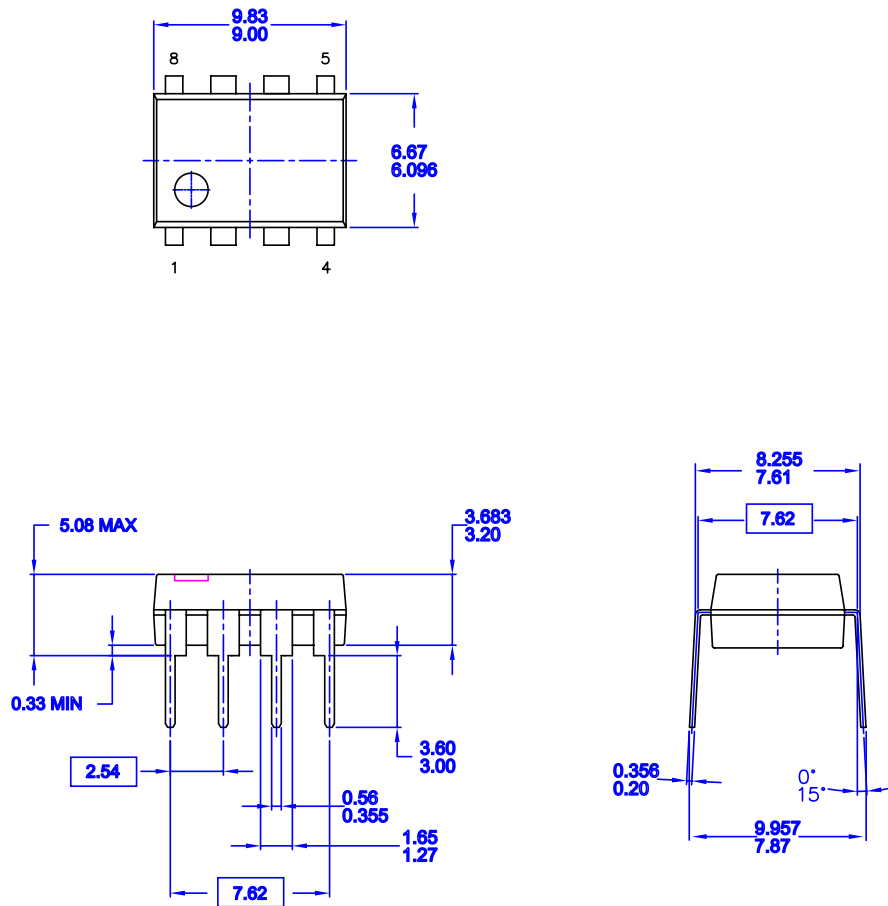


Figure 13. Layout Considerations for FSDx321 using 8DIP

## Package Dimensions

### 8DIP

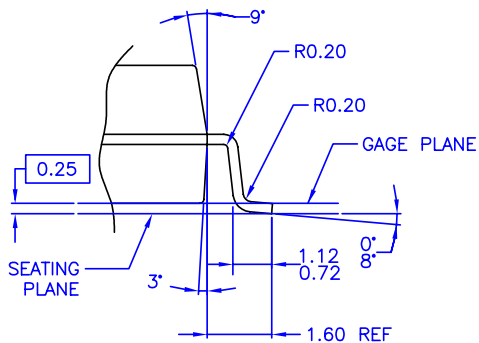
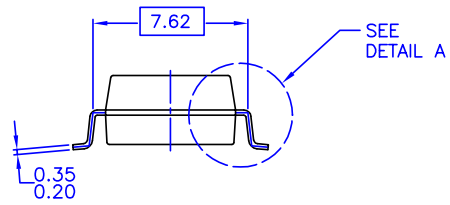
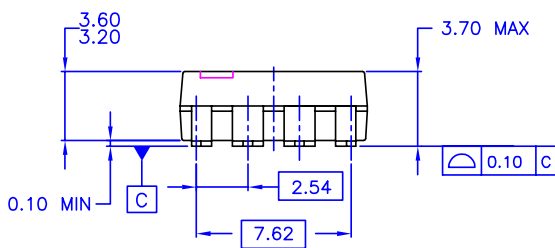
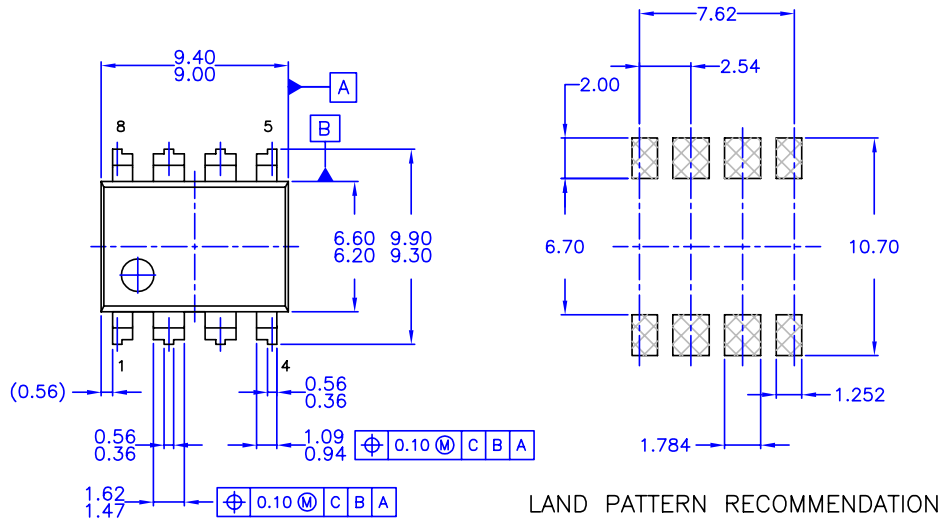


- NOTES: UNLESS OTHERWISE SPECIFIED**
- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-N08FrevB

Package Dimensions (Continued)

8LSOP



DETAIL A  
SCALE: 2X

- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE DOESNOT CONFORM TO ANY CURRENT PACKAGE STANDARD  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.  
 D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

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**Ordering Information**

Product Number	Package	Marking Code	BVDSS	FOSC	RDS(on)
FSDH321	8DIP	DH321	650V	100KHz	14Ω
FSDL321	8DIP	DL321	650V	50KHz	14Ω
FSDH321L	8LSOP	DH321	650V	100KHz	14Ω
FSDL321L	8LSOP	DL321	650V	50KHz	14Ω

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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