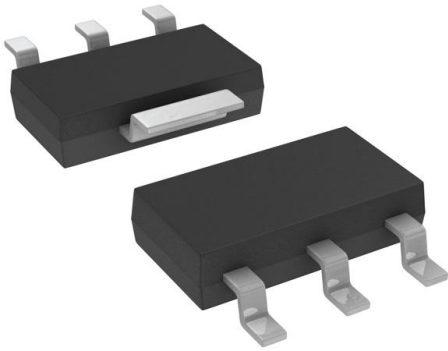


FSQ500L Datasheet

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DiGi Electronics Part Number	FSQ500L-DG
Manufacturer	onsemi
Manufacturer Product Number	FSQ500L
Description	IC OFFLINE SW FLYBACK SOT223-4
Detailed Description	Converter Offline Flyback Topology 130kHz SOT-223-4

This model FSQ500L is available at DiGi Electronics.

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Manufacturer Product Number:

FSQ500L

Series:

FPS™

Output Isolation:

Isolated

Voltage - Breakdown:

700V

Voltage - Start Up:

6 V

Duty Cycle:

60%

Power (Watts):

3 W

Control Features:

Soft Start

Package / Case:

TO-261-4, TO-261AA

Mounting Type:

Surface Mount

Manufacturer:

onsemi

Product Status:

Obsolete

Internal Switch(s):

Yes

Topology:

Flyback

Voltage - Supply (Vcc/Vdd):

5V ~ 10V

Frequency - Switching:

130kHz

Fault Protection:

Current Limiting, Over Load, Over Temperature

Operating Temperature:

-40°C ~ 85°C (TA)

Supplier Device Package:

SOT-223-4

Base Product Number:

FSQ500

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



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May 2024

FSQ500L

Compact, Green Mode, Fairchild Power Switch (FPS™)

Features

- Single Chip 700V SenseFET Power Switch
- Precision Fixed Operating Frequency: 130kHz
- No-load consumption 250mW at 265V_{AC} with Burst Mode and Down to 60mW with External Bias
- Internal Startup Switch
- Soft-Start Time Tuned by External Capacitor
- Under-Voltage Lockout (UVLO) with Hysteresis
- Pulse-by-Pulse Current Limit
- Overload Protection (OLP) and Internal Thermal Shutdown Function (TSD) with Hysteresis
- Auto-Restart Mode
- No Need for Auxiliary Bias Winding

Applications

- Cost-Effective Linear Power Supplies Replacement
- Charger and Adapter for Mobile Phone, PDA, MP3, and Cordless Phone

Related Resources

- [AN4137 — Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch \(FPS™\)](#)
- [AN4141 — Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)
- [AN-4147 — Design Guidelines for RCD Snubber of Flyback Converters](#)
- [AN-6075 — Compact Green Mode Adapter Using FSQ500L for Low Cost](#)
- [AN-4138 — Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch \(FPS™\)](#)
- [Evaluation Board: FEBFSQ500L](#)

Description

The FSQ500L is specially designed for a replacement of linear power supplies with low cost. This device combines current-mode Pulse Width Modulator (PWM) with a senseFET. The integrated PWM controller features include: a fixed oscillator, Under Voltage Lockout (UVLO) protection, Overload Protection (OLP), Leading-Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection with hysteresis, and temperature-compensated precision-current sources for loop compensation. When compared to a linear power supply, the FSQ500L device reduces total size and weight, while increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective flyback converters.

Maximum Output Power ⁽¹⁾			
230V _{AC} ± 15% ⁽²⁾		85-265V _{AC}	
Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾
2.5W	3.0W	2.0W	2.5W

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
4. Maximum practical continuous power in an open frame design at 50°C ambient.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSQ500L	-40°C to +85°C	4-Lead, Small Outline Package (SOT223-4L)	Tape & Reel

Pin Assignments

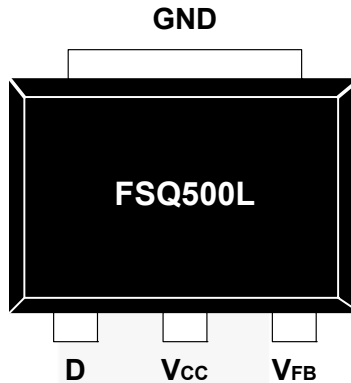


Figure 3. Package / Pin Diagram

Pin Definitions

Pin #	Name	Description
1	D	High-voltage power senseFET drain connection. In addition, at start up, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V _{CC} pin. Once V _{CC} reaches 6.0V, all internal blocks are activated. The internal high-voltage current source is alive until V _{CC} reaches 6.5V. After that, the internal high voltage current source turns on and off irregularly to maintain V _{CC} at 6.5V.
2	V _{CC}	This pin is connected to a storage capacitor. A high-voltage regulator connected between pin 1 (D) and this pin provides the supply voltage to the FSQ500L at startup and when switching during normal operation. The FSQ500L eliminates the need for auxiliary bias winding and associated external components.
3	V _{FB}	This pin is internally connected to the non-inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 4.5V, the overload protection triggers, which shuts down the FPS.
4	GND	This pin is the control ground and the senseFET source.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DS}	Drain Pin Voltage ⁽⁵⁾	700		V
V_{CC}	Supply Voltage		10	V
V_{FB}	Feedback Voltage Range	-0.3	V_{CC}	V
P_D	Total Power Dissipation		0.78	W
I_{DM}	Drain Current Pulsed ⁽⁶⁾		0.41	A
T_J	Operating Junction Temperature	-40	Internally Limited	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

5. LDMOS available drain voltage is -0.3V ~ 700V.
6. Repetitive rating: pulse width is limited by maximum junction temperature.

Thermal Impedance

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance ⁽⁷⁾	+160	°C/W

Note:

7. Free-standing with no heat sink; minimum land pattern.

Electrical Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{CC} = 6.5\text{V}$, $V_{FB} = 0\text{V}$, $I_D = 150\mu\text{A}$	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{CC} = 6.5\text{V}$, $V_{FB} = 0\text{V}$, $V_{DS} = 560\text{V}$			150	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	$T_J = 25^\circ\text{C}$, $I_D = 25\text{mA}$		25	29	Ω
		$T_J = 100^\circ\text{C}$, $I_D = 25\text{mA}$		35	41	Ω
C_{ISS}	Input Capacitance ⁽⁸⁾	$V_{GS} = 6.5\text{V}$		42		pF
C_{OSS}	Output Capacitance ⁽⁸⁾	$V_{DS} = 40\text{V}$, $f_s = 1\text{MHz}$		25		pF
t_r	Rise Time ⁽⁸⁾	$V_{DS} = 350\text{V}$, $I_D = 25\text{mA}$		100		ns
t_f	Fall Time ⁽⁸⁾	$V_{DS} = 350\text{V}$, $I_D = 25\text{mA}$		50		ns
Control Section						
f_s	Switching Frequency	$V_{CC} = 6.5\text{V}$, $V_{FB} = 1.0\text{V}$	120	130	140	kHz
Δf_s	Switching Frequency Variation ⁽⁸⁾	$-25^\circ\text{C} < T_J < 125^\circ\text{C}$		± 5	± 7	%
$I_{FB(Burst)}$	Feedback Source Current	$V_{CC} = 6.5\text{V}$, $V_{FB} = 0\text{V}$	98	110	122	μA
$I_{FB(Normal)}$		$V_{CC} = 6.5\text{V}$	200	225	250	μA
D_{MAX}	Maximum Duty Ratio	$V_{CC} = 6.5\text{V}$, $V_{FB} = 4.0\text{V}$	54	60	66	%
D_{MIN}	Minimum Duty Ratio	$V_{CC} = 6.5\text{V}$, $V_{FB} = 0\text{V}$			0	%
V_{START}	UVLO Threshold Voltage	$V_{FB} = 0\text{V}$, V_{CC} Sweep	5.5	6.0	6.5	V
V_{STOP}		After turn-on, $V_{FB} = 0\text{V}$, V_{CC} Sweep	4.5	5.0	5.5	V
V_{DLY_EN}	Shutdown Delay Current Enable Voltage	$V_{FB} = V_{SD}$, V_{CC} Sweep from 6V	6.0	6.5	7.0	V
Burst-Mode Section						
V_{BURH}	Burst Mode Voltage	$V_{CC} = 6.5\text{V}$, V_{FB} Sweep	0.75	0.80	0.85	V
V_{BURL}			0.70	0.75	0.80	V
HYS			30	50	80	mV
Protection Section						
I_{LIM}	Peak Current Limit	$di/dt = 150\text{mA}/\mu\text{s}$	245	280	315	mA
V_{SD}	Shutdown Feedback Voltage	$V_{CC} = 6.5\text{V}$, V_{FB} Sweep	4.1	4.5	4.9	V
I_{DELAY}	Shutdown Delay Current	$V_{CC} = 6.5\text{V}$, $V_{FB} = 4.0\text{V}$	4	5	6	μA
t_{LEB}	Leading Edge Blanking Time ⁽⁸⁾			250		ns
t_{CLD}	Current Limit Delay Time ⁽⁸⁾			100		ns
TDS	Thermal Shutdown Temperature ⁽⁸⁾		130	140	150	$^\circ\text{C}$
HYS				80		$^\circ\text{C}$
Total Device Section						
I_{OP_BURST}	Operating Supply Current (Control Part Only)	$V_{CC} = 6.5\text{V}$, $V_{FB} = 0\text{V}$	360	430	500	μA
I_{OP_FB}		$V_{CC} = 6.5\text{V}$, $V_{FB} = 4\text{V}$	640	760	880	μA
I_{CH}	Startup Charging Current	$V_{CC} = V_{FB} = 0\text{V}$, $V_{DS} = 40\text{V}$	3.3			mA
V_{CCREG}	Supply Shunt Regulator	$V_{DS} = 40\text{V}$, $V_{FB} = 0\text{V}$	6.0	6.5	7.0	V
V_{CCREG_TSD}	Supply Shunt Regulator During TSD ⁽⁸⁾		5.2	5.7	6.2	V

Note:

8. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

These characteristic graphs are measured at $T_A = 25^\circ\text{C}$.

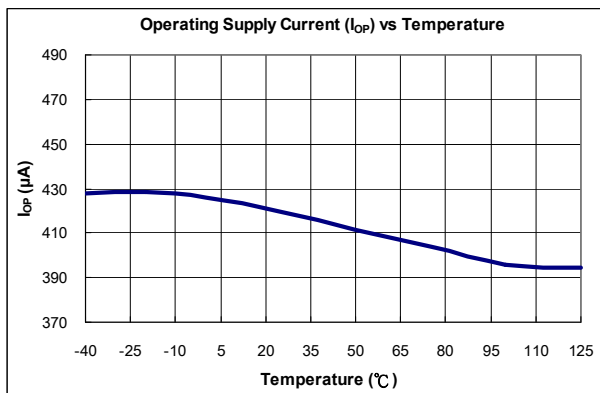


Figure 4. Operating Supply Current (I_{OP_BURST}) vs. Temperature

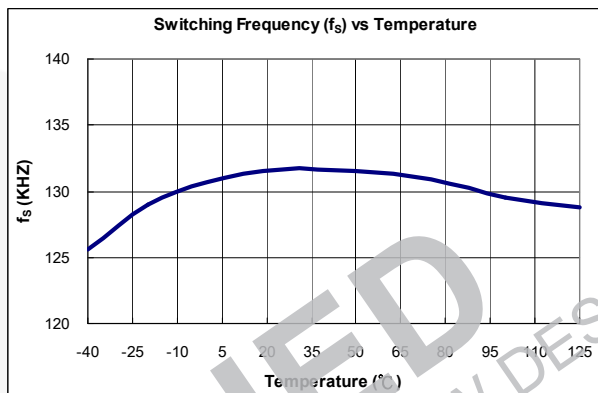


Figure 5. Switching Frequency (f_s) vs. Temperature

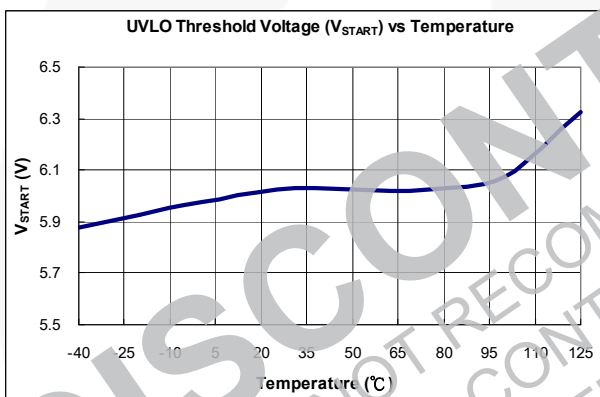


Figure 6. UVLO Threshold Voltage (V_{START}) vs. Temperature

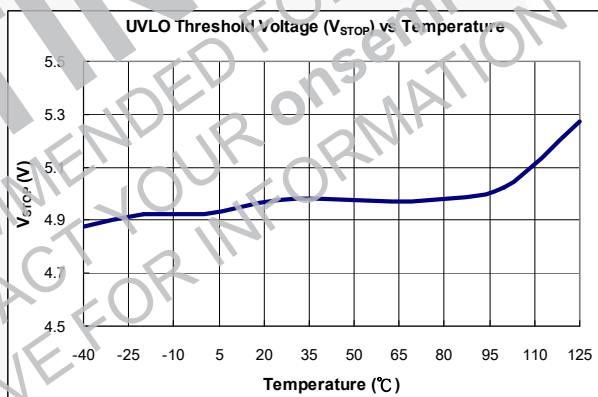


Figure 7. UVLO Threshold Voltage (V_{STOP}) vs. Temperature

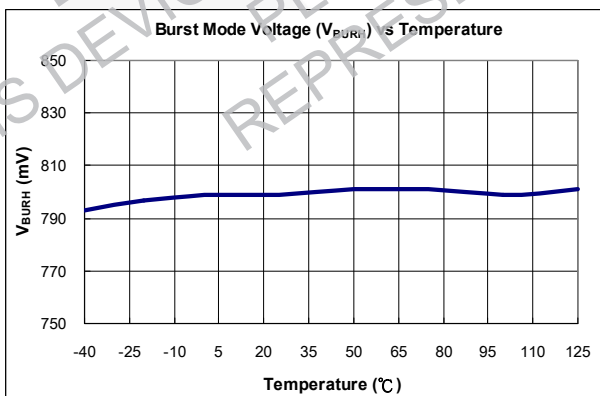


Figure 8. Burst-Mode Voltage (V_{BURH}) vs. Temperature

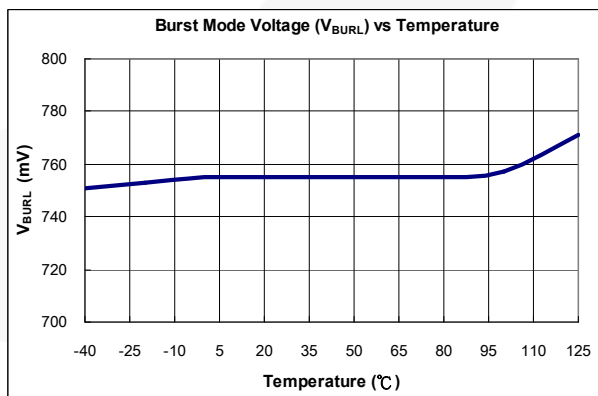


Figure 9. Burst-Mode Voltage (V_{BURL}) vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are measured at $T_A = 25^\circ\text{C}$.

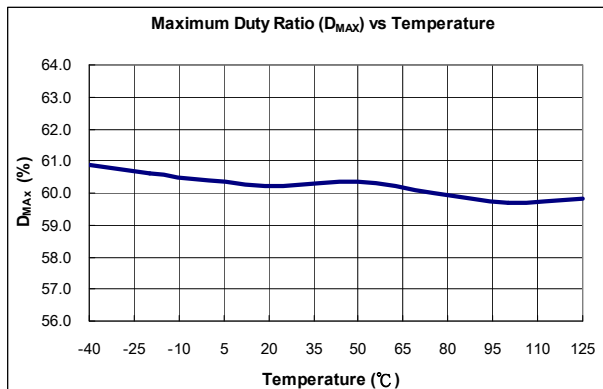


Figure 10. Maximum Duty Ratio (D_{MAX}) vs. Temperature

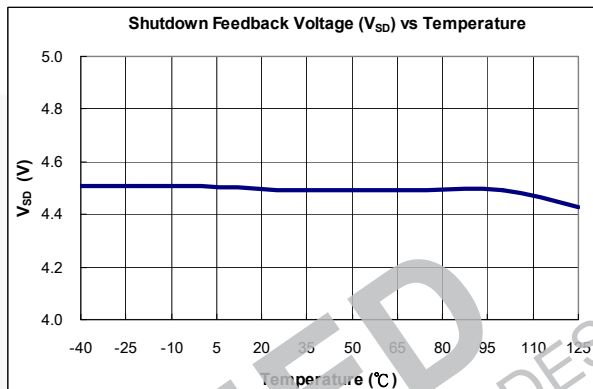


Figure 11. Shutdown Feedback Voltage (V_{SD}) vs. Temperature

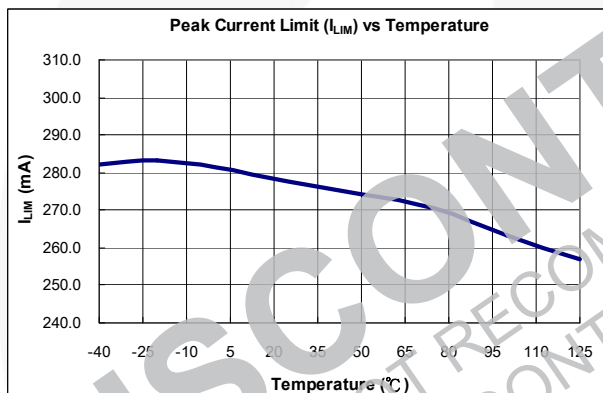


Figure 12. Peak Current Limit (I_{LIM}) vs. Temperature

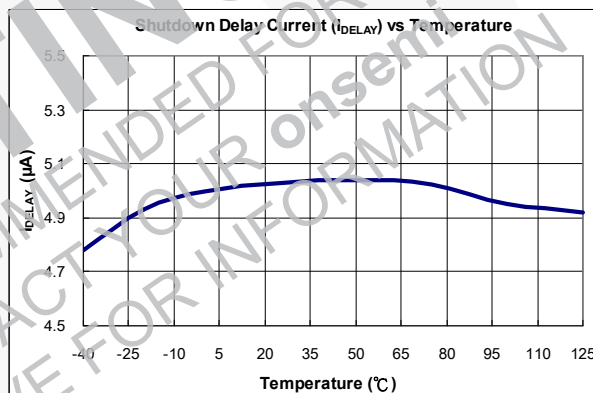


Figure 13. Shutdown Delay Current (I_{DELAY}) vs. Temperature

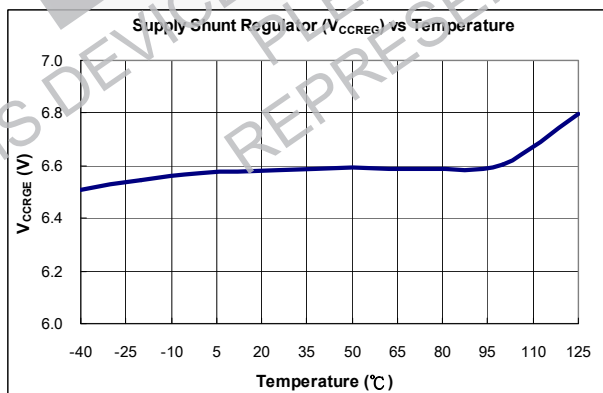


Figure 14. Supply Shunt Regulator (V_{CCREG}) vs. Temperature

3.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger after a specified time to determine whether the situation is transient or a true overload. Because of the pulse-by-pulse current limit capability, the maximum peak current through the senseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.7V, D1 is blocked and the $5\mu A$ current source starts to charge C_B slowly up to V_{CC} . In this condition, V_{FB} continues increasing until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 18. The delay time for shutdown is the time required to charge C_B from 2.7V to 4.5V with $5\mu A$. In general, a 10 ~ 50ms delay time is typical for most applications. This protection is implemented in auto restart mode.

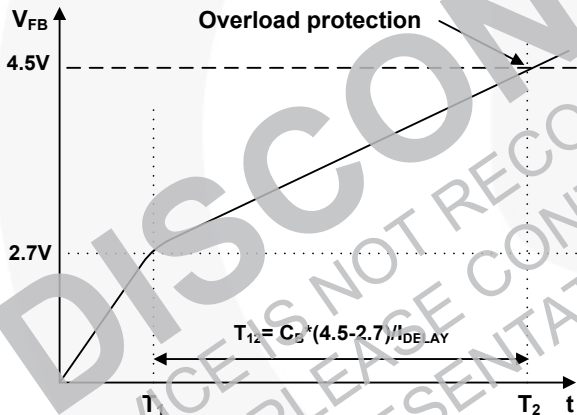


Figure 18. Overload Protection

3.2 Thermal Shutdown (TSD): The senseFET and the control IC in one package makes it easy for the control IC to detect an abnormal over temperature of the senseFET. When the temperature exceeds approximately 140°C, the thermal shutdown triggers. When TSD triggers, delay current is disabled, switching operation stops, and V_{CC} through the internal high-voltage current source is set to 5.7V from 6.5V, as shown in Figure 19. Since TSD signal prohibits the senseFET from switching, there is no switching until the junction temperature decreases sufficiently. If the junction temperature is lower than 60°C typically, TSD signal is removed and V_{CC} is set to 6.5V again. While V_{CC} increases from 5.7V to 6.5V, the soft-start function makes the senseFET turn on and off with no voltage and/or current stress.

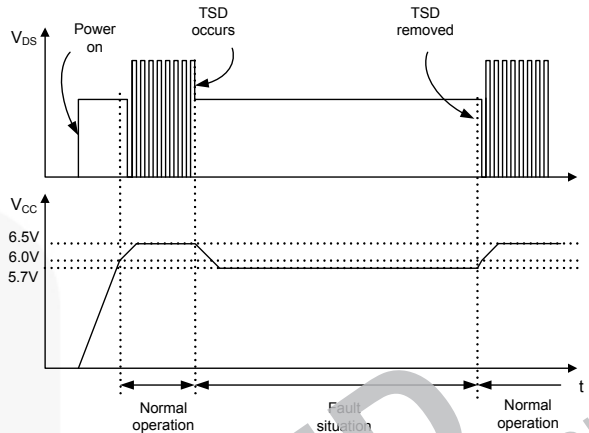


Figure 19. Over-Temperature Protection (OTP)

4. Soft-Start: The soft-start time is tuned by an external V_{CC} capacitor (C_A), which increases PWM comparator non-inverting input voltage together with the senseFET current slowly after it starts up. Before V_{CC} reaches V_{START} , C_A is charged by the current $I_{CH-I_{START}}$, where I_{CH} and I_{START} are described in Figure 15. After V_{CC} reaches V_{START} , all internal blocks are activated, so that the current consuming inside IC becomes I_{CP} . Therefore, C_A is charged by the current $I_{CH-I_{CP}}$, which makes the increasing slope of V_{CC} become sluggish. V_{CC} is shifted by 6.0V negatively (it is performed in soft-start block in Figure 2), and then $V_{CC} - 6.0V$ is an input of one of the input terminals of the PWM comparator. The drain current follows $V_{CC} - 6.0V$ instead of the V_{FB}^* because of the low-dominant feature of the PWM comparator. The soft-start time can be made long or short by selecting C_A , as described in Figure 20. During $t_{S/S}$, I_{DELAY} is disabled to avoid unwanted OLP. Typically, $t_{S/S}$ is around 4.6ms with 27 μF of C_A .

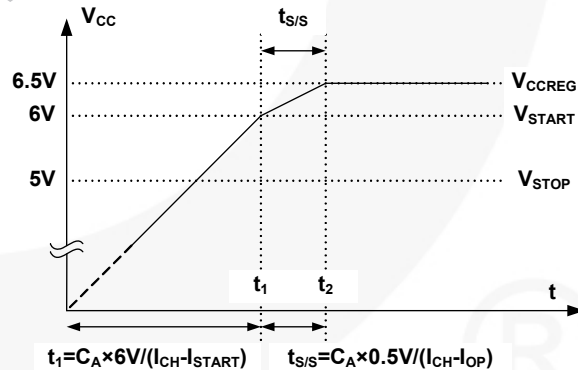


Figure 20. Soft-Start Function

The peak value of the drain current of the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce stress on the secondary diode during startup.

5. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. During the burst mode operation, $I_{FB(Burst)}$ decreases half of $I_{FB(Normal)}$. As the load decreases, the feedback voltage decreases. As shown in Figure 21, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (800mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode alternately enables and disables switching of the power senseFET, reducing switching loss in standby mode.

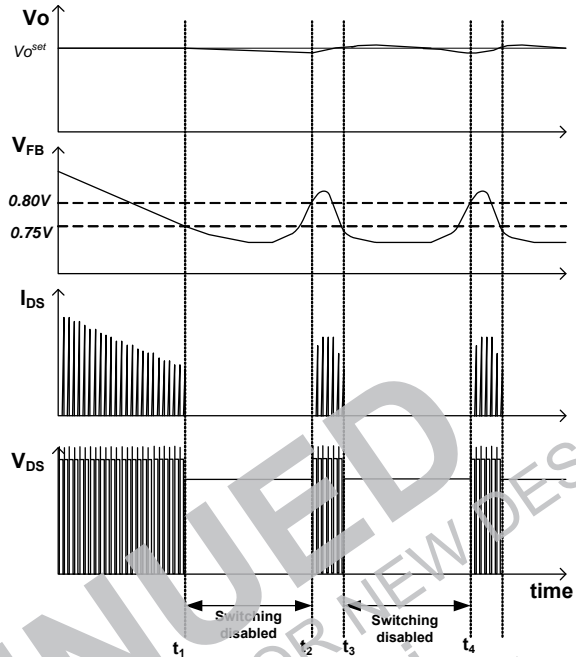



Figure 21. Burst-Mode Operation

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