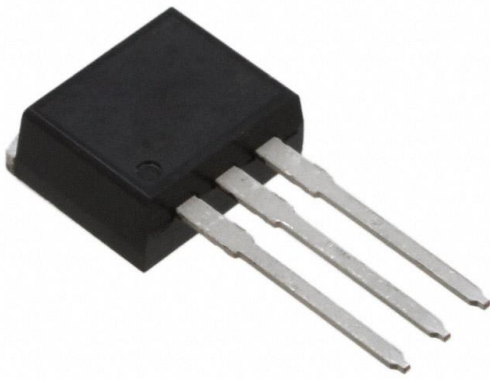


# IRLW630ATM Datasheet

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DiGi Electronics Part Number	IRLW630ATM-DG
Manufacturer	<a href="#">onsemi</a>
Manufacturer Product Number	IRLW630ATM
Description	MOSFET N-CH 200V 9A I2PAK
Detailed Description	N-Channel 200 V 9A (Tc) 3.1W (Ta), 69W (Tc) Through Hole TO-262 (I2PAK)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

Manufacturer Product Number:

IRLW630ATM

Series:

-

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

200 V

Drive Voltage (Max Rds On, Min Rds On):

5V

Vgs(th) (Max) @ Id:

2V @ 250μA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

TO-262 (I2PAK)

Base Product Number:

IRLW63

Manufacturer:

onsemi

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

9A (Tc)

Rds On (Max) @ Id, Vgs:

400mOhm @ 4.5A, 5V

Gate Charge (Qg) (Max) @ Vgs:

27 nC @ 5 V

Input Capacitance (Ciss) (Max) @ Vds:

755 pF @ 25 V

Power Dissipation (Max):

3.1W (Ta), 69W (Tc)

Mounting Type:

Through Hole

Package / Case:

TO-262-3 Long Leads, I2PAK, TO-262AA

## Environmental & Export classification

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

# Advanced Power MOSFET

# IRLW/I630A

## FEATURES

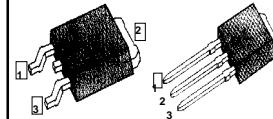
- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ 150°C Operating Temperature
- ◆ Lower Leakage Current: 10 $\mu$ A (Max.) @  $V_{DS} = 200V$
- ◆ Lower  $R_{DS(ON)}$ : 0.335 $\Omega$  (Typ.)

$$BV_{DSS} = 200 V$$

$$R_{DS(on)} = 0.4\Omega$$

$$I_D = 9 A$$

**D<sup>2</sup>-PAK I<sup>2</sup>-PAK**



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	200	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	9	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	5.7	
$I_{DM}$	Drain Current-Pulsed (1)	32	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (2)	54	mJ
$I_{AR}$	Avalanche Current (1)	9	A
$E_{AR}$	Repetitive Avalanche Energy (1)	6.9	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ ) *	3.1	W
	Total Power Dissipation ( $T_C=25^\circ C$ )	69	W
	Linear Derating Factor	0.55	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.81	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount).

Rev. B

**IRLW/I630A****N-CHANNEL  
POWER MOSFET****Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	200	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.18	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=200V$
		--	--	100		$V_{DS}=160V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.4	$\Omega$	$V_{GS}=5V, I_D=4.5A$ (4)
$g_{fs}$	Forward Transconductance	--	4.5	--	$\bar{U}$	$V_{DS}=40V, I_D=4.5A$ (4)
$C_{iss}$	Input Capacitance	--	580	755	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	90	115		
$C_{rss}$	Reverse Transfer Capacitance	--	44	55		
$t_{d(on)}$	Turn-On Delay Time	--	8	25	ns	$V_{DD}=100V, I_D=9A,$ $R_G=6\Omega$ <b>See Fig 13</b> (4) (5)
$t_r$	Rise Time	--	6	20		
$t_{d(off)}$	Turn-Off Delay Time	--	30	70		
$t_f$	Fall Time	--	9	30		
$Q_g$	Total Gate Charge	--	18.6	27	nC	$V_{DS}=160V, V_{GS}=5V,$ $I_D=9A$ <b>See Fig 6 &amp; Fig 12</b> (4) (5)
$Q_{gs}$	Gate-Source Charge	--	3.5	--		
$Q_{gd}$	Gate-Drain (. Miller. ) Charge	--	8.3	--		

**Source-Drain Diode Ratings and Characteristics**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	9	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current (1)	--	--	32		
$V_{SD}$	Diode Forward Voltage (4)	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=9A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	158	--	ns	$T_J=25^\circ\text{C}, I_F=9A$
$Q_{rr}$	Reverse Recovery Charge	--	0.78	--	$\mu\text{C}$	$di_F/dt=100A/\mu\text{s}$ (4)

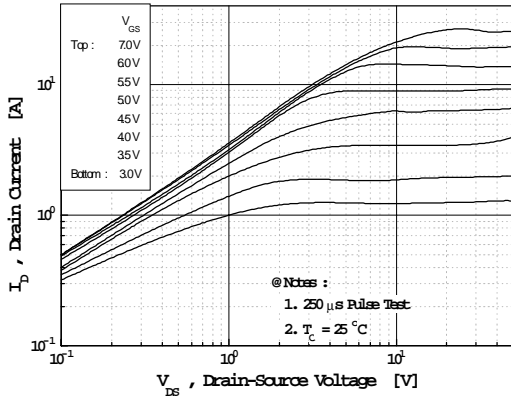
**Notes;**

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2)  $L=1\text{mH}, I_{AS}=9A, V_{DD}=50V, R_G=27\Omega,$  Starting  $T_J=25^\circ\text{C}$
- (3)  $I_{SD} \leq 9A, di/dt \leq 220A/\mu\text{s}, V_{DD} \leq BV_{DSS},$  Starting  $T_J=25^\circ\text{C}$
- (4) Pulse Test: Pulse Width = 250 $\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- (5) Essentially Independent of Operating Temperature

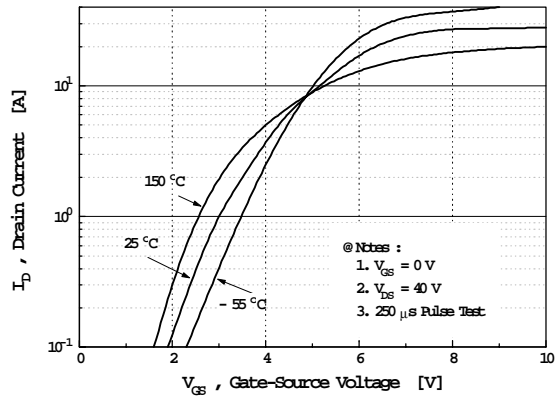
**N-CHANNEL  
POWER MOSFET**

**IRLW/I630A**

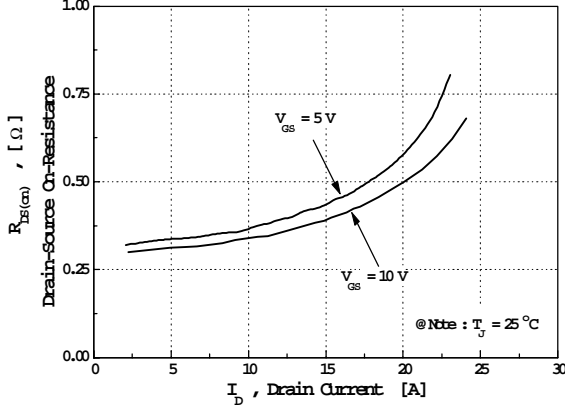
**Fig 1. Output Characteristics**



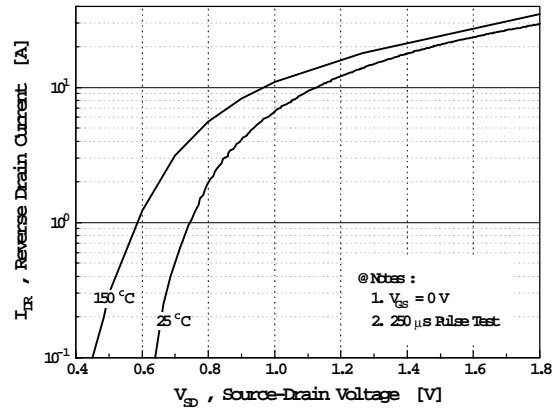
**Fig 2. Transfer Characteristics**



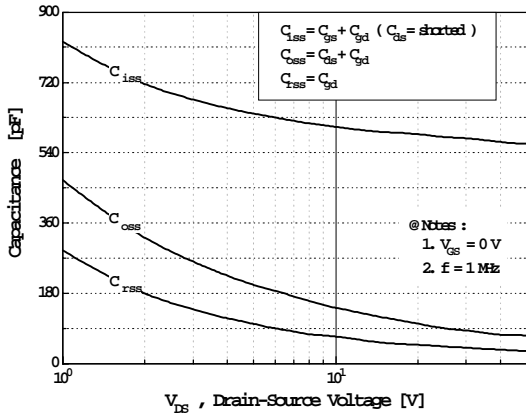
**Fig 3. On-Resistance vs. Drain Current**



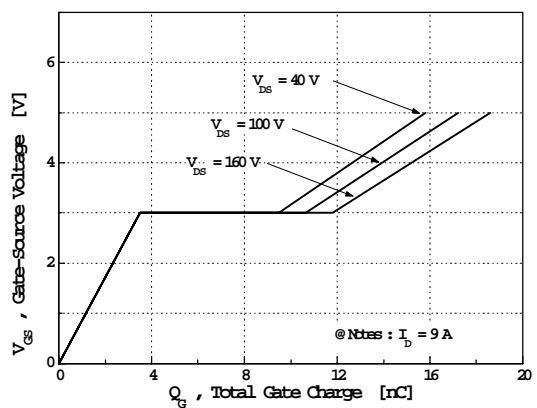
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**



# IRLW/I630A

## N-CHANNEL POWER MOSFET

Fig 7. Breakdown Voltage vs. Temperature

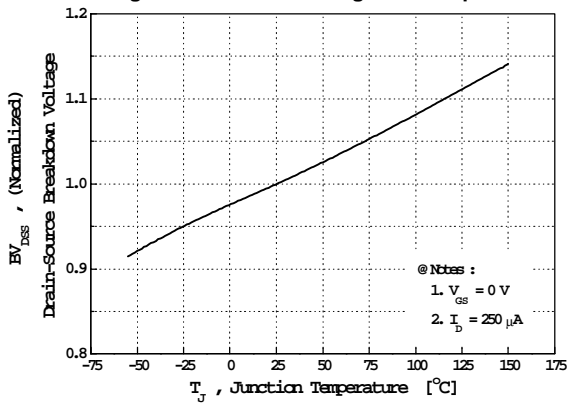


Fig 8. On-Resistance vs. Temperature

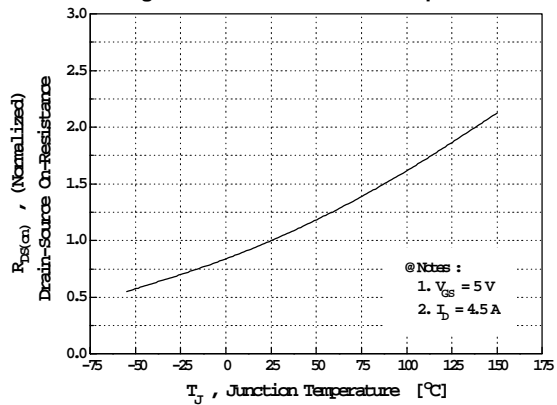


Fig 9. Max. Safe Operating Area

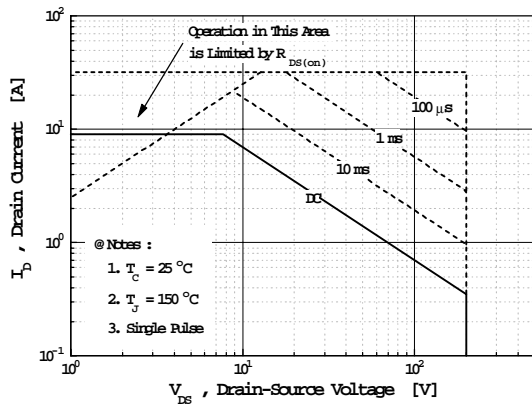


Fig 10. Max. Drain Current vs. Case Temperature

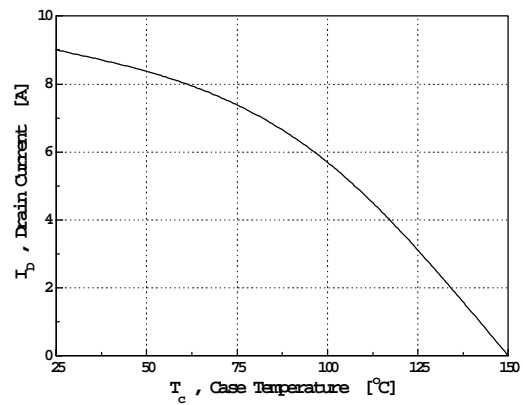
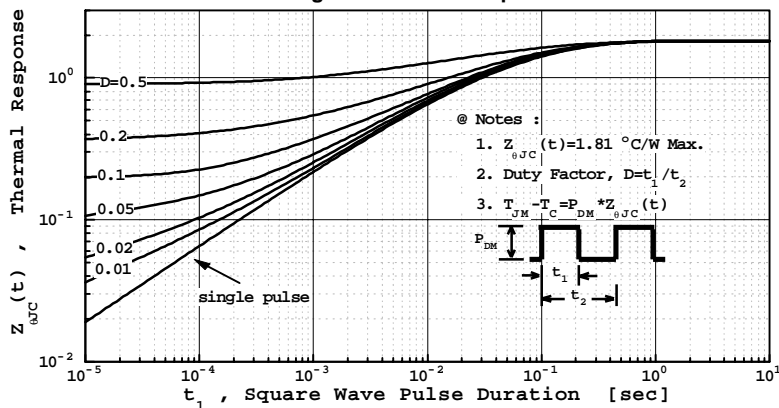


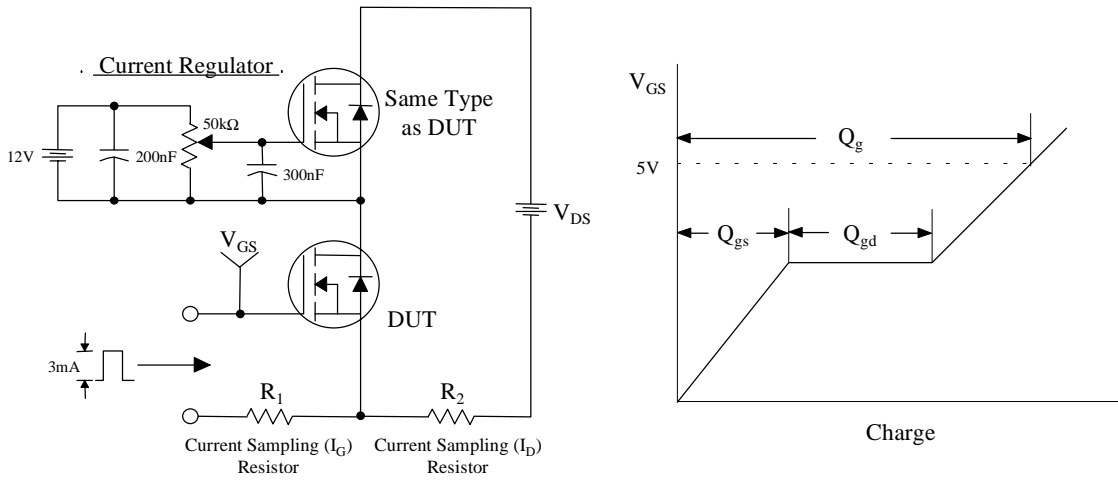
Fig 11. Thermal Response



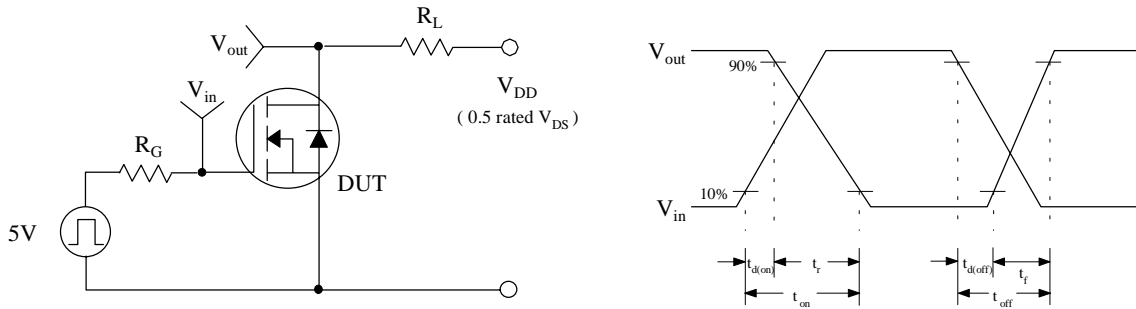
**N-CHANNEL  
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**IRLW/I630A**

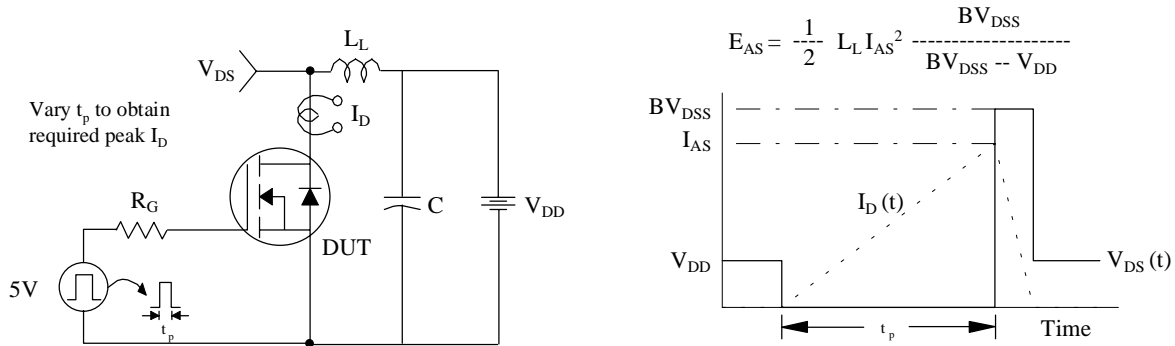
**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



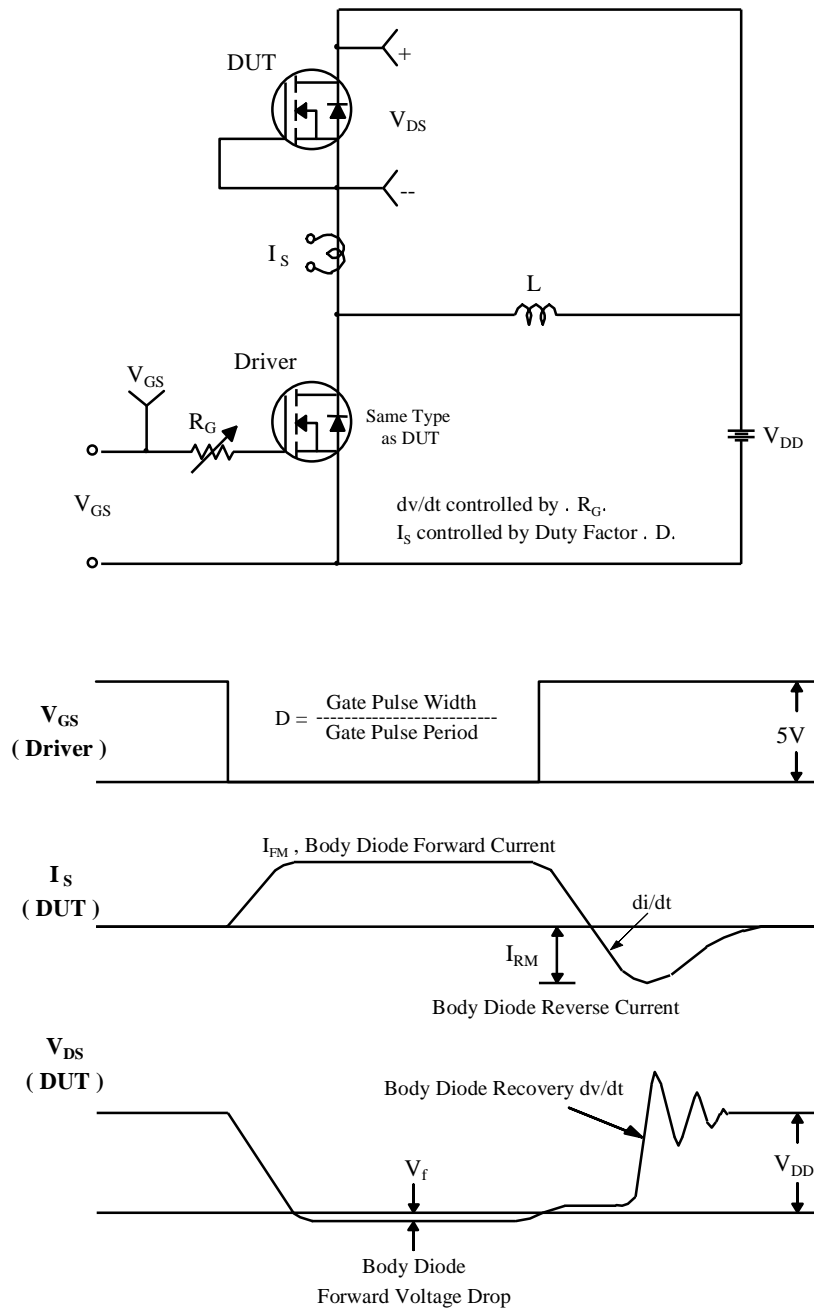
**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**



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## N-CHANNEL POWER MOSFET

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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