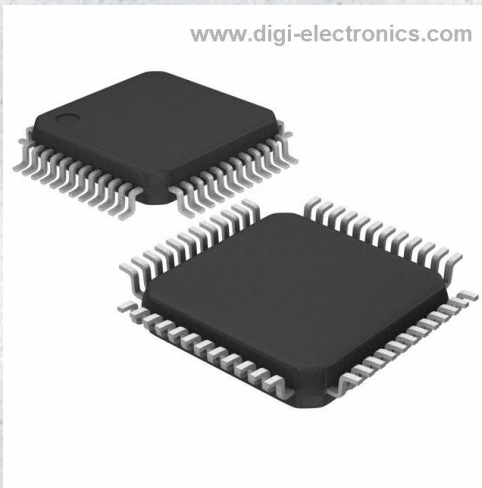


LC75833W-E Datasheet



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---------------------------------|
| DiGi Electronics Part Number | LC75833W-E-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | LC75833W-E |
| Description | IC DRVR LCD DISPLAY 105 SEGMENT |
| Detailed Description | LCD Driver |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

LC75833W-E

Series:

-

Display Type:

LCD

Interface:

Serial

Current - Supply:

250 μ A

Operating Temperature:

-40°C ~ 85°C

Package / Case:

48-LQFP

Manufacturer:

onsemi

Product Status:

Obsolete

Configuration:

105 Segment

Digits or Characters:

-

Voltage - Supply:

2.7V ~ 6V

Mounting Type:

Surface Mount

Base Product Number:

LC75833

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

4 (72 Hours)

ECCN:

EAR99



LC75833E, 75833W, 75833JE

1/3 Duty General-Purpose LCD Display Drivers

An ON Semiconductor Company



Overview

The LC75833E, LC75833W, and LC75833JE are 1/3-duty general-purpose LCD display drivers that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75833E and LC75833W can drive an LCD with up to 105 segments directly, the LC75833JE can drive an LCD with up to 93 segments directly. The LC75833E and LC75833W and LC75833JE can also control up to 8 general-purpose output ports. Since the LC75833E, LC75833W, and LC75833JE use separate power supply systems for the LCD drive block and the logic block, the LCD driver block power-supply voltage can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.

Features

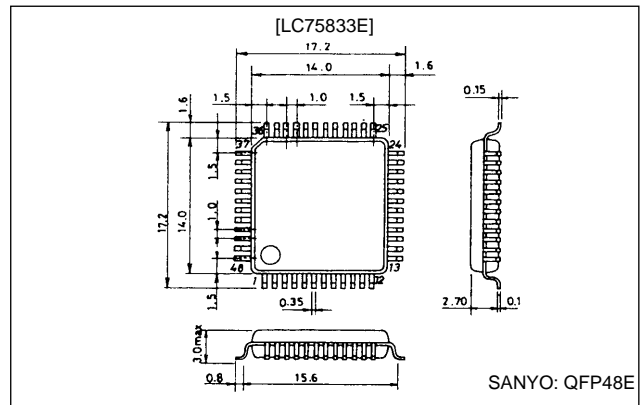
- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD drive under serial data control.
 - LC75833E, LC75833W: up to 105 segments
 - LC75833JE: up to 93 segments (without the S12, S23, S24, S35 segment output pins from the LC75833E, LC75833W)
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and the general-purpose output port functions
- High generality, since display data is displayed directly without decoder intervention.
- Independent V_{LCD} for the LCD driver block (V_{LCD} can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.)
- The \overline{INH} pin can force the display to the off state.
- RC oscillator circuit

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

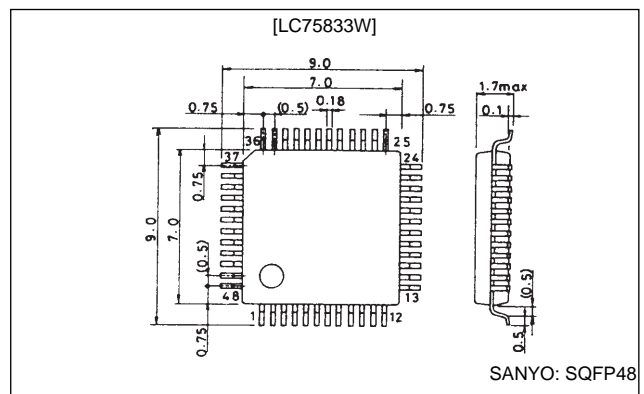
unit: mm

3156-QFP48E



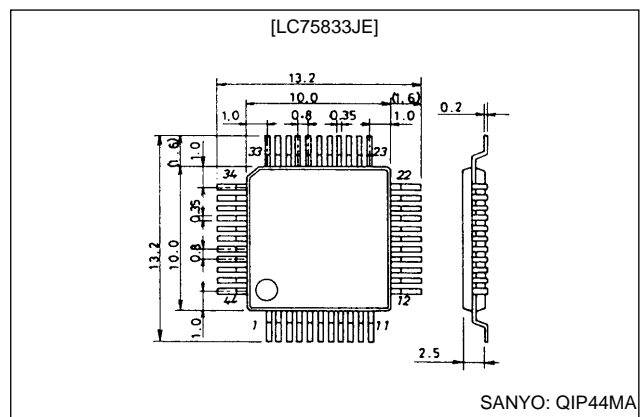
unit: mm

3163A-SQFP48



unit: mm

3148-QFP44MA



LC75833E, 75833W, 75833JE

Specifications**Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V**

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|----------------------|---|--------------------------------|------|
| Maximum supply voltage | V _{DD max} | V _{DD} | -0.3 to +7.0 | V |
| | V _{LCD max} | V _{LCD} | -0.3 to +7.0 | V |
| Input voltage | V _{IN 1} | CE, CL, DI, $\overline{\text{INH}}$ | -0.3 to +7.0 | V |
| | V _{IN 2} | OSC | -0.3 to V _{DD} + 0.3 | V |
| | V _{IN 3} | V _{LCD 1} , V _{LCD 2} | -0.3 to V _{LCD} + 0.3 | V |
| Output voltage | V _{OUT 1} | OSC | -0.3 to V _{DD} + 0.3 | V |
| | V _{OUT 2} | S1 to S35, COM1 to COM3, P1 to P8 | -0.3 to V _{LCD} + 0.3 | V |
| Output current | I _{OUT 1} | S1 to S35 | 300 | μA |
| | I _{OUT 2} | COM1 to COM3 | 3 | mA |
| | I _{OUT 3} | P1 to P8 | 5 | mA |
| Allowable power dissipation | Pd max | Ta = 85°C | 150 | mW |
| Operating temperature | T _{opr} | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

Allowable Operating Ranges at Ta = -40 to +85°C, V_{SS} = 0 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|--|---------------------|----------------------|---------------------|------|
| | | | min | typ | max | |
| Supply voltage | V _{DD} | V _{DD} | 2.7 | | 6.0 | V |
| | V _{LCD} | V _{LCD} | 2.7 | | 6.0 | V |
| Input voltage | V _{LCD1} | V _{LCD1} | | 2/3 V _{LCD} | V _{LCD} | V |
| | V _{LCD2} | V _{LCD2} | | 1/3 V _{LCD} | V _{LCD} | V |
| Input high-level voltage | V _{IH} | CE, CL, DI, $\overline{\text{INH}}$ | 0.8 V _{DD} | | 6.0 | V |
| Input low-level voltage | V _{IL} | CE, CL, DI, $\overline{\text{INH}}$ | 0 | | 0.2 V _{DD} | V |
| Recommended external resistance | R _{OSC} | OSC | | 39 | | kΩ |
| Recommended external capacitance | C _{OSC} | OSC | | 1000 | | pF |
| Guaranteed oscillation range | f _{OSC} | OSC | 19 | 38 | 76 | kHz |
| Data setup time | t _{ds} | CL, DI: Figure 2 | 160 | | | ns |
| Data hold time | t _{dh} | CL, DI: Figure 2 | 160 | | | ns |
| CE wait time | t _{cp} | CE, CL: Figure 2 | 160 | | | ns |
| CE setup time | t _{cs} | CE, CL: Figure 2 | 160 | | | ns |
| CE hold time | t _{ch} | CE, CL: Figure 2 | 160 | | | ns |
| High-level clock pulse width | t _{øH} | CL: Figure 2 | 160 | | | ns |
| Low-level clock pulse width | t _{øL} | CL: Figure 2 | 160 | | | ns |
| Rise time | t _r | CE, CL, DI: Figure 2 | | 160 | | ns |
| Fall time | t _f | CE, CL, DI: Figure 2 | | 160 | | ns |
| $\overline{\text{INH}}$ switching time | t _c | $\overline{\text{INH}}$, CE: Figure 3 | 10 | | | μs |

LC75833E, 75833W, 75833JE

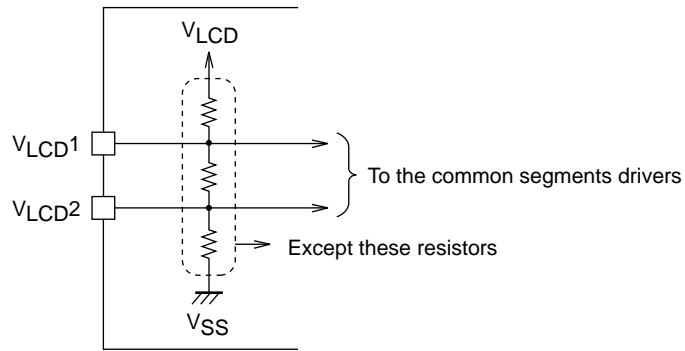
Electrical Characteristics for the Allowable Operating Ranges

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------|------------|--|---------------------|--------------|---------------------|---------------|
| | | | min | typ | max | |
| Hysteresis width | V_H | CE, CL, DI, $\overline{\text{INH}}$ | | 0.1 V_{DD} | | V |
| Input high level current | I_{IH} | CE, CL, DI, $\overline{\text{INH}}$; $V_I = 6.0$ V | | | 5.0 | μA |
| Input low level current | I_{IL} | CE, CL, DI, $\overline{\text{INH}}$; $V_I = 0$ V | -5.0 | | | μA |
| Output high-level voltage | V_{OH1} | S1 to S35; $I_O = -20$ μA | $V_{LCD} - 0.9$ | | | V |
| | V_{OH2} | COM1 to COM3; $I_O = -100$ μA | $V_{LCD} - 0.9$ | | | V |
| | V_{OH3} | P1 to P8; $I_O = -1$ mA | $V_{LCD} - 0.9$ | | | V |
| Output low-level voltage | V_{OL1} | S1 to S35; $I_O = 20$ μA | | | 0.9 | V |
| | V_{OL2} | COM1 to COM3; $I_O = 100$ μA | | | 0.9 | V |
| | V_{OL3} | P1 to P8; $I_O = 1$ mA | | | 0.9 | V |
| Output middle-level voltage*1 | V_{MID1} | COM1 to COM3; 1/2 bias, $I_O = \pm 100$ μA | $1/2 V_{LCD} - 0.9$ | | $1/2 V_{LCD} + 0.9$ | V |
| | V_{MID2} | S1 to S35; 1/3 bias, $I_O = \pm 20$ μA | $2/3 V_{LCD} - 0.9$ | | $2/3 V_{LCD} + 0.9$ | V |
| | V_{MID3} | S1 to S35; 1/3 bias, $I_O = \pm 20$ μA | $1/3 V_{LCD} - 0.9$ | | $1/3 V_{LCD} + 0.9$ | V |
| | V_{MID4} | COM1 to COM3; 1/3 bias, $I_O = \pm 100$ μA | $2/3 V_{LCD} - 0.9$ | | $2/3 V_{LCD} + 0.9$ | V |
| | V_{MID5} | COM1 to COM3; 1/3 bias, $I_O = \pm 100$ μA | $1/3 V_{LCD} - 0.9$ | | $1/3 V_{LCD} + 0.9$ | V |
| Oscillator frequency | f_{OSC} | OSC; $R_{OSC} = 39$ k Ω $C_{OSC} = 1000$ pF | 30.4 | 38 | 45.6 | kHz |
| Current drain | I_{DD1} | V_{DD} : power saving mode | | | 5 | μA |
| | I_{DD2} | V_{DD} : $V_{DD} = 6.0$ V, output open, $f_{osc} = 38$ kHz | | 250 | 500 | μA |
| | I_{LCD1} | V_{LCD} : power saving mode | | | 5 | μA |
| | I_{LCD2} | V_{LCD} : $V_{LCD} = 6.0$ V, output open 1/2 bias, $f_{osc} = 38$ kHz | | 100 | 200 | μA |
| | I_{LCD3} | V_{LCD} : $V_{LCD} = 6.0$ V, output open 1/3 bias, $f_{osc} = 38$ kHz | | 60 | 120 | μA |

Note: *1 Excluding the bias voltage generation divider resistors built in the V_{LCD1} and V_{LCD2} . (See Figure 1.)

The LC75833JE does not have the S12, S23, S24, S35 output pins.

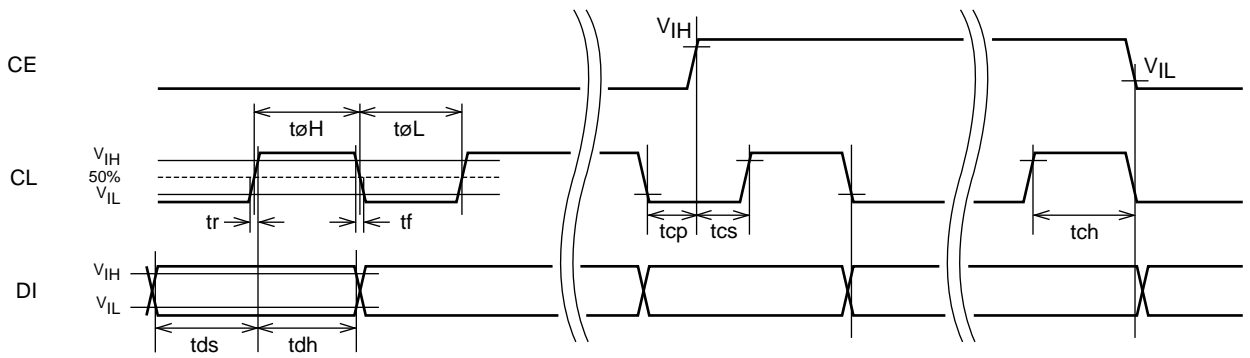
LC75833E, 75833W, 75833JE



A06550

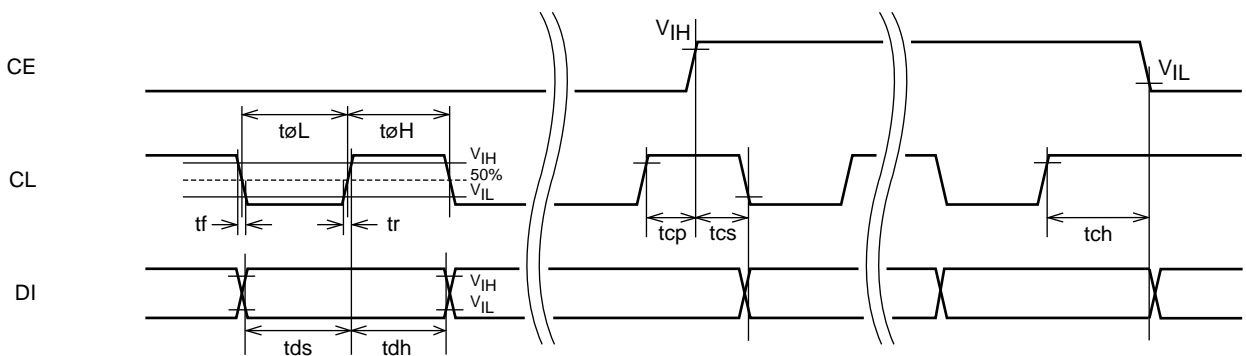
Figure 1

1. When CL is stopped at the low level



A06551

2. When CL is stopped at the high level

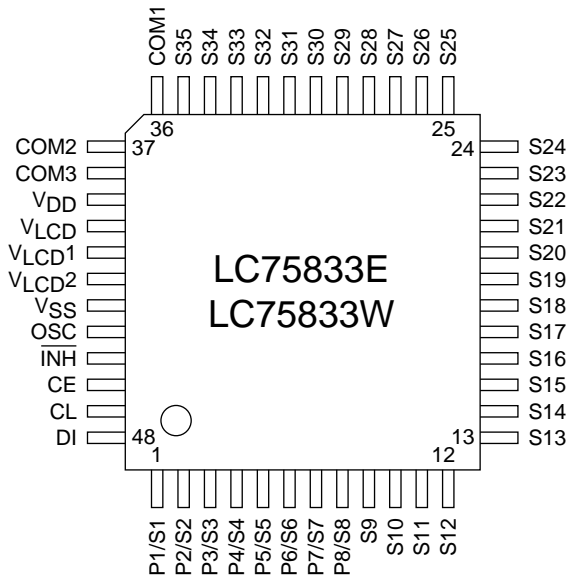


A06552

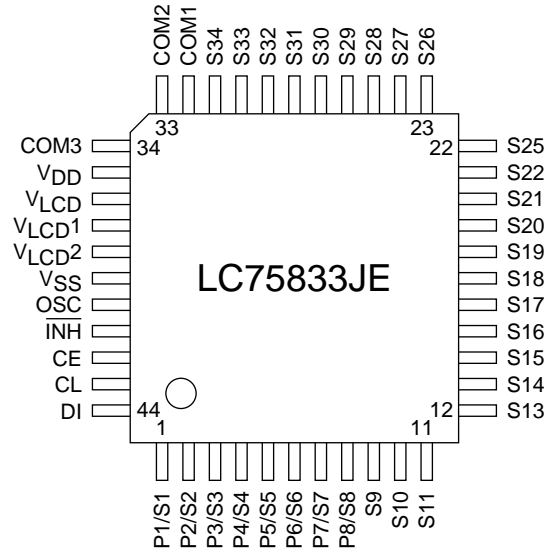
Figure 2

LC75833E, 75833W, 75833JE

Pin Assignments

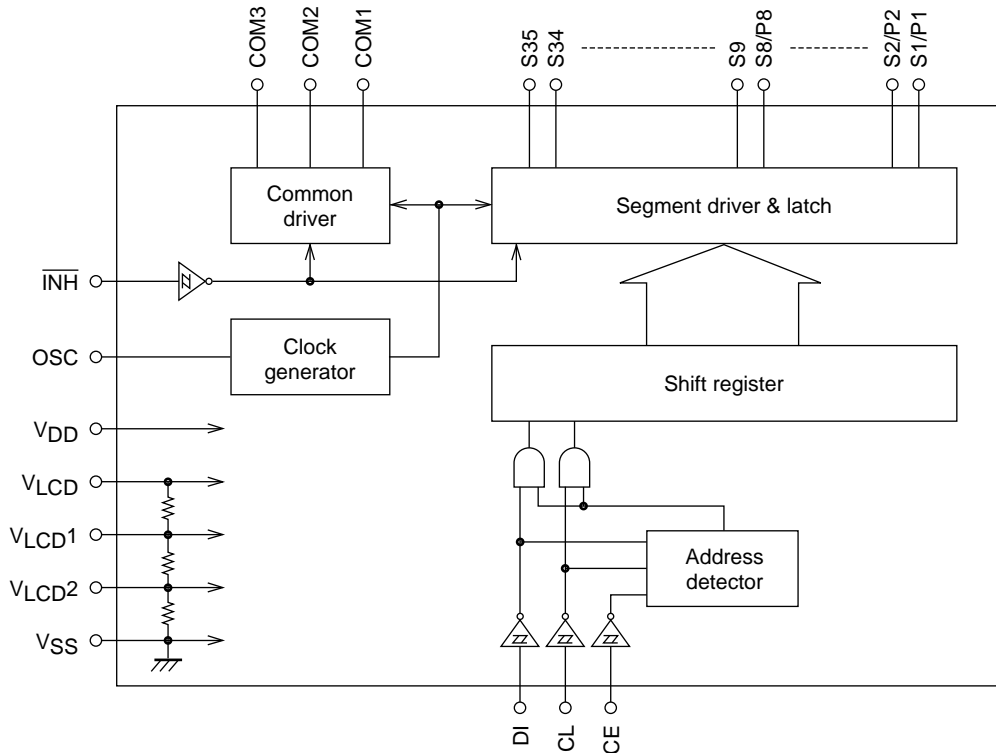


A06549



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Block Diagram



A06553

Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

LC75833E, 75833W, 75833JE

Pin Functions

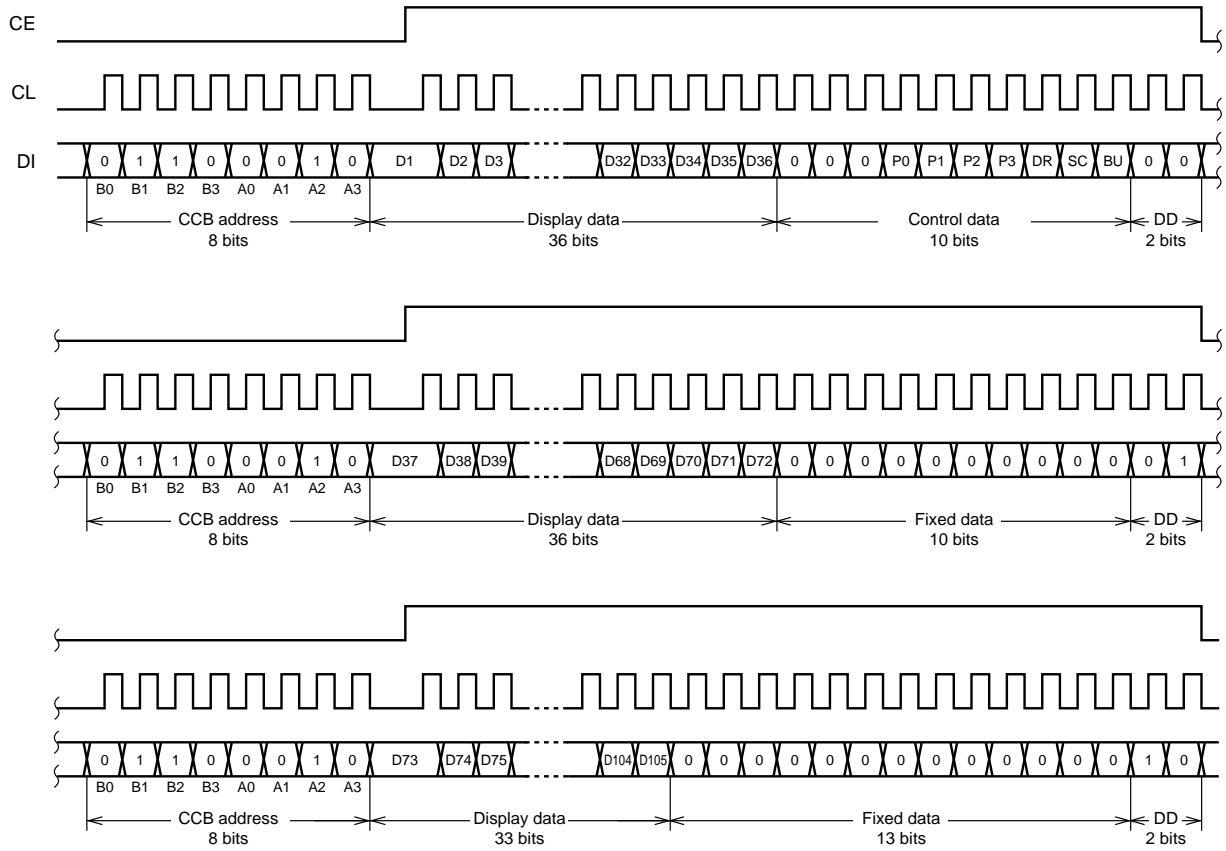
| Pin | Pin No. | | Functions | Active | I/O | Handling when unused |
|--------------------------------|---------------------|-------------------|---|---|-------------|----------------------|
| | LC75833E, 75833W | LC75833JE | | | | |
| S1/P1 to S8/P8 S9 to S35 | 1 to 8 9 to 35 | 1 to 8 9 to 31 | Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S8/P8 can be used as general-purpose output ports when so set up by the control data. | — | O | Open |
| COM1 COM2 COM3 | 36 37 38 | 32 33 34 | Common driver outputs. The frame frequency f_O is given by: $f_O = (f_{OSC}/384)$ Hz. | — | O | Open |
| OSC | 44 | 40 | Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. | — | I/O | V_{DD} |
| CE CL DI | 46 47 48 | 42 43 44 | Serial data transfer inputs. These pins are connected to the control microprocessor. | CE: Chip enable CL: Synchronization clock DI: Transfer data | H I — | GND |
| \overline{INH} | 45 | 41 | Display off control input • \overline{INH} = low (V_{SS}): Off S1/P1 to S8/P8 = Low (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S9 to S35 = Low (V_{SS}). COM1 to COM3 = Low (V_{SS}) • \overline{INH} = high (V_{DD}): On Note that serial data transfers can be performed when the display is forced off by this pin. | L | I | GND |
| V_{LCD1} | 41 | 37 | Used to apply the LCD drive 2/3-bias voltage externally. This pin must be connected to V_{LCD2} when 1/2-bias drive is used. | — | I | Open |
| V_{LCD2} | 42 | 38 | Used to apply the LCD drive 1/3-bias voltage externally. This pin must be connected to V_{LCD1} when 1/2-bias drive is used. | — | I | Open |
| V_{DD} | 39 | 35 | Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V. | — | — | — |
| V_{LCD} | 40 | 36 | LCD driver block power supply. Provide a voltage in the range 2.7 to 6.0 V. | — | — | — |
| V_{SS} | 43 | 39 | Ground pin. Connect to ground. | — | — | — |

Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

LC75833E, 75833W, 75833JE

Serial Data Transfer Format

1. When CL is stopped at the low level

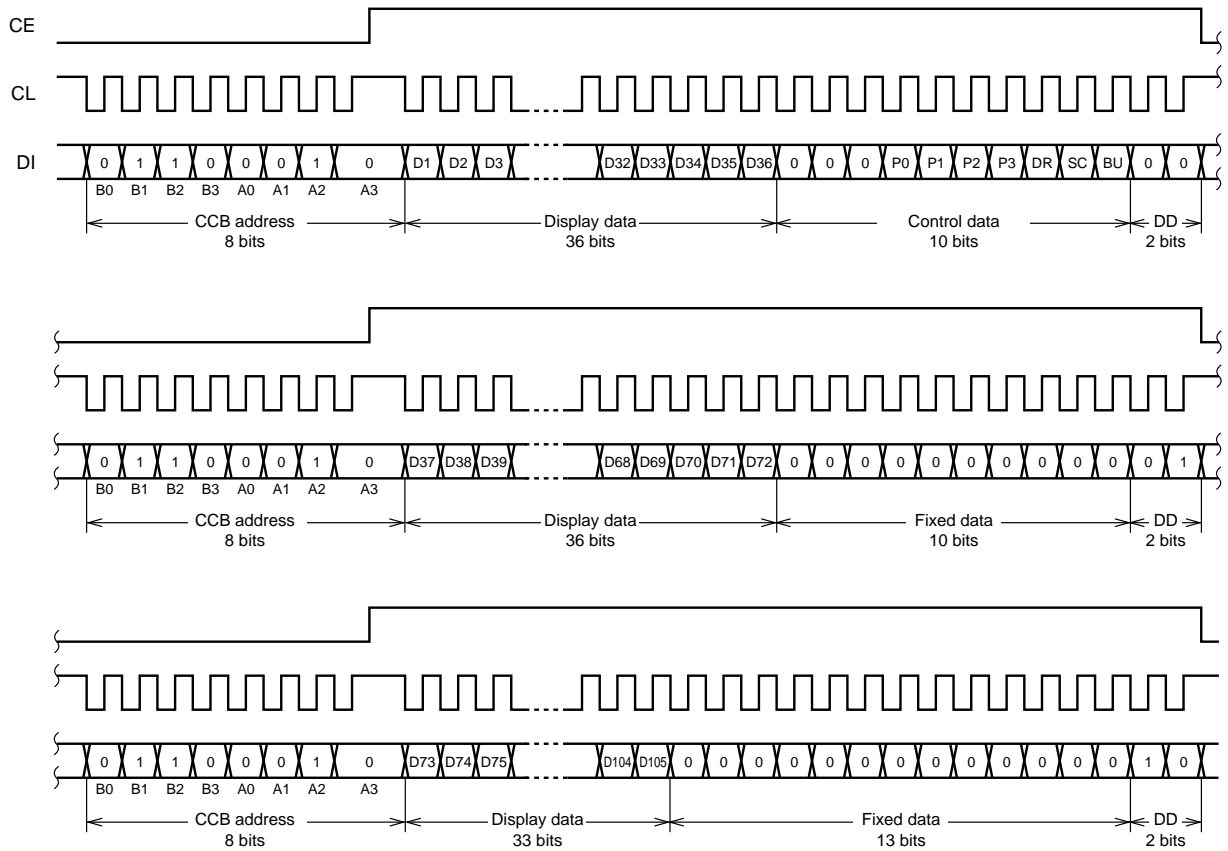


A06554

Note: DD ... Direction data

LC75833E, 75833W, 75833JE

2. When CL is stopped at the high level



A06555

Note: DD ... Direction data

- CCB address.....46H
- D1 to D105.....Display data (At the LC75833JE, the display data D34 to D36, D67 to D72, D103 to D105 must be set to 0.
- P0 to P3Segment output port/general-purpose output port switching control data
- DR1/2-bias drive or 1/3-bias drive switching control data
- SC.....Segments on/off control data
- BUNormal mode/power-saving mode control data

LC75833E, 75833W, 75833JE

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

| Output pin | Corresponding display data |
|------------|----------------------------|
| S1/P1 | D1 |
| S2/P2 | D4 |
| S3/P3 | D7 |
| S4/P4 | D10 |

| Output pin | Corresponding display data |
|------------|----------------------------|
| S5/P5 | D13 |
| S6/P6 | D16 |
| S7/P7 | D19 |
| S8/P8 | D22 |

For example, if the output pin S4/P4 has the general-purpose output port function selected, it will output a high level (V_{LCD}) when the display data D10 is 1, and will output a low level (V_{SS}) when D10 is 0.

2. **DR:** 1/2-bias drive or 1/3-bias drive switching control data

This control data bit selects either 1/2-bias drive or 1/3-bias drive.

| DR | Drive type |
|----|----------------|
| 0 | 1/3-bias drive |
| 1 | 1/2-bias drive |

3. **SC:** Segments on/off control data

This control data bit controls the on/off state of the segments.

| SC | Display state |
|----|---------------|
| 0 | On |
| 1 | Off |

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

4. **BU:** Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

| BU | Mode |
|----|--|
| 0 | Normal mode |
| 1 | Power saving mode (The OSC pin oscillator is stopped, and the common and segment output pins go to the VSS level. However, the S1/P1 to S8/P8 output pins that are set to be general-purpose output ports by the control data P0 to P3 can be used as general-purpose output ports.) |

LC75833E, 75833W, 75833JE

Display Data to Segment Output Pin Correspondence

| Segment output pin | COM1 | COM2 | COM3 |
|--------------------|------|------|------|
| S1/P1 | D1 | D2 | D3 |
| S2/P2 | D4 | D5 | D6 |
| S3/P3 | D7 | D8 | D9 |
| S4/P4 | D10 | D11 | D12 |
| S5/P5 | D13 | D14 | D15 |
| S6/P6 | D16 | D17 | D18 |
| S7/P7 | D19 | D20 | D21 |
| S8/P8 | D22 | D23 | D24 |
| S9 | D25 | D26 | D27 |
| S10 | D28 | D29 | D30 |
| S11 | D31 | D32 | D33 |
| S12 | D34 | D35 | D36 |
| S13 | D37 | D38 | D39 |
| S14 | D40 | D41 | D42 |
| S15 | D43 | D44 | D45 |
| S16 | D46 | D47 | D48 |
| S17 | D49 | D50 | D51 |
| S18 | D52 | D53 | D54 |

| Segment output pin | COM1 | COM2 | COM3 |
|--------------------|------|------|------|
| S19 | D55 | D56 | D57 |
| S20 | D58 | D59 | D60 |
| S21 | D61 | D62 | D63 |
| S22 | D64 | D65 | D66 |
| S23 | D67 | D68 | D69 |
| S24 | D70 | D71 | D72 |
| S25 | D73 | D74 | D75 |
| S26 | D76 | D77 | D78 |
| S27 | D79 | D80 | D81 |
| S28 | D82 | D83 | D84 |
| S29 | D85 | D86 | D87 |
| S30 | D88 | D89 | D90 |
| S31 | D91 | D92 | D93 |
| S32 | D94 | D95 | D96 |
| S33 | D97 | D98 | D99 |
| S34 | D100 | D101 | D102 |
| S35 | D103 | D104 | D105 |

Note: This applies to the case where the S1/P1 to S8/P8 output pins are set to be segment output ports.

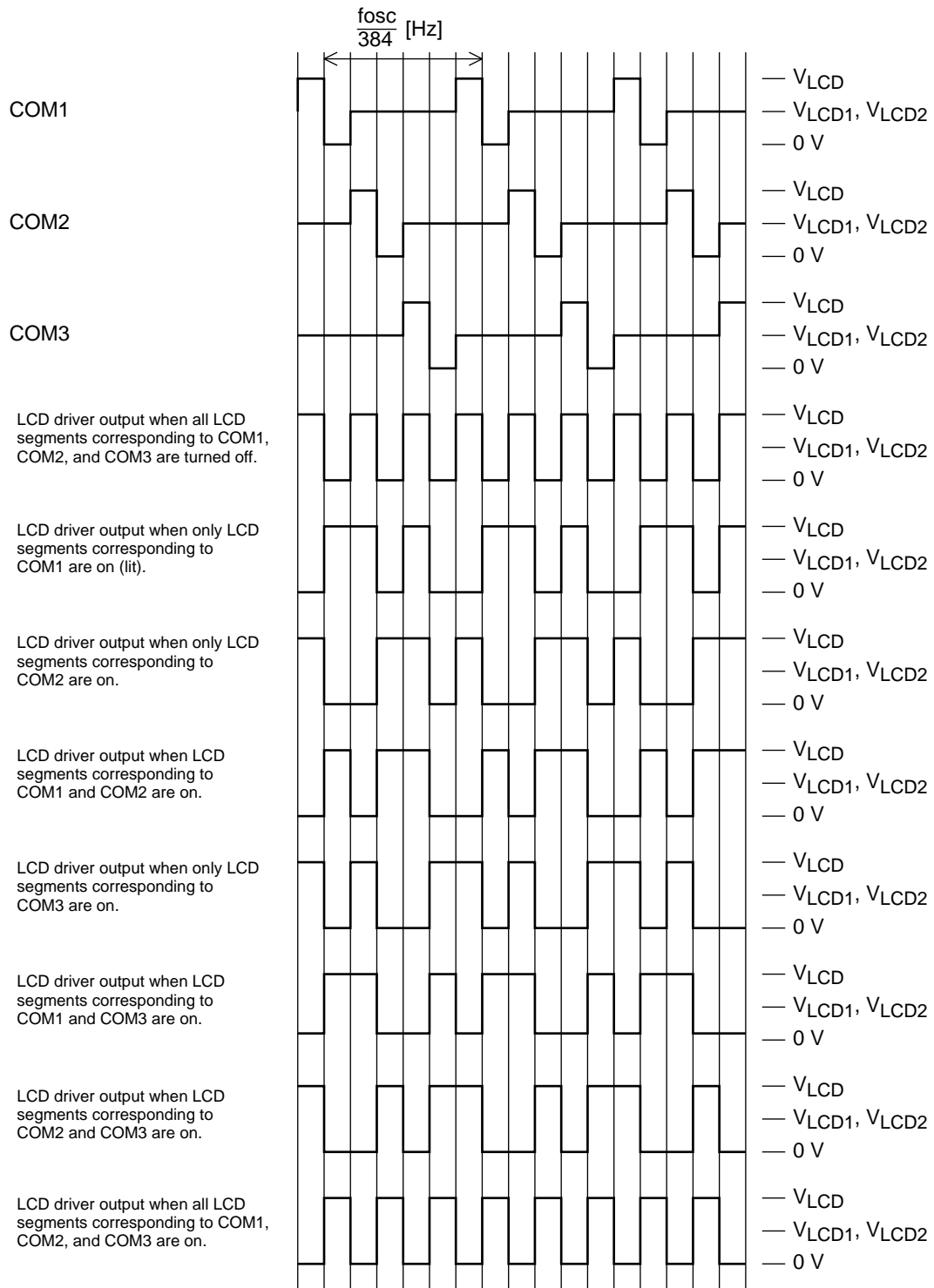
The LC75833JE do not have the S12, S23, S24, S35 output pins.

For example, the table below lists the segment output states for the S11 output pin.

| Display data | | | Segment output pin (S11) state |
|--------------|-----|-----|---|
| D31 | D32 | D33 | |
| 0 | 0 | 0 | The LCD segments corresponding to COM1 to COM3 are off. |
| 0 | 0 | 1 | The LCD segments corresponding to COM3 is on. |
| 0 | 1 | 0 | The LCD segments corresponding to COM2 is on. |
| 0 | 1 | 1 | The LCD segments corresponding to COM2 and COM3 are on. |
| 1 | 0 | 0 | The LCD segments corresponding to COM1 is on. |
| 1 | 0 | 1 | The LCD segments corresponding to COM1 and COM3 are on. |
| 1 | 1 | 0 | The LCD segments corresponding to COM1 and COM2 are on. |
| 1 | 1 | 1 | The LCD segments corresponding to COM1 to COM3 are on. |

LC75833E, 75833W, 75833JE

1/3-Duty 1/2-Bias Drive Technique

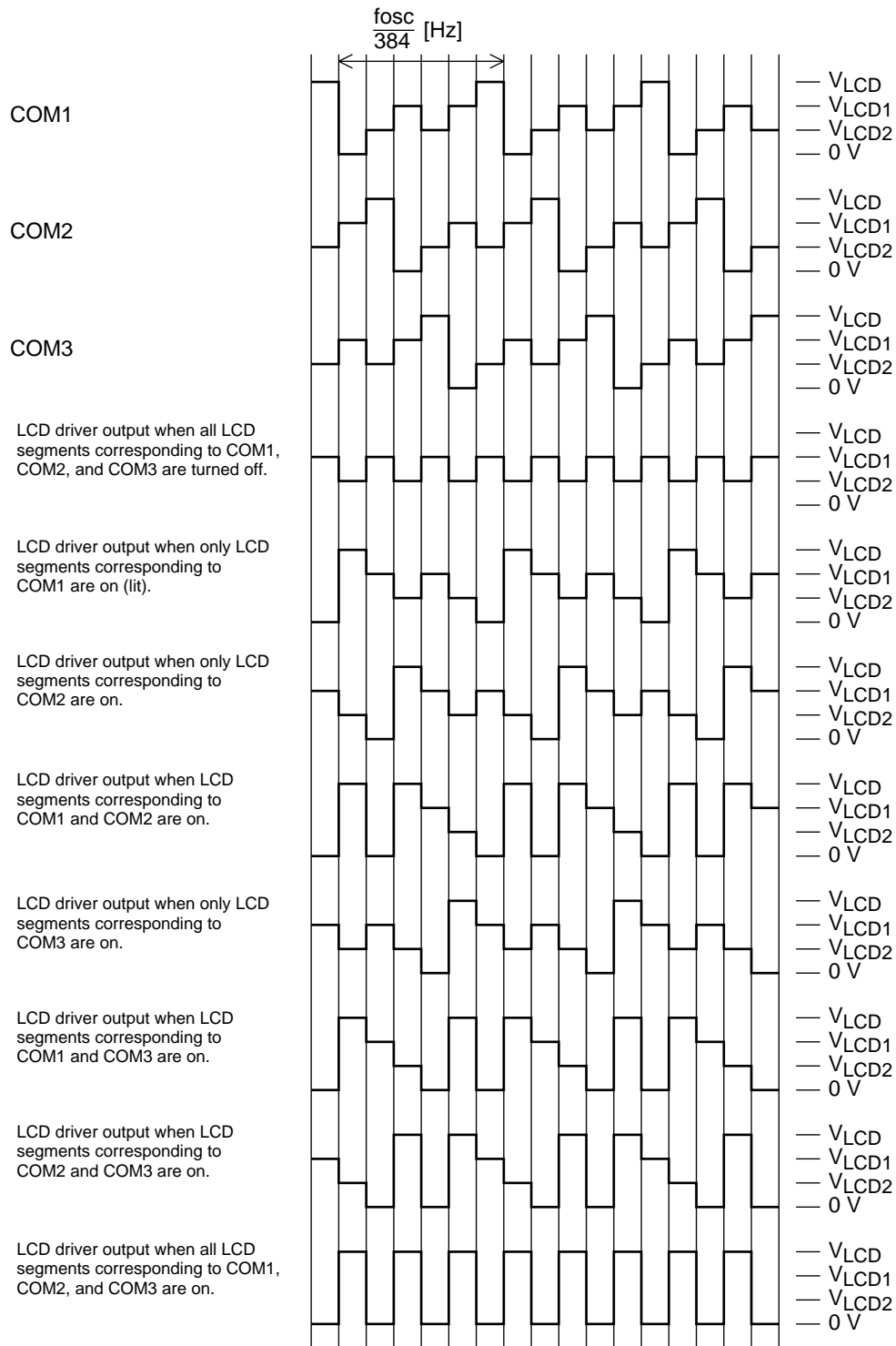


A06558

1/3-Duty 1/2-Bias Waveforms

LC75833E, 75833W, 75833JE

1/3-Duty 1/3-Bias Technique



A06559

1/3-Duty 1/3-Bias Waveforms

LC75833E, 75833W, 75833JE

The $\overline{\text{INH}}$ pin and Display Control

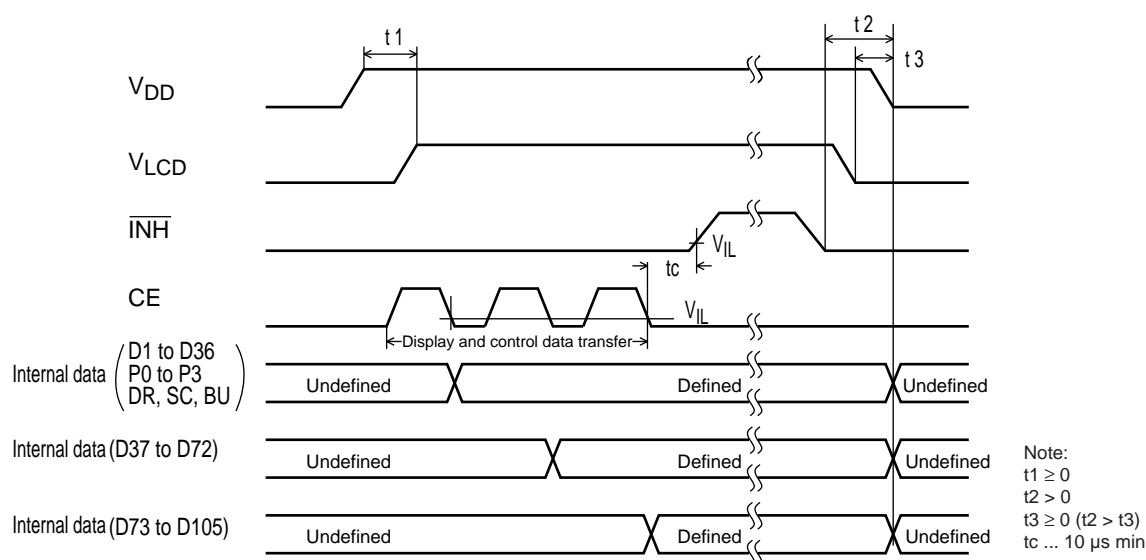
Since the LSI internal data (the display data and the control data) is undefined when power is first applied, applications should set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display (LC75833E, LC75833W: This sets the S1/P1 to S8/P8, S9 to S35, and COM1 to COM3 to the V_{SS} level. LC75833JE: This sets the S1/P1 to S8/P8, S9 to S11, S13 to S22, S25 to S34, and COM1 to COM3 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{\text{INH}}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figure 3.)

Notes on the Power On/Off Sequences

Applications should observe the following sequence when turning the LC75833E, LC75833W, and LC75833JE power on and off.

- At power on: Logic block power supply (V_{DD}) on \rightarrow LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off \rightarrow Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.



Note: At the LC75833JE, the display data D34 to D36, D67 to D72, D103 to D105 must be set to 0.

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Figure 3

Notes on Controller Transfer of Display Data

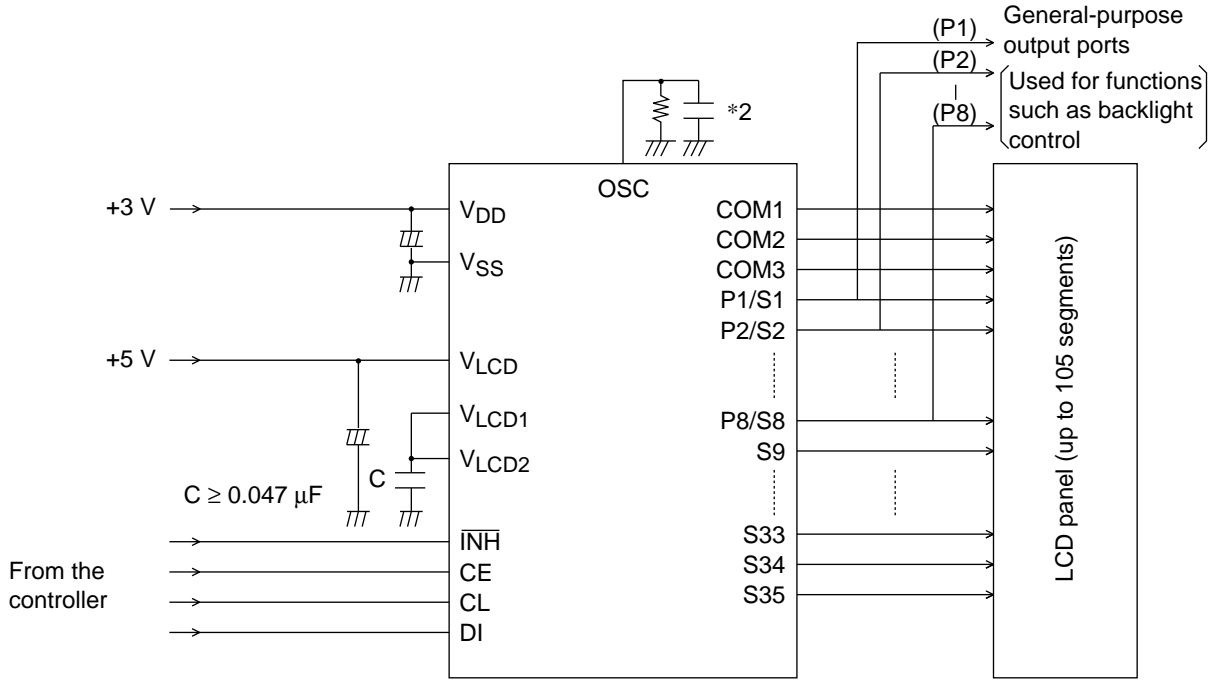
Since the LC75833E, LC75833W, and LC75833JE accept display data divided into three separate transfer operations, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

LC75833E, 75833W, 75833JE

Sample Application Circuit 1

1/2 Bias (for use with normal size panels)

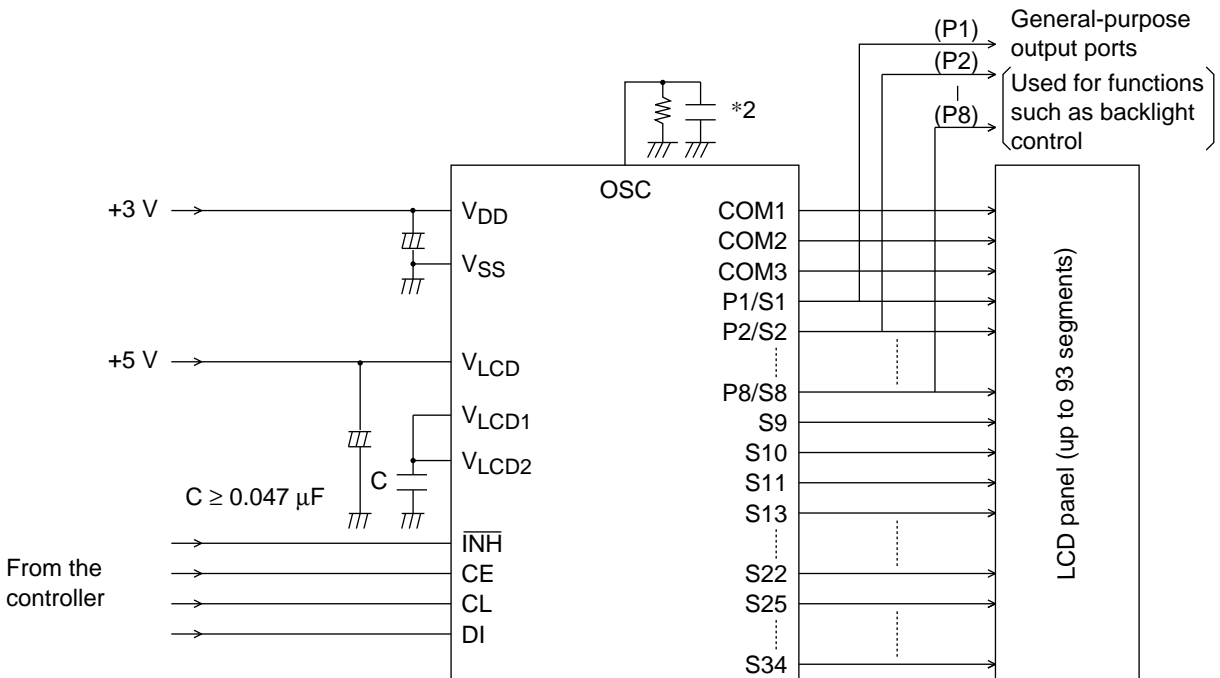
- LC75833E, LC75833W



A06561

Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE



A06583

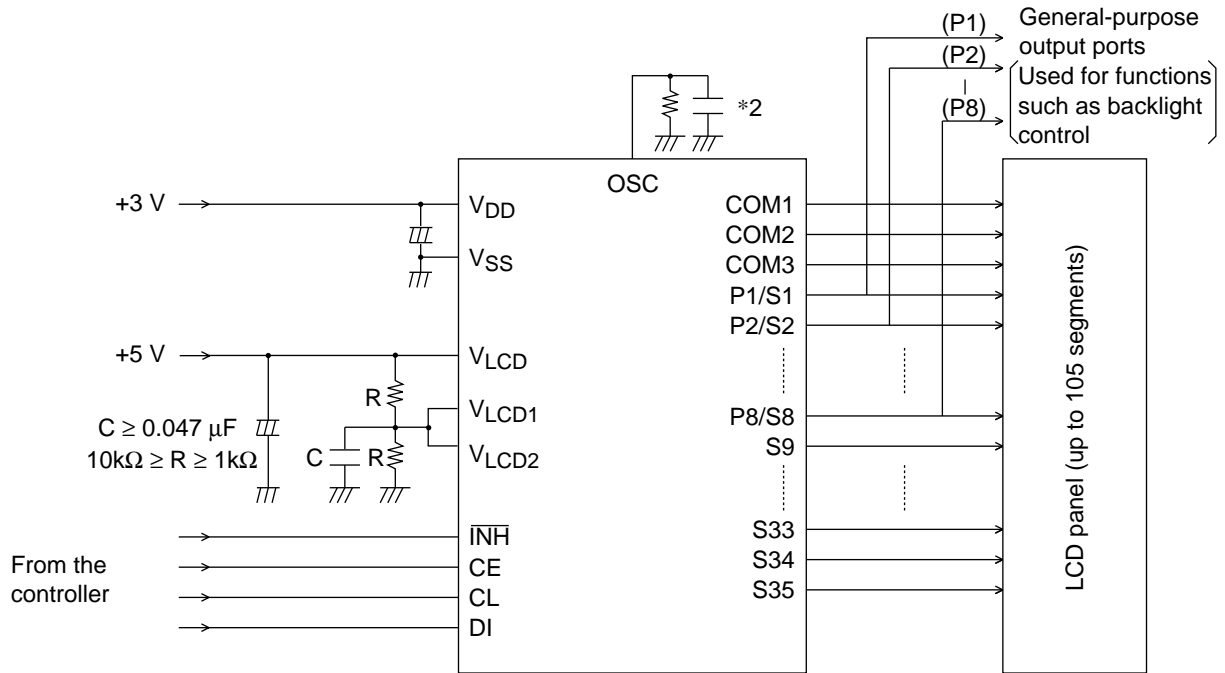
Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

LC75833E, 75833W, 75833JE

Sample Application Circuit 2

1/2 Bias (for use with large panels)

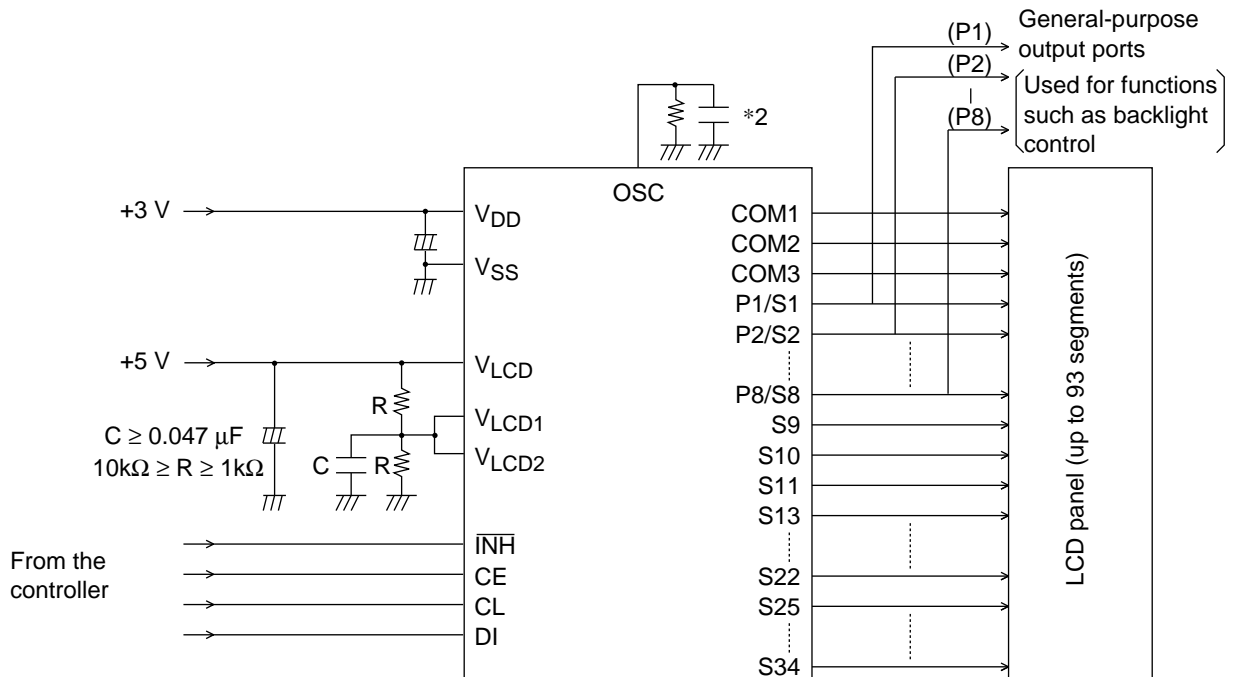
- LC75833E, LC75833W



A06562

Note: *2 When a capacitor except the recommended external capacitance ($C_{OSC} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE



A06584

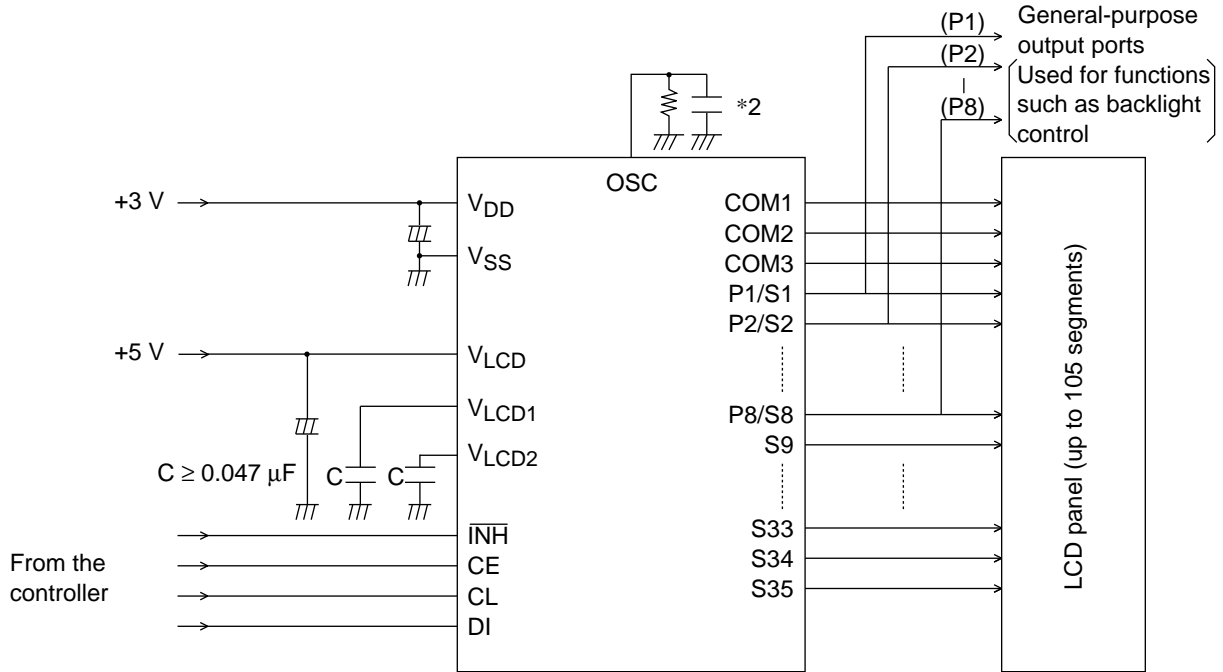
Note: *2 When a capacitor except the recommended external capacitance ($C_{OSC} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

LC75833E, 75833W, 75833JE

Sample Application Circuit 3

1/3 Bias (for use with normal size panels)

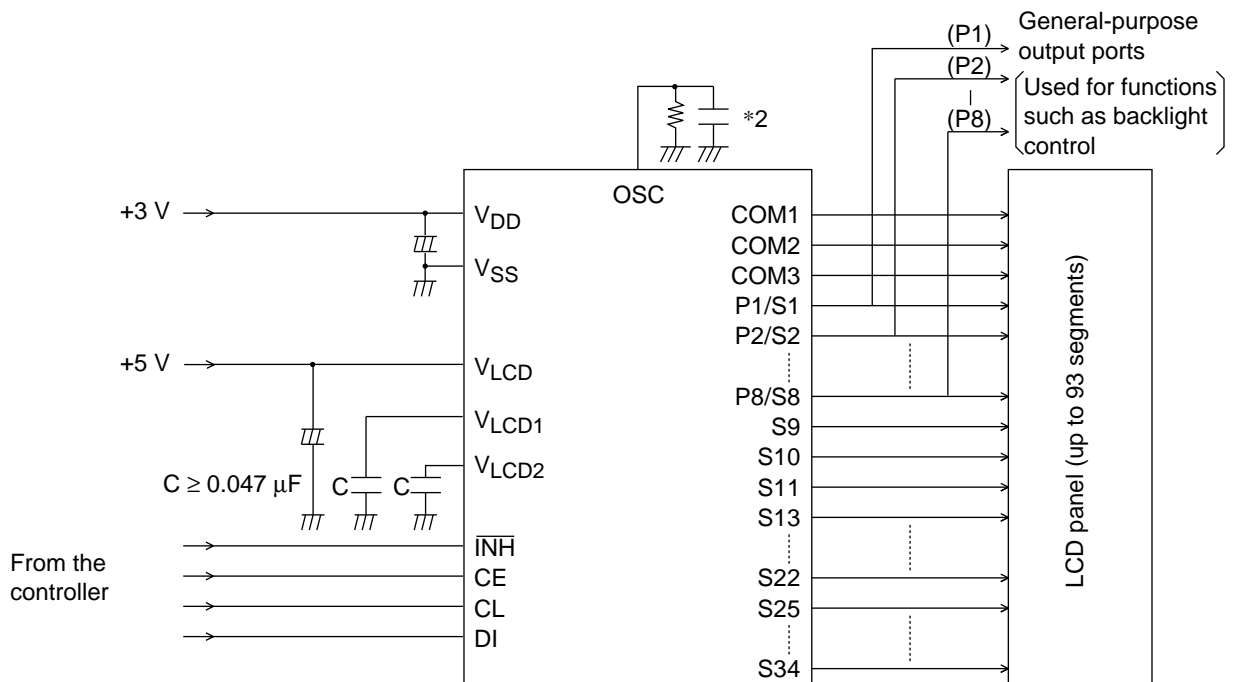
- LC75833E, LC75833W



A06562

Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE



A06584

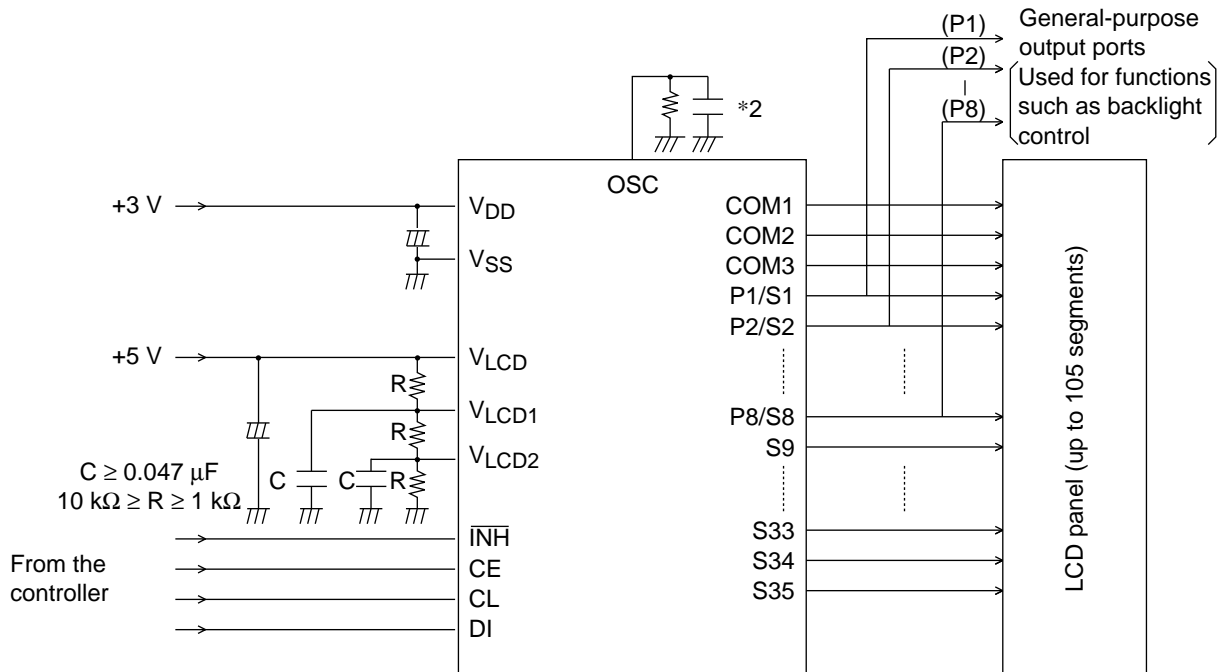
Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

LC75833E, 75833W, 75833JE

Sample Application Circuit 4

1/3 Bias (for use with large panels)

- LC75833E, LC75833W

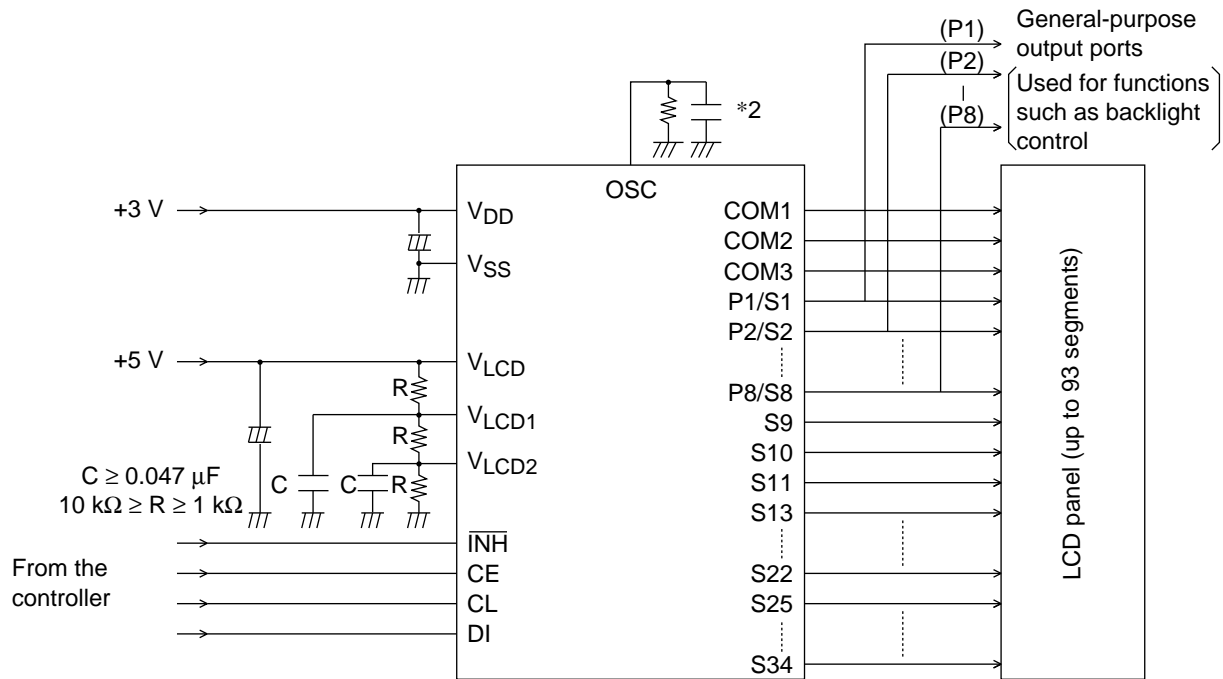


A06563

Note: *2 When a capacitor except the recommended external capacitance ($C_{OSC} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

LC75833E, 75833W, 75833JE

• LC75833JE



A06585

Note: *2 When a capacitor except the recommended external capacitance ($C_{OSC} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

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