LM317LZRAG Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	LM317LZRAG-DG
Manufacturer	onsemi
Manufacturer Product Number	LM317LZRAG
Description	IC REG LINEAR POS ADJ 100MA TO92
Detailed Description	Linear Voltage Regulator IC Positive Adjustable 1 Output 100mA TO-92 (TO-226)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
LM317LZRAG	onsemi
Series:	Product Status:
-	Active
Output Configuration:	Output Type:
Positive	Adjustable
Number of Regulators:	Voltage - Input (Max):
1	40V
Voltage - Output (Min/Fixed):	Voltage - Output (Max):
1.2V	37V
Voltage Dropout (Max):	Current - Output:
-	100mA
Current - Quiescent (Iq):	PSRR:
10 mA	80dB (120Hz)
Control Features:	Protection Features:
-	Over Current, Over Temperature, Short Circuit
Operating Temperature:	Mounting Type:
0°C ~ 125°C	Through Hole
Package / Case:	Supplier Device Package:
TO-226-3, TO-92-3 Long Body (Formed Leads)	TO-92 (TO-226)
Base Product Number:	
LM317	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	Not Applicable
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

Voltage Regulator - Adjustable Output, Positive
100 mA

LM317L, NCV317L

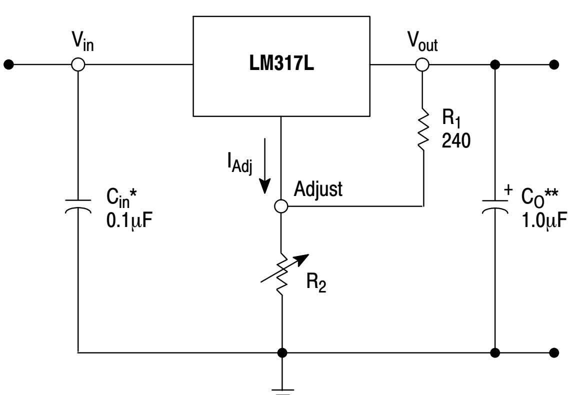
The LM317L is an adjustable 3−terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow−out proof.

The LM317L serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator.

Features

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe−Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3−Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Simplified Application



* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

ON Semiconductor®

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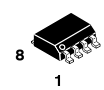
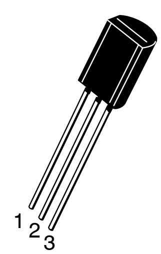
LOW CURRENT THREE−TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

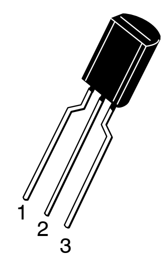


SOIC−8
D SUFFIX
CASE 751

Pin 1. V_{in}
2. V_{out}
3. V_{out}
4. Adjust
5. N.C.
6. V_{out}
7. V_{out}
8. N.C.



STRAIGHT LEAD



BENT LEAD

TO−92
Z SUFFIX
CASE 29−10

Pin 1. Adjust
2. V_{out}
3. V_{in}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input−Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation Case 29 (TO−92) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case Case 751 (SOIC−8) (Note 1) T_A = 25°C Thermal Resistance, Junction−to−Ambient Thermal Resistance, Junction−to−Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 160 83 Internally Limited 180 45	 W °C/W °C/W W °C/W °C/W
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. SOIC−8 Junction−to−Ambient Thermal Resistance is for minimum recommended pad size. Refer to Figure 24 for Thermal Resistance variation versus pad size.
2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model, 2000 V per MIL STD 883, Method 3015.
   Machine Model Method, 200 V.

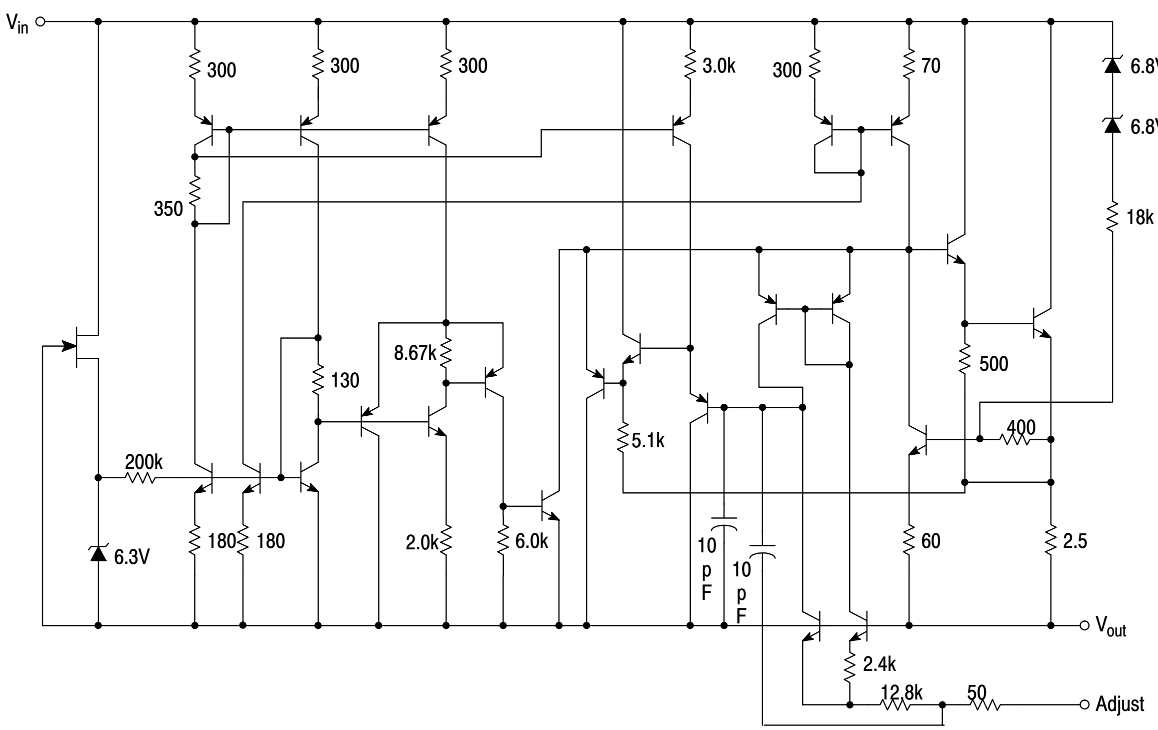


Figure 1. Representative Schematic Diagram

ELECTRICAL CHARACTERISTICS

(V_I–V_O = 5.0 V; I_O = 40 mA; T_J = T_{low} to T_{high} (Note 3); I_{max} and P_{max} (Note 4); unless otherwise noted.)

Characteristics	Figure	Symbol	LM317L, LB, NCV317LB Min	Typ	Max	Unit
Line Regulation (Note 5) T_A = 25°C, 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 5), T_A = 25°C 10 mA ≤ I_O ≤ I_{max} – LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} – LM317L	1, 2	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage 3.0 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} – LM317L	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 5), 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 5) 10 mA ≤ I_O ≤ I_{max} – LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 – –	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation (V_I – V_O = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current V_I – V_O ≤ 6.25 V, P_D ≤ P_{max}, Z Package V_I – V_O ≤ 40 V, P_D ≤ P_{max}, T_A = 25°C, Z Package	3	I_{max}	 100 –	 200 20	 – –	mA
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	–	N	–	0.003	–	% V_O
Ripple Rejection (Note 6) V_O = 1.2 V, f = 120 Hz C_{Adj} = 10 μF, V_O = 10.0 V	4	RR	 60 –	 80 80	 – –	dB
Thermal Shutdown (Note 7)	–	–	–	180	–	°C
Long Term Stability, T_J = T_{high} (Note 8) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.

3. T_{low} to T_{high} = 0° to +125°C for LM317L −40° to +125°C for LM317LB, NCV317LB
4. I_{max} = 100 mA P_{max} = 625 mW
5. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
6. C_{Adj}, when used, is connected between the adjustment pin and ground.
7. Thermal characteristics are not subject to production test.
8. Since Long−Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

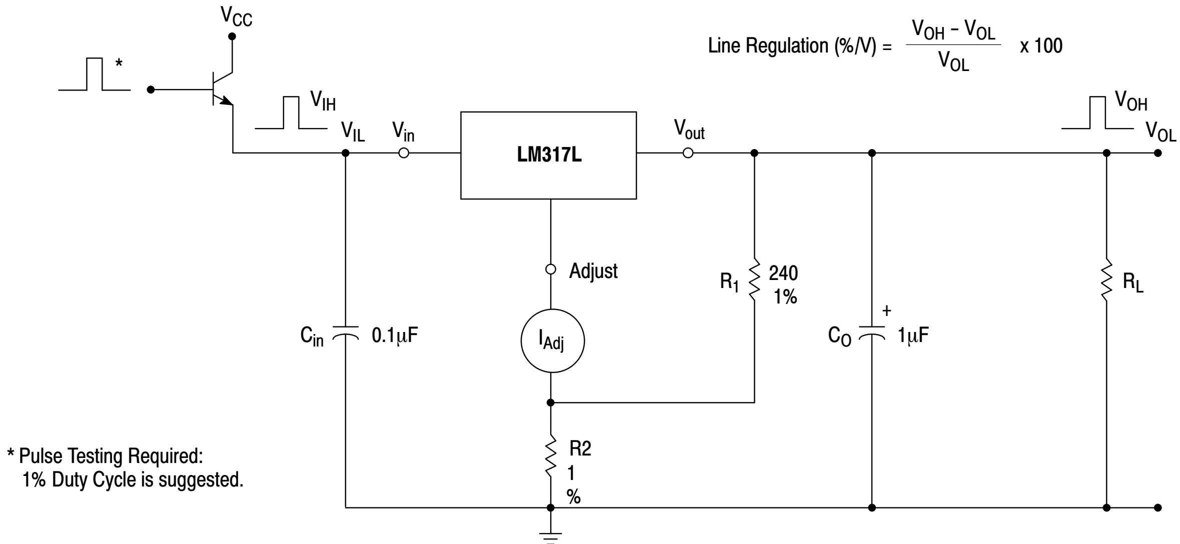


Figure 2. Line Regulation and ΔI_{Adj}/Line Test Circuit

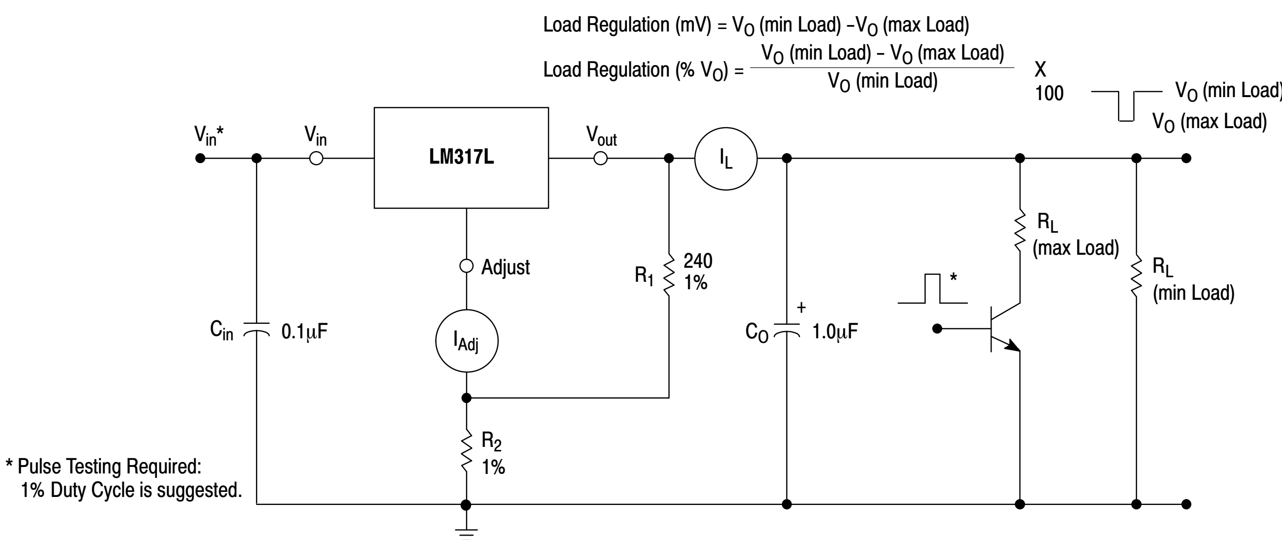


Figure 3. Load Regulation and ΔI_{Adj}/Load Test Circuit

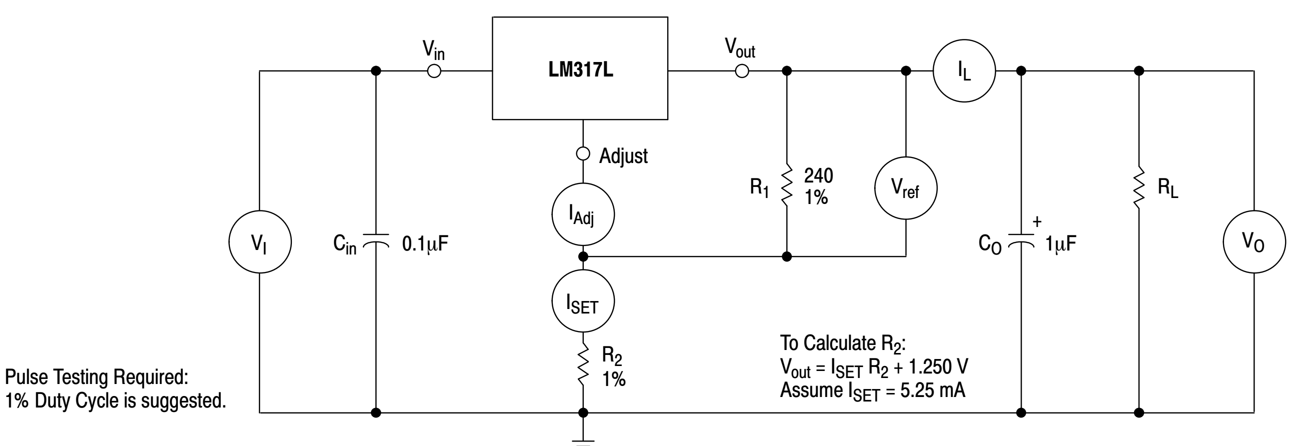


Figure 4. Standard Test Circuit

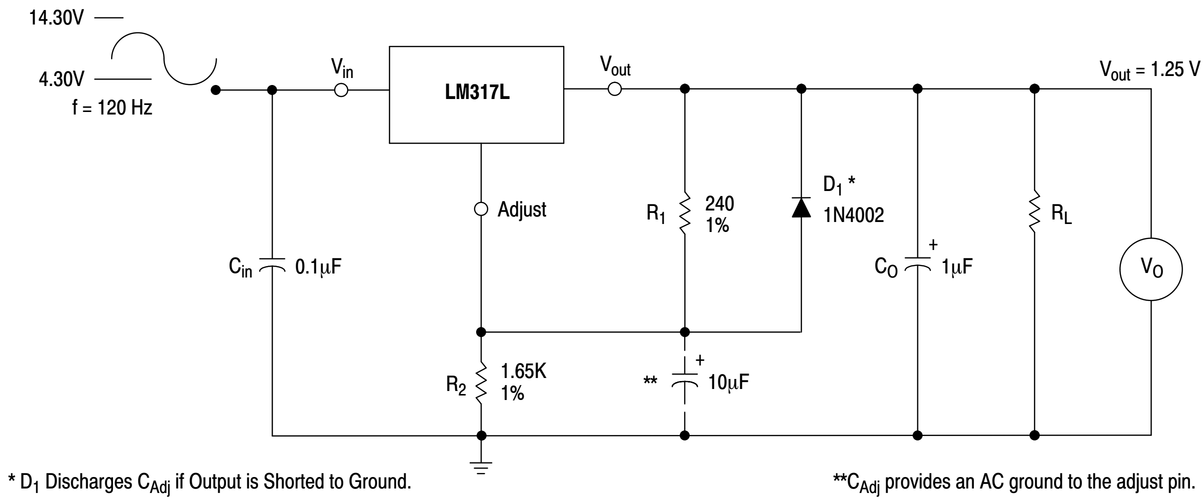


Figure 5. Ripple Rejection Test Circuit

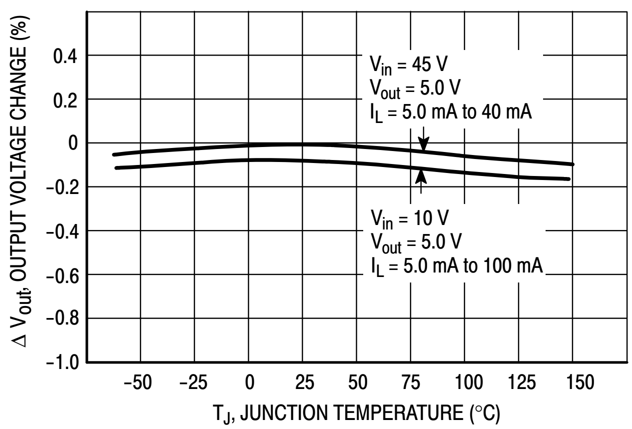


Figure 6. Load Regulation

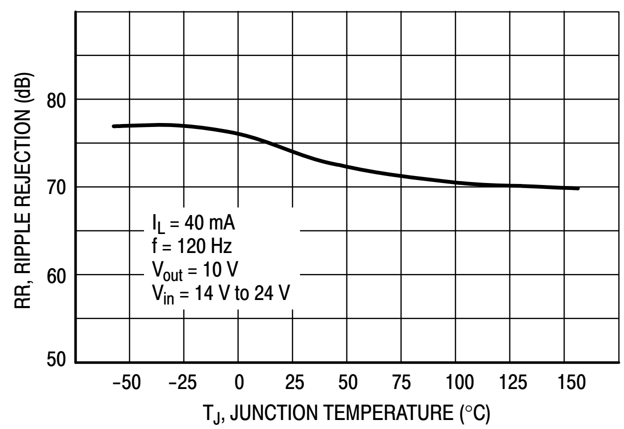


Figure 7. Ripple Rejection

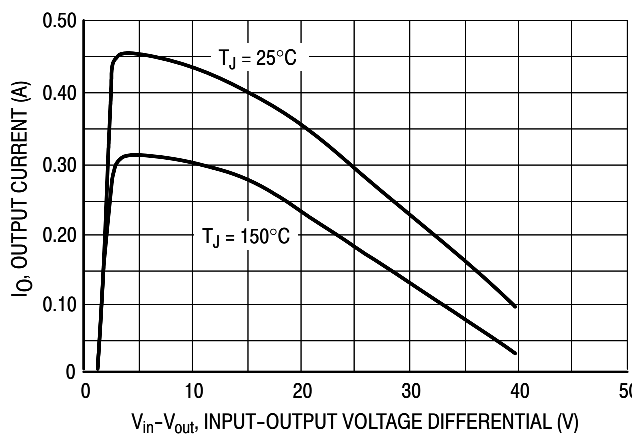


Figure 8. Current Limit

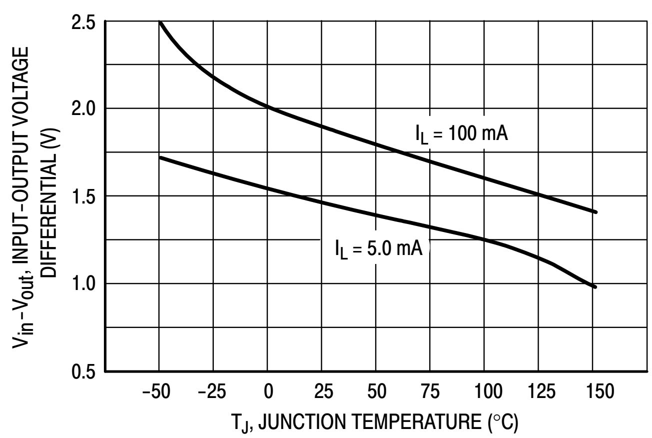


Figure 9. Dropout Voltage

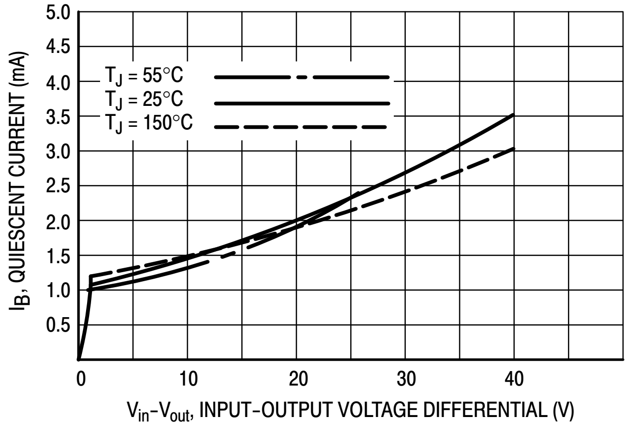


Figure 10. Minimum Operating Current

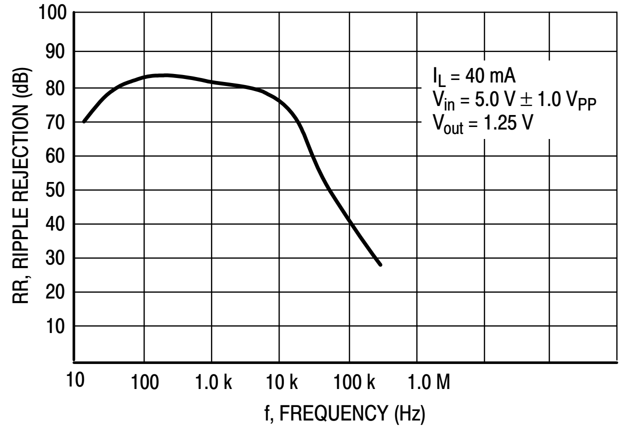


Figure 11. Ripple Rejection versus Frequency

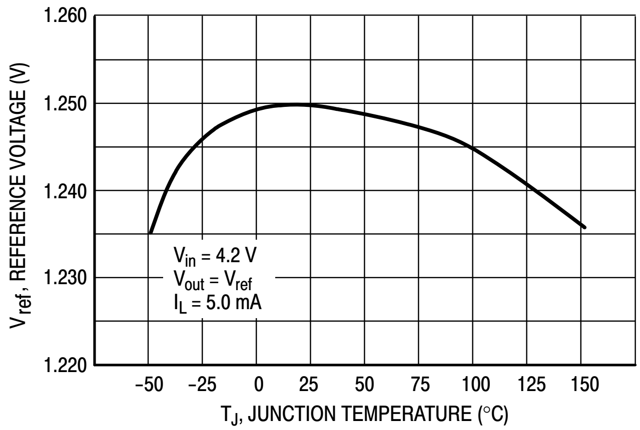


Figure 12. Temperature Stability

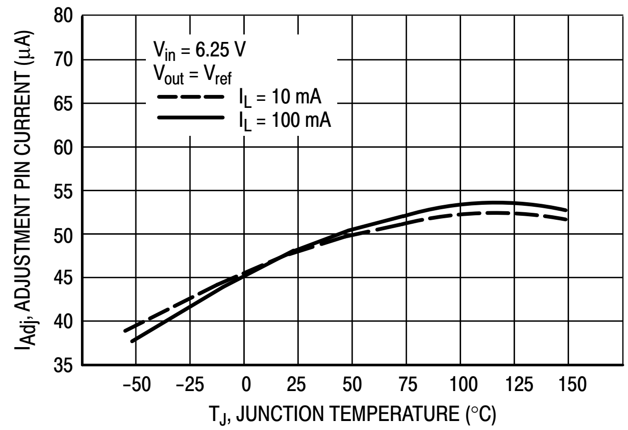


Figure 13. Adjustment Pin Current

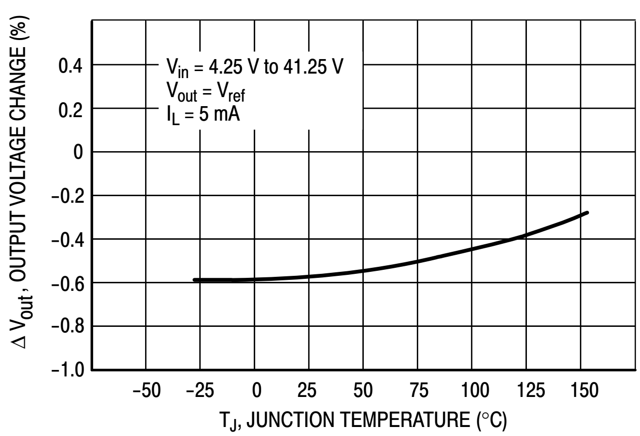


Figure 14. Line Regulation

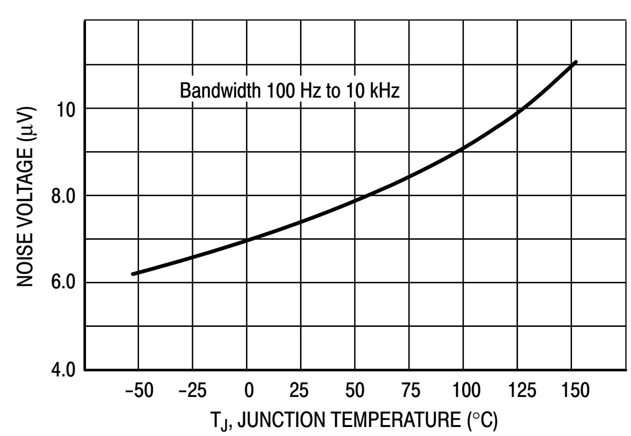


Figure 15. Output Noise

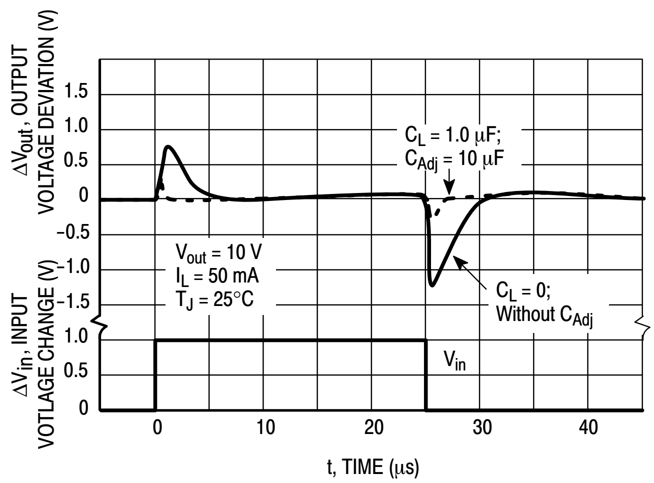


Figure 16. Line Transient Response

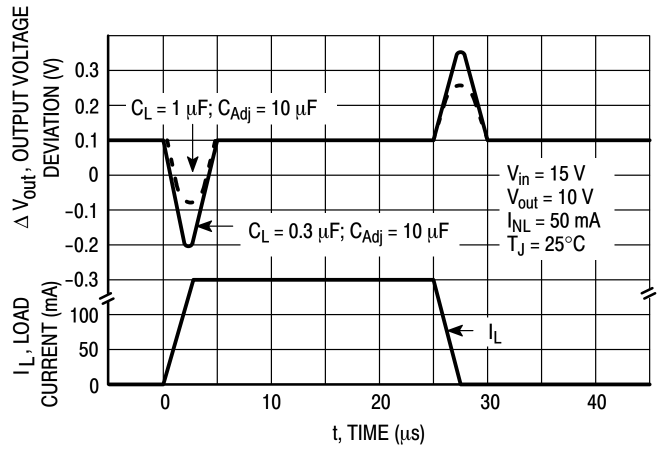


Figure 17. Load Transient Response

APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317L is a 3−terminal floating regulator. In operation, the LM317L develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 13), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

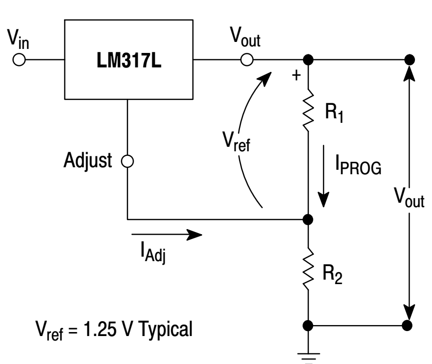


Figure 18. Basic Circuit Configuration

Load Regulation

The LM317L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM317L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 10 µF, C_{Adj} > 5.0 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

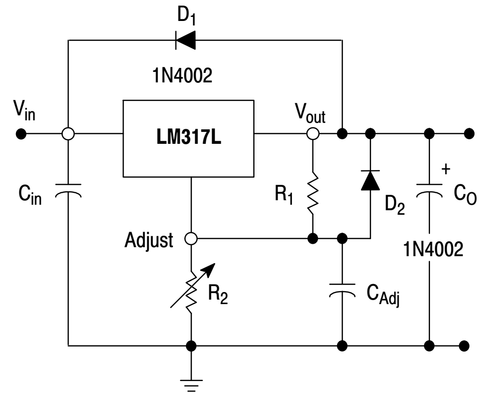
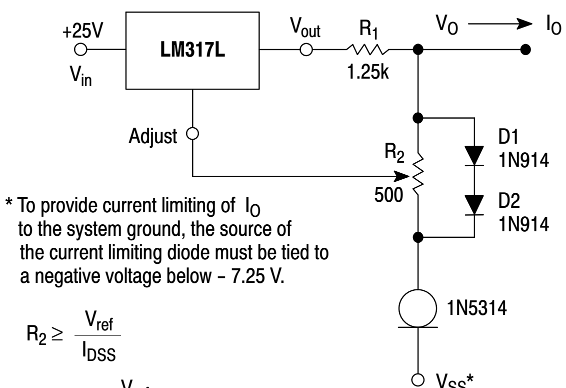


Figure 19. Voltage Regulator with Protection Diodes

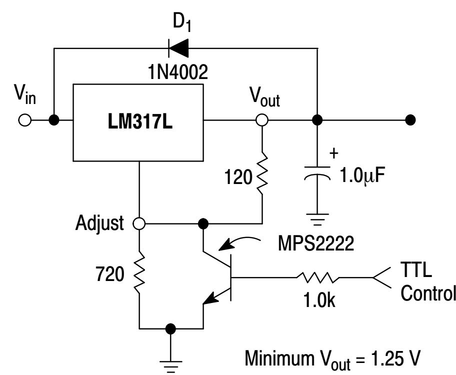


$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\text{ V} + V_{SS}$
$I_{Lmin} - I_P < I_O < 100\text{ mA} - I_P$
As shown $0 < I_O < 95$ mA

Figure 20. Adjustable Current Limiter



D_1 protects the device during an input short circuit.

Figure 21. 5.0 V Electronic Shutdown Regulator

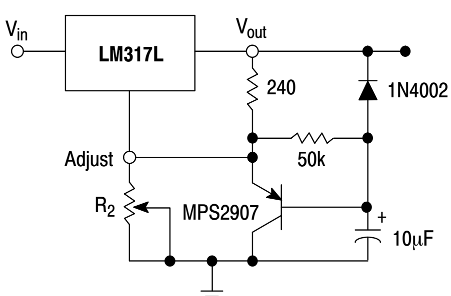
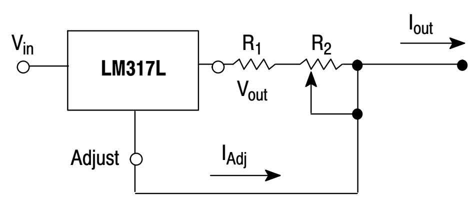


Figure 22. Slow Turn−On Regulator



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\text{ V}}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\text{ V}}{R_1 + R_2}$$

$5.0\text{ mA} < I_{out} < 100\text{ mA}$

Figure 23. Current Regulator

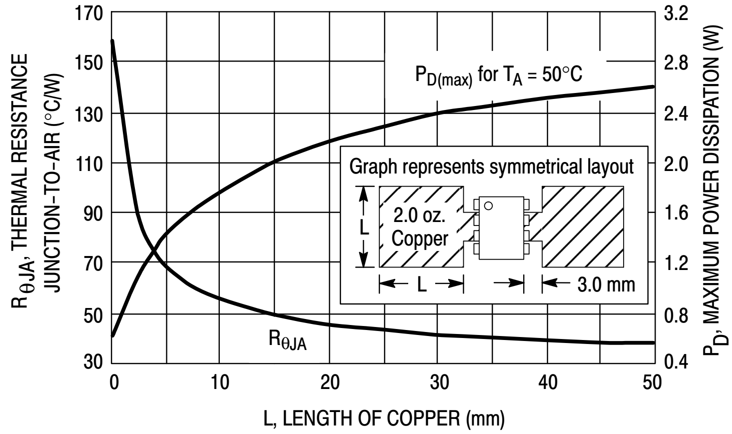
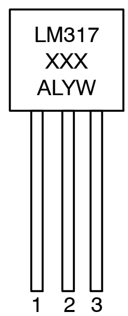


Figure 24. SOP−8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

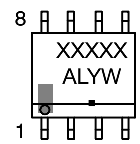
MARKING DIAGRAMS

TO−92
CASE 29−10



XXX = LBZ, LZ, LZR
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

SOIC−8
CASE 751



XXXXX = 317LB, LM317
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
LM317LBDG		SOIC−8 (Pb−Free)	98 Units / Rail
LM317LBDR2G		SOIC−8 (Pb−Free)	2500/Tape & Reel
LM317LBZG		TO−92 (Pb−Free)	2000 Units / Bag
LM317LBZRAG		TO−92 (Pb−Free)	2000 Tape & Reel
LM317LBZRPG	T_J = −40°C to +125°C	TO−92 (Pb−Free)	2000 Ammo Pack
NCV317LBDG*		SOIC−8 (Pb−Free)	98 Units / Rail
NCV317LBDR2G*		SOIC−8 (Pb−Free)	2500/Tape & Reel
NCV317LBZG*		TO−92 (Pb−Free)	2000 Units / Bag
NCV317LBZRAG*		TO−92 (Pb−Free)	2000 Tape & Reel
LM317LDG		SOIC−8 (Pb−Free)	98 Units / Rail
LM317LDR2G		SOIC−8 (Pb−Free)	2500/Tape & Reel
LM317LZG		TO−92 (Pb−Free)	2000 Units / Bag
LM317LZRAG	T_J = 0°C to +125°C	TO−92 (Pb−Free)	2000 Tape & Reel
LM317LZREG		TO−92 (Pb−Free)	2000 Tape & Reel
LM317LZRMG		TO−92 (Pb−Free)	2000 Ammo Pack
LM317LZRPG		TO−92 (Pb−Free)	2000 Ammo Pack

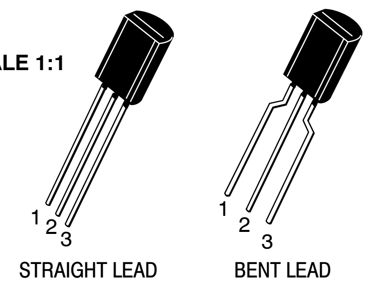
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV devices: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

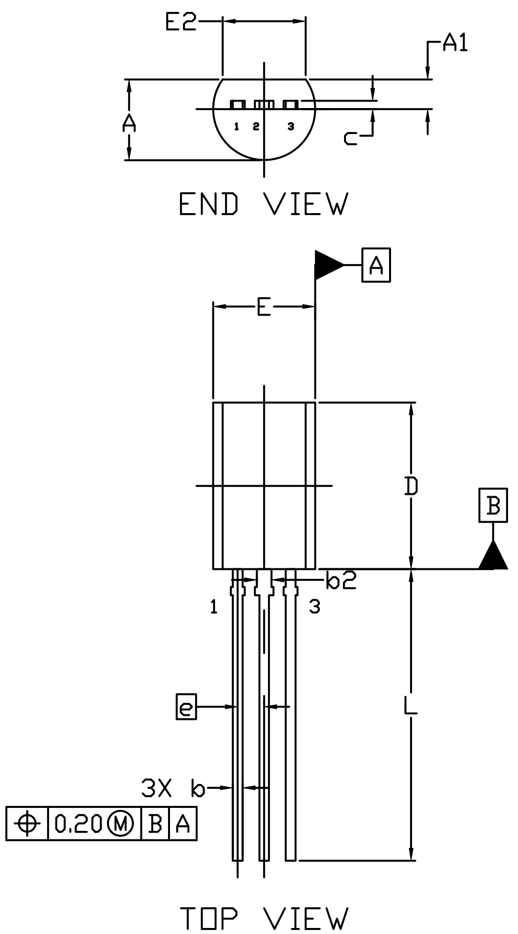
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

SCALE 1:1



STRAIGHT LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

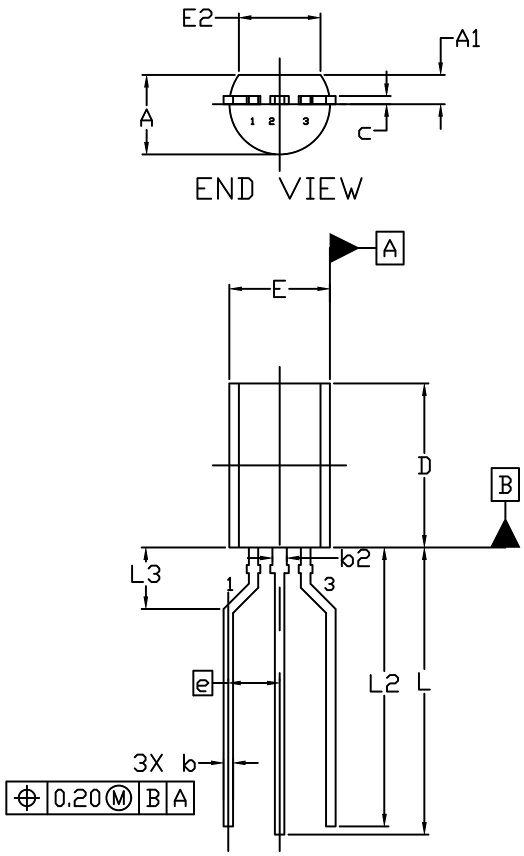
STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 2 OF 3**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC
MARKING DIAGRAM*

XXXXX
XXXXX
ALYW▪
▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

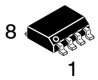
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TO−92 (TO−226) 1 WATT	PAGE 3 OF 3

onsemi

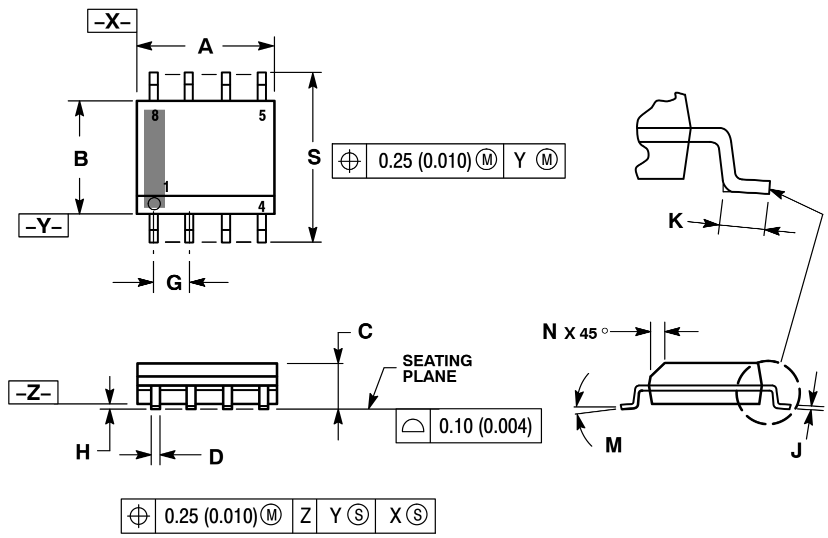
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

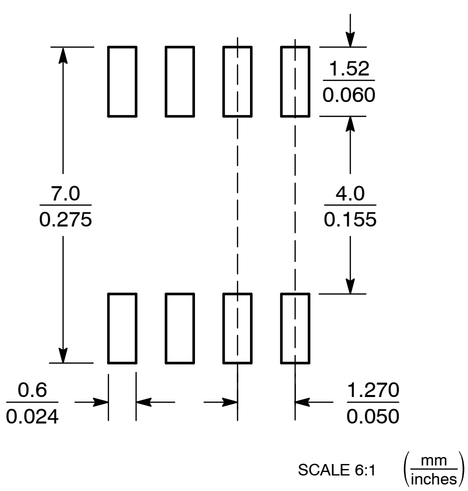
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

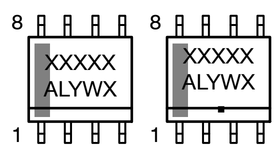
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

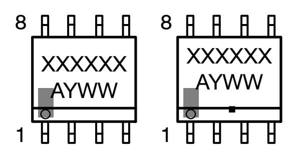


*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)**



Discrete **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 2 OF 2**

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