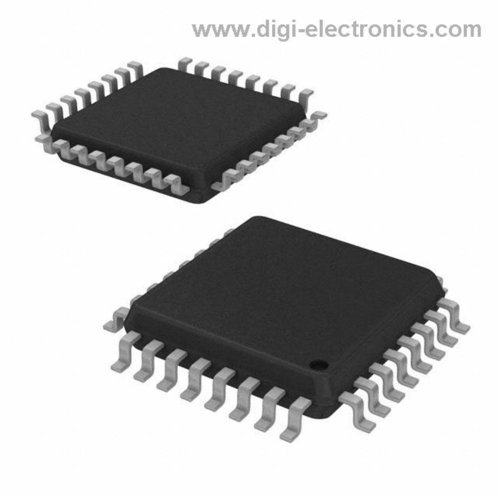
MC100EP210SFAG Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MC100EP210SFAG-DG
Manufacturer	onsemi
Manufacturer Product Number	MC100EP210SFAG
Description	IC CLK BUFFER 1:5 1GHZ 32LQFP
Detailed Description	Clock Fanout Buffer (Distribution) IC 1:5 1 GHz 32-LQFP

Purchase and inquiry

Manufacturer Product Number: MC100EP210SFAG

Manufacturer: onsemi

Series: 100EP

Product Status: Active

Type: Fanout Buffer (Distribution)

Number of Circuits: 2

Ratio - Input:Output: 1:5

Differential - Input:Output: Yes/Yes

Input: LVDS, LVPECL

Output: LVDS

Frequency - Max: 1 GHz

Voltage - Supply: 2.375V ~ 2.625V

Operating Temperature: -40°C ~ 85°C

Mounting Type: Surface Mount

Package / Case: 32-LQFP

Supplier Device Package: 32-LQFP (7x7)

Base Product Number: MC100EP210

Environmental & Export classification

RoHS Status: ROHS3 Compliant

Moisture Sensitivity Level (MSL): 2 (1 Year)

REACH Status: REACH Unaffected

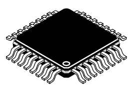
ECCN: EAR99

HTSUS: 8542.39.0001

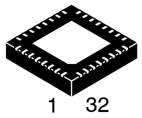
DATA SHEET
www.onsemi.com

2.5 V 1:5 Dual Differential LVDS Compatible Clock Driver

MC100EP210S



LQFP−32
FA SUFFIX
CASE 561AB



QFN32
MN SUFFIX
CASE 488AM

Description

The MC100EP210S is a low skew 1−to−5 dual differential driver, designed with LVDS clock distribution in mind. The LVDS or LVPECL input signals are differential and the signal is fanned out to five identical differential LVDS outputs.

The EP210S specifically guarantees low output−to−output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

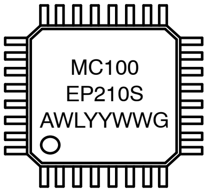
Two internal 50 Ω resistors are provided across the inputs. For LVDS inputs, VTA and VTB pins should be unconnected. For LVPECL inputs, VTA and VTB pins should be connected to the V_{TT} (V_{CC} − 2.0 V) supply.

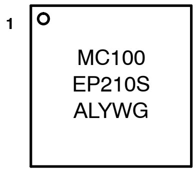
Designers can take advantage of the EP210S performance to distribute low skew LVDS clocks across the backplane or the board.

Features

- 20 ps Typical Output−to−Output Skew
- 85 ps Typical Device−to−Device Skew
- 550 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Maximum Frequency > 1 GHz Typical
- Operating Range: V_{CC} = 2.375 V to 2.625 V with V_{EE} = 0 V
- Internal 50 Ω Input Termination Resistors
- LVDS Input/Output Compatible
- These are Pb−Free Devices

MARKING DIAGRAM





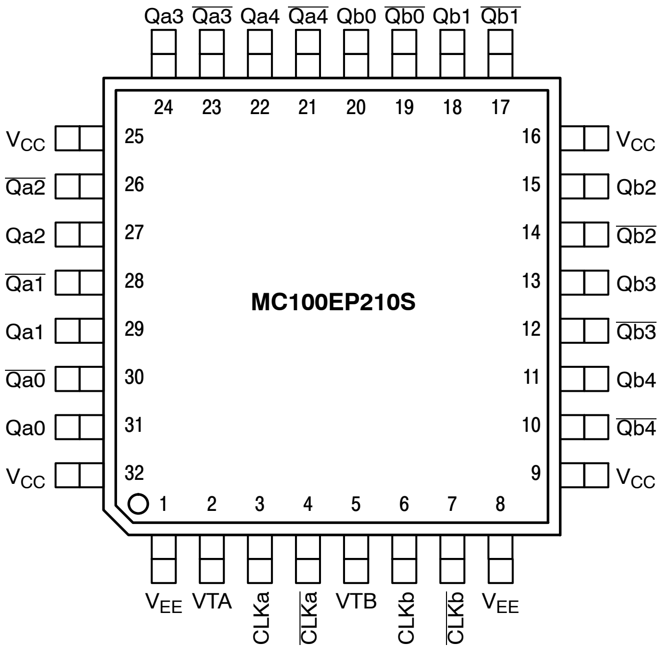
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

January, 2024 − Rev. 11



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32–Lead LQFP Pinout (Top View)

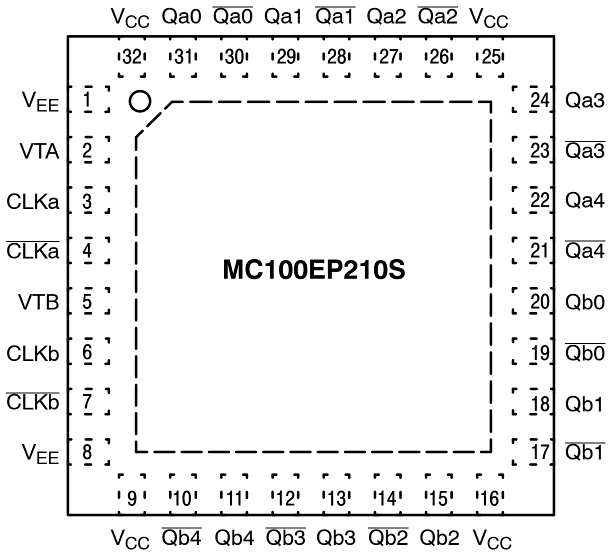


Figure 1. 32–Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLKn, $\overline{CLKn}$	LVDS, LVPECL CLK Inputs*
Qn0:4, $\overline{Qn0:4}$	LVDS Outputs
VTA	50 Ω Termination Resistors
VTB	50 Ω Termination Resistors
V_{CC}	Positive Supply
V_{EE}	Ground
EP for QFN–32, only	The Exposed Pad (EP) on the QFN–32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat–sinking conduit. The pad is electrically connected to V_{EE}.

*Under open or floating conditions with input pins converging to a common termination bias voltage the device is susceptible to auto oscillation.

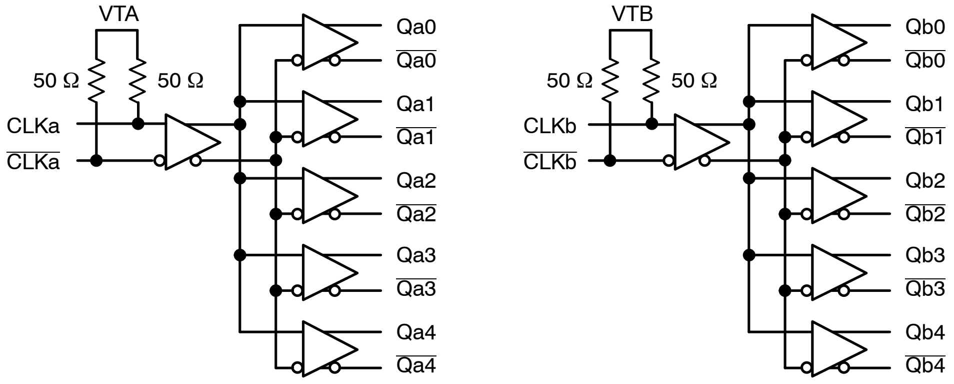


Figure 2. Logic Diagram

Table 2. ATTRIBUTES

Characteristics		Value	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	LQFP−32 QFN−32	Level 2	Level 2 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		461 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, refer to Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Power Supply (GND)	V_{CC} = 2.5 V		−6	V
V_I	LVDS, LVPECL Input Voltage	V_{EE} = 0 V	$V_I \leq V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	32 LQFP	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. DC CHARACTERISTICS V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		150	200		150	200		150	200	mA
V_{OH}	Output HIGH Voltage (Note 3)	1250	1400	1550	1250	1400	1550	1250	1400	1550	mV
V_{OL}	Output LOW Voltage (Note 3)	800	950	1100	800	950	1100	800	950	1100	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{\text{CLK}}$	–150 –150		150 150	–150 –150		150 150	–150 –150		150 150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}.
3. All loading with 100 Ω across LVDS differential outputs.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS V_{CC} = 2.375 to 2.625 V, V_{EE} = 0 V (Note 5)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{maxLVDS/LVPECL}$	Maximum Frequency (See Figure 2. F_{max}/JITTER)		> 1			> 1			> 1		GHz
t_{PLH} t_{PHL}	Propagation Delay	425	525	625	450	550	650	475	575	675	ps
t_{skew}	Within–Device Skew (Note 6) Device–to–Device Skew (Note 7) Duty Cycle Skew (Note 8)		20 85 80	25 160 100		20 85 80	25 160 100		20 85 80	35 160 100	ps
t_{JITTER}	RMS Random Clock Jitter		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	50	130	200	75	150	225	80	160	230	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Measured with 400 mV source, 50% duty cycle clock source. All loading with 100 Ω across differential outputs.
6. Skew is measured between outputs under identical transitions of similar paths through a device.
7. Device–to–Device skew for identical transitions at identical V_{CC} levels.
8. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.

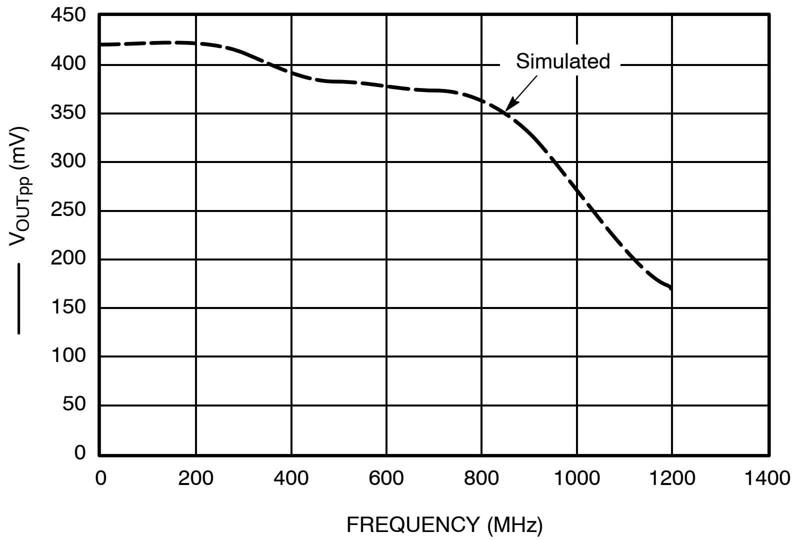


Figure 2. F_{max}

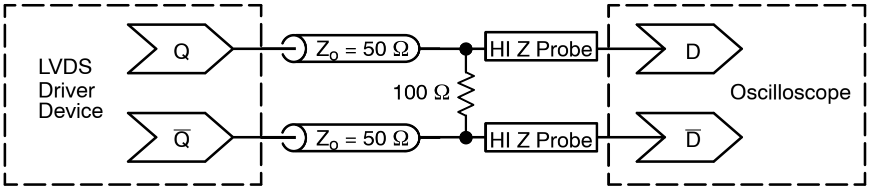


Figure 3. Typical Termination for Output Driver and Device Evaluation

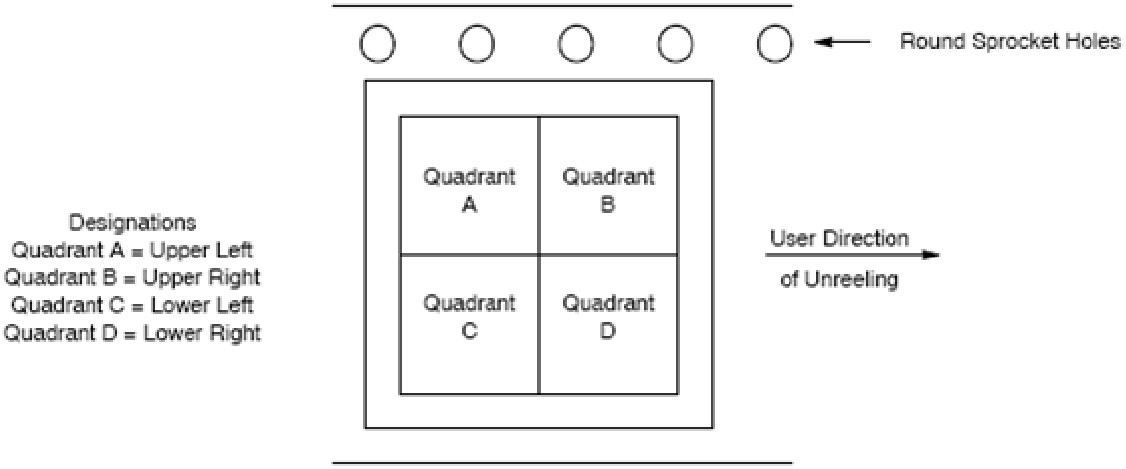


Figure 4. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP210SFAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC100EP210SFAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 4)
MC100EP210SMNG	QFN−32 (Pb−Free)	72 Units / Tray
MC100EP210SMNR4G	QFN−32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

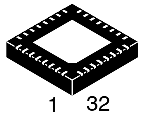
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P

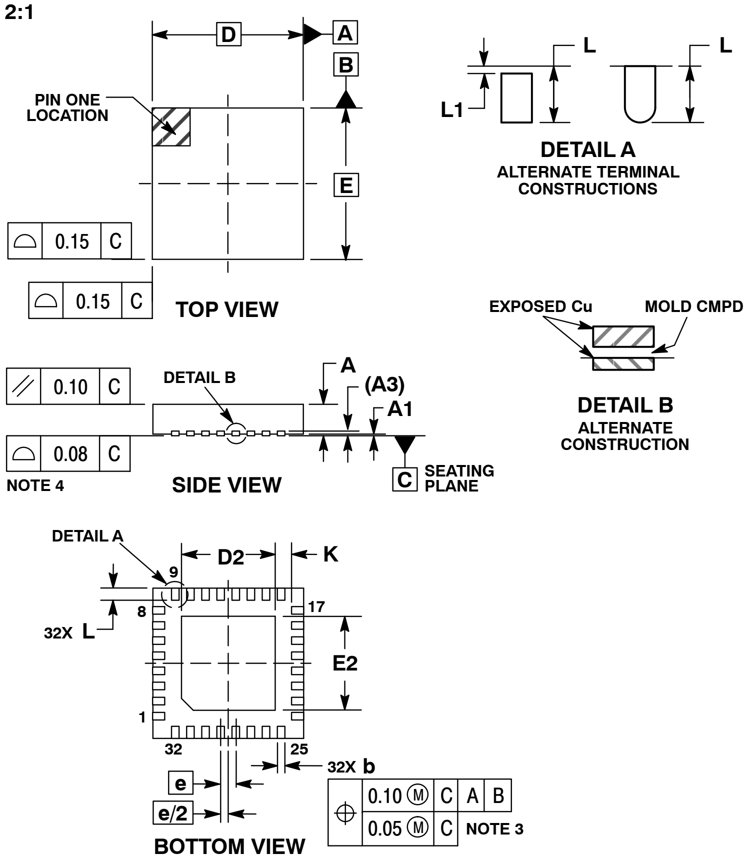
CASE 488AM

ISSUE A

DATE 23 OCT 2013



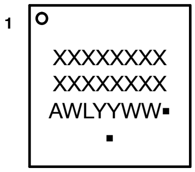
SCALE 2:1



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

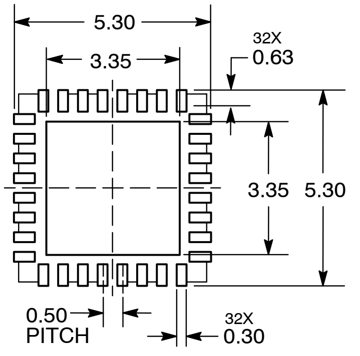


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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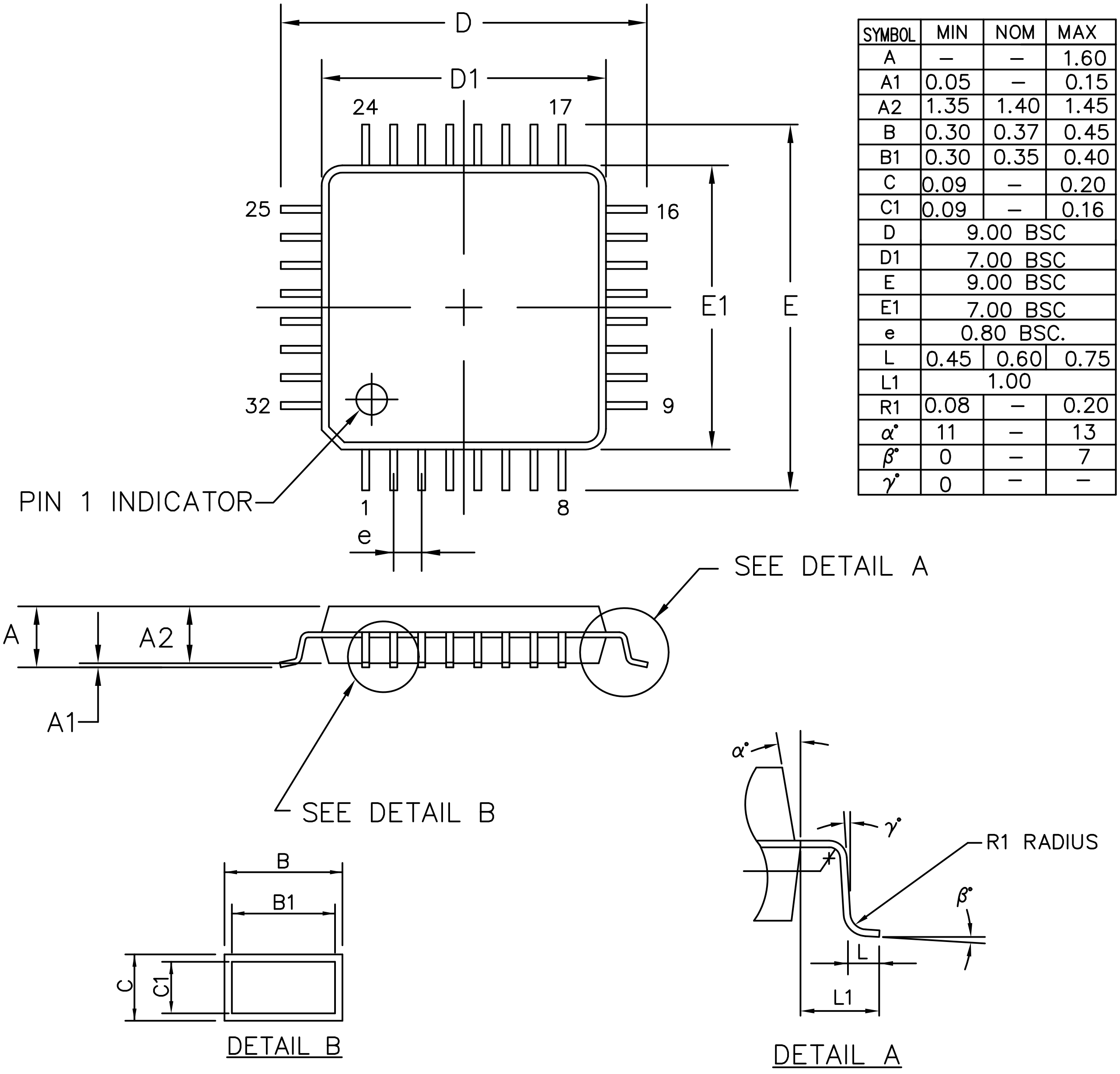
DESCRIPTION:	**QFN32 5x5 0.5P**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 2008



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–

ALL DIMENSIONS IN MM

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DESCRIPTION:	**32 LEAD LQFP, 7X7**	**PAGE 1 OF 1**

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