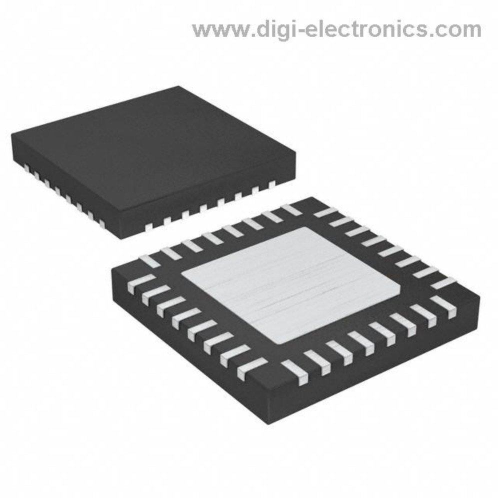
MC100EP809MNG Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MC100EP809MNG-DG
Manufacturer	onsemi
Manufacturer Product Number	MC100EP809MNG
Description	IC CLK BUFFER 1:9 750MHZ 32QFN
Detailed Description	Clock Fanout Buffer (Distribution), Multiplexer IC 1:9 750 MHz 32-VFQFN Exposed Pad

Purchase and inquiry

Manufacturer Product Number:	MC100EP809MNG	Manufacturer:	onsemi
Series:	100EP	Product Status:	Active
Type:	Fanout Buffer (Distribution), Multiplexer	Number of Circuits:	2
Ratio - Input:Output:	1:9	Differential - Input:Output:	Yes/Yes
Input:	HSTL, LVDS, LVPECL	Output:	HSTL
Frequency - Max:	750 MHz	Voltage - Supply:	3V ~ 3.6V
Operating Temperature:	0°C ~ 85°C	Mounting Type:	Surface Mount
Package / Case:	32-VFQFN Exposed Pad	Supplier Device Package:	32-QFN (5x5)
Base Product Number:	MC100EP809		

Environmental & Export classification

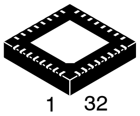
RoHS Status:	ROHS3 Compliant	Moisture Sensitivity Level (MSL):	1 (Unlimited)
REACH Status:	REACH Unaffected	ECCN:	EAR99
HTSUS:	8542.39.0001		

onsemi

DATA SHEET
www.onsemi.com

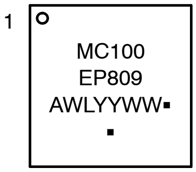
3.3 V 2:1:9 Differential HSTL/PECL/LVDS to HSTL Clock Driver with LVTTL Clock Select and Enable

MC100EP809



QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC100EP809MNG	QFN32 (Pb−Free)	74 Units / Rail

Description

The MC100EP809 is a low skew 2:1:9 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are one differential HSTL and one differential LVPECL. Both input pairs can accept LVDS levels. They are selected by the CLK_SEL pin which is LVTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (Figure 8).

The MC100EP809 guarantees low output−to−output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. The MC100EP809 output structure uses open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (Figure 6). To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

Designers can take advantage of the EP809's performance to distribute low skew clocks across the backplane of the board. Both clock inputs may be single−end driven by biasing the non−driven pin in an input pair (Figure 7).

Features

- 100 ps Typical Device−to−Device Skew
- 15 ps Typical within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to GND with no Offset Voltage
- Maximum Frequency > 750 MHz
- 850 ps Typical Propagation Delay
- Fully Compatible with Micrel SY89809L
- PECL and HSTL Mode Operating Range: V_{CCI} = 3 V to 3.6 V with GND = 0 V, V_{CCO} = 1.6 V to 2.0 V
- Open Input Default State
- This Device is Pb−Free and is RoHS Compliant

June, 2024 − Rev. 12

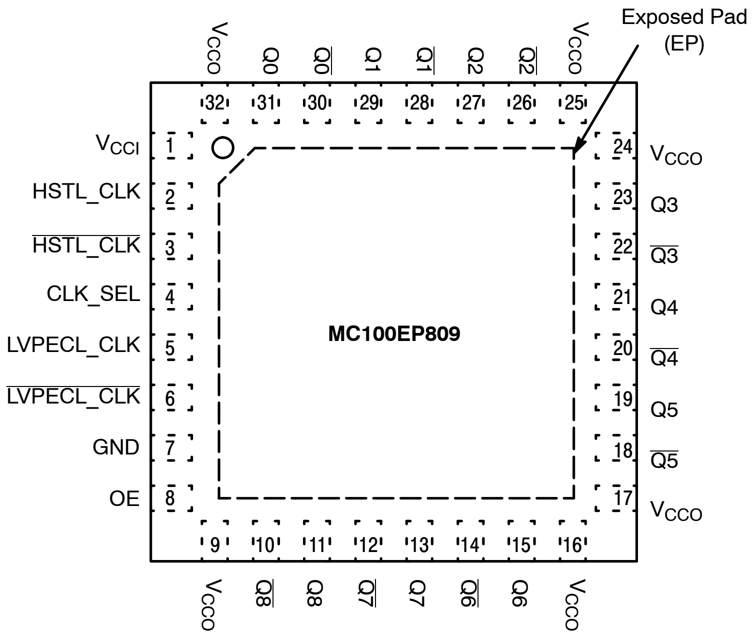


Figure 1. 32−Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
HSTL_CLK*, $\overline{\text{HSTL\_CLK}}$**	HSTL or LVDS Differential Inputs
LVPECL_CLK*, $\overline{\text{LVPECL\_CLK}}$**	LVPECL or LVDS Differential Inputs
CLK_SEL**	LVCMOS/LVTTL Input CLK Select
OE**	LVCMOS/LVTTL Output Enable
Q0 – Q8, $\overline{\text{Q0}}$ – $\overline{\text{Q8}}$	HSTL Differential Outputs
V_{CC1}	Positive Supply_Core (3.0 V – 3.6 V)
V_{CC0}	Positive Supply_HSTL Outputs (1.6 V – 2.0 V)
GND	Ground
EP	The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of the package. THe exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND.

* Pins will default LOW when left open.
** Pins will default HIGH when left open.

Table 2. TRUTH TABLE

OE*	CLK_SEL	Q0 – Q8	$\overline{\text{Q0}}$ – $\overline{\text{Q8}}$
L	L	L	H
L	H	L	H
H	L	HSTL_CLK	$\overline{\text{HSTL\_CLK}}$
H	H	LVPECL_CLK	$\overline{\text{LVPECL\_CLK}}$

*The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVOCL_CLK signals.

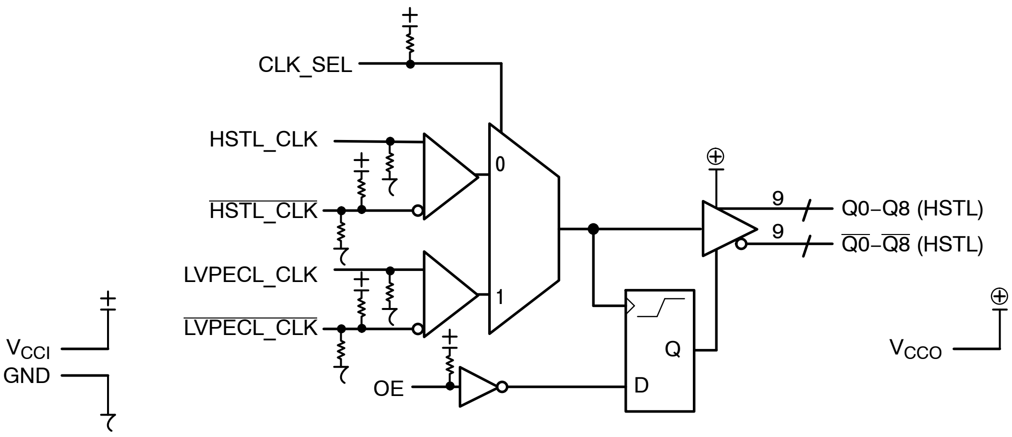


Figure 2. Logic Diagram

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	37.5 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
QFN−32	Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	478 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC1}	Core Power Supply	GND = 0 V	V_{CC0} = 1.6 to 2.0 V	4	V
V_{CC0}	HSTL Output Power Supply	GND = 0 V	V_{CC1} = 3.0 to 3.6 V	4	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC1}$	4	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm		31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P		12	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. LVPECL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Core Power Supply Current	75	95	115	75	95	115	75	95	115	mA
V_{IH}	Input HIGH Voltage (Single–Ended)	V_{CCI} – 1.165		V_{CCI} – 0.88	V_{CCI} – 1.165		V_{CCI} – 0.88	V_{CCI} – 1.165		V_{CCI} – 0.88	V
V_{IL}	Input LOW Voltage (Single–Ended)	V_{CCI} – 1.945		V_{CCI} – 1.6	V_{CCI} – 1.945		V_{CCI} – 1.6	V_{CCI} – 1.945		V_{CCI} – 1.6	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) (Figure 4) LVPECL_CLK/$\overline{\text{LVPECL\_CLK}}$	1.2		V_{CCI}	1.2		V_{CCI}	1.2		V_{CCI}	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	µA
I_{IL}	Input LOW Current	–150		150	–150		150	–150		150	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. LVTTL/LVCMOS DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	µA
I_{IL}	Input LOW Current	–300		300	–300		300	–300		300	µA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 7. HSTL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 3)	1.0		1.2	1.0		1.2	1.0		1.2	V
V_{OL}	Output LOW Voltage (Note 3)	0.1		0.4	0.1		0.4	0.1		0.4	V
V_{IH}	Input HIGH Voltage (Figure 5)	V_X + 0.1		1.6	V_X + 0.1		1.6	V_X + 0.1		1.6	V
V_{IL}	Input LOW Voltage (Figure 5)	–0.3		V_X – 0.1	–0.3		V_X – 0.1	–0.3		V_X – 0.1	V
V_X	HSTL Input Crossover Voltage	0.68	–	0.9	0.68	–	0.9	0.68	–	0.9	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	µA
I_{IL}	Input LOW Current	–300		300	–300		300	–300		300	µA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) HSTL_CLK/$\overline{\text{HSTL\_CLK}}$	0.6		V_{CCI} – 1.2	0.6		V_{CCI} – 1.2	0.6		V_{CCI} – 1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. All outputs loaded with 50 Ω to GND (Figure 6).
4. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V (Note 5)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{Opp}	Differential Output Voltage (Figure 3)										
	f_{out} < 100 MHz	600	850		600	850		600	850		mV
	f_{out} < 500 MHz	600	750		600	750		600	750		mV
	f_{out} < 750 MHz	450	575		450	575		450	575		mV
t_{PLH} t_{PHL}	Propagation Delay (Differential Configuration)										
	LVPECL_CLK to Q	680	800	930	700	820	950	780	920	1070	ps
	HSTL_CLK to Q	690	830	990	700	850	1000	790	950	1110	ps
t_{skew}	Within−Device Skew (Note 6)		15	50		15	50		15	50	ps
	Device−to−Device Skew (Note 7)		100	200		100	200		100	200	ps
t_{JITTER}	Random Clock Jitter (Figure 3) (RMS)		1.4	3.0		1.4	3.0		1.4	3.0	ps
V_{PP}	Input Swing (Differential Configuration) (Note 8) (Figure 4)										
	LVPECL	200			200			200			mV
	HSTL	200			200			200			mV
t_S	OE Set Up Time (Note 9)	0.5			0.5			0.5			ns
t_H	OE Hold Time	0.5			0.5			0.5			ns
t_r/t_f	Output Rise/Fall Time (20% − 80%)	350		600	350	450	600	350		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to GND (Figure 6).
6. Skew is measured between outputs under identical transitions and conditions on any one device.
7. Device−to−Device skew for identical transitions and conditions.
8. V_{PP} is the Differential Input Voltage swing required to maintain AC characteristics listed herein.
9. OE Set Up Time is defined with respect to the rising edge of the clock. OE High−to−Low transition ensures outputs remain disabled during the next clock cycle. OE Low−to−High transition enables normal operation of the next input clock (Figure 8).

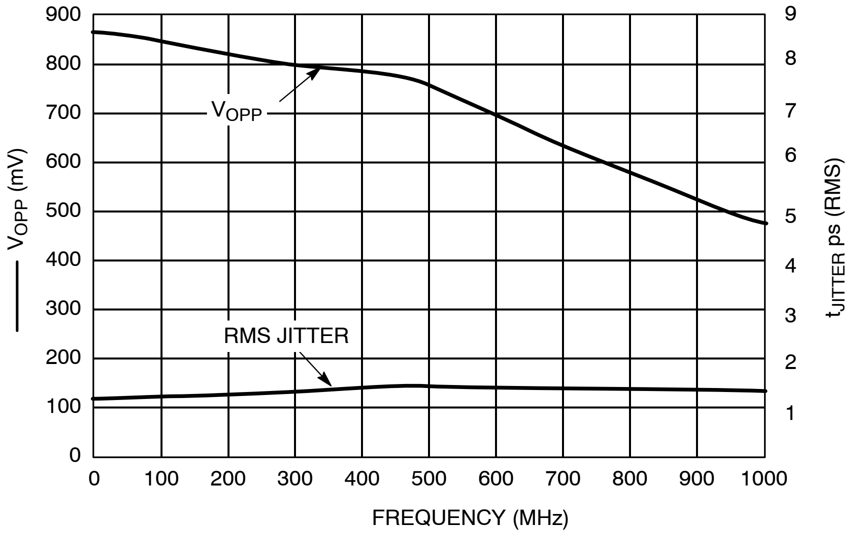


Figure 3. Output Frequency (F_{OUT}) versus Output Voltage (V_{OPP}) and Random Clock Jitter (t_{JITTER})

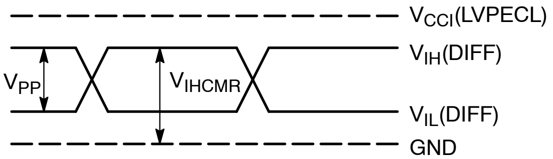


Figure 4. LVPECL Differential Input Levels

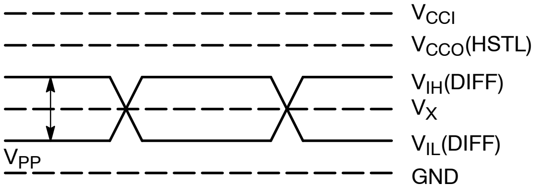


Figure 5. HSTL Differential Input Levels

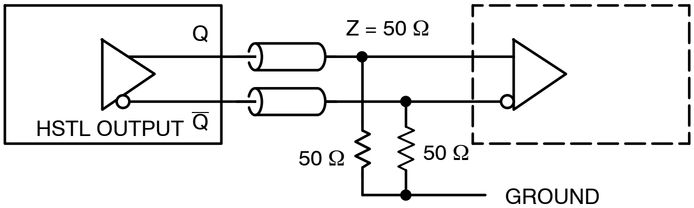
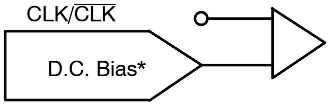


Figure 6. HSTL Output Termination and AC Test Reference



*Must be CLK/$\overline{CLK}$ common mode voltage: ((V_{IH} + V_{IL})/2).

Figure 7. Single−Ended CLK/$\overline{CLK}$ Input Configuration

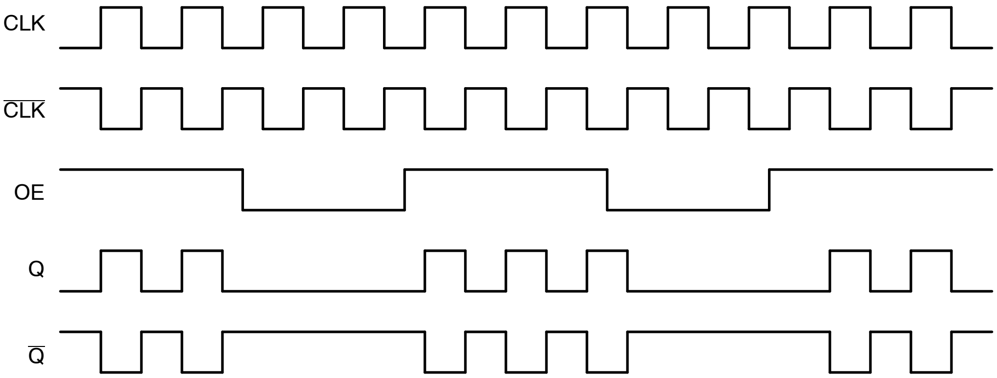


Figure 8. Output Enable (OE) Timing Diagram

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

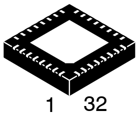
AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

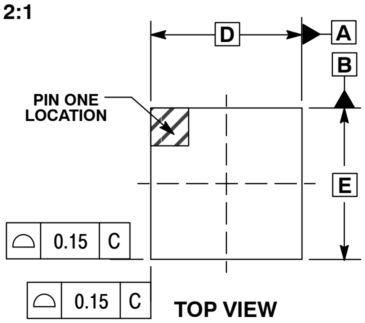
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



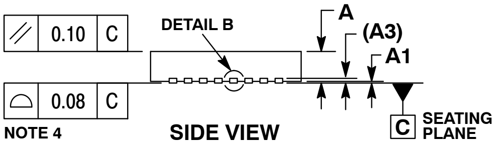
SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

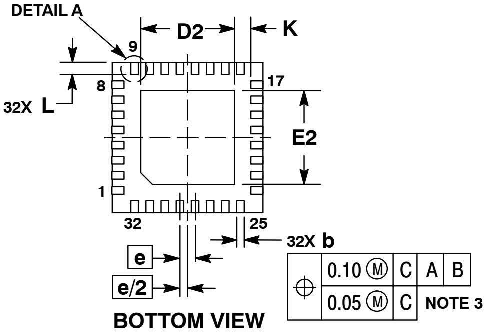
DATE 23 OCT 2013



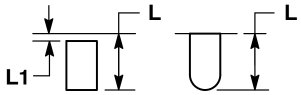
TOP VIEW



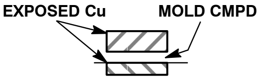
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

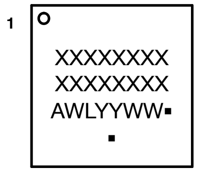


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

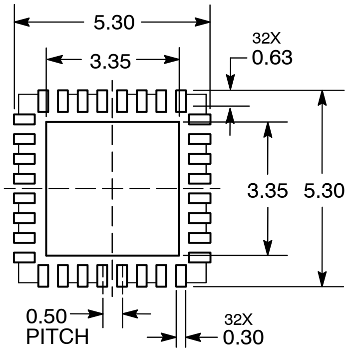


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON20032D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN32 5x5 0.5P**	**PAGE 1 OF 1**

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we striciy control the quality of products and services. Welcome your RFQ to Email: Info@DiGi-Electronics.com

DCI.

QUALITY MANAGEMENT SYSTEM CERTIFICATE

DIGI ELECTRONICS HK LIMITED

GB/T 19001-2016 idt ISO9001:2015

DCI Certification Ltd

DCI.

ENVIRONMENTAL MANAGEMENT SYSTEM CERTIFICATE

DIGI ELECTRONICS HK LIMITED

GB/T 24001-2016 idt ISO14001:2015

DCI Certification Ltd

DCI.

OCCUPATIONAL HEALTH & SAFETY MANAGEMENT SYSTEM CERTIFICATE

DIGI ELECTRONICS HK LIMITED

GB/T45001-2020 idt ISO45001:2018

DCI Certification Ltd

CR

CERTIFICATE OF INCORPORATION

ASA

MEMBERSHIP

Certificate

DIGI ELECTRONICS HK LIMITED

dun&bradstreet

A Dun & Bradstreet

D-U-N-S® Registered™ Business