# MC100LVEL34DTG Datasheet
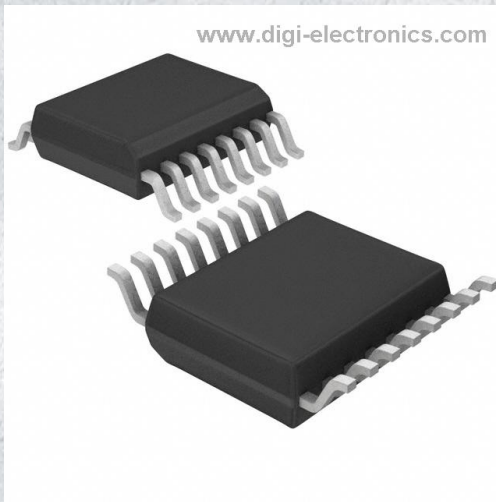
www.digi-electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | MC100LVEL34DTG-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | MC100LVEL34DTG |
| Description | IC CLOCK GENERATOR 16TSSOP |
| Detailed Description | Clock Generator IC 1.5GHz 1 16-TSSOP (0.173", 4.40 mm Width) |

https://www.DiGi-Electronics.com

# Purchase and inquiry

| | |
|---|---|
| Manufacturer Product Number: | Manufacturer: |
| MC100LVEL34DTG | onsemi |
| Series: | Product Status: |
| 100LVEL | Obsolete |
| DiGi-Electronics Programmable: | Type: |
| Not Verified | Clock Generator |
| PLL: | Input: |
| No | LVDS, NECL, PECL |
| Output: | Number of Circuits: |
| ECL | 1 |
| Ratio - Input:Output: | Differential - Input:Output: |
| 1:4 | Yes/Yes |
| Frequency - Max: | Divider/Multiplier: |
| 1.5GHz | Yes/No |
| Voltage - Supply: | Operating Temperature: |
| 3V ~ 3.8V | -40°C ~ 85°C |
| Mounting Type: | Package / Case: |
| Surface Mount | 16-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package: | Base Product Number: |
| 16-TSSOP | MC100 |

# Environmental & Export classification

| | |
|---|---|
| RoHS Status: | Moisture Sensitivity Level (MSL): |
| ROHS3 Compliant | 1  (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

**onsemi**

# 3.3 V ECL ÷2, ÷4, ÷8 Clock Generation Chip
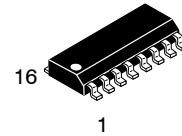# MC100LVEL34

## Description

The MC100LVEL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 µF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start−up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple LVEL34s in a system.

## Features

- 50 ps Typical Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 1.5 GHz Toggle Frequency
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range:
  $V_{CC}$ = 3.0 V to 3.8 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −3.8 V
- Open Input Default State
- LVDS Input Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

**SOIC−16**
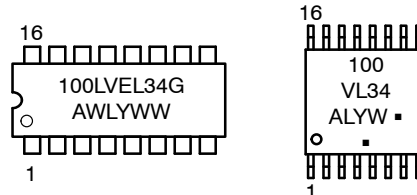**D SUFFIX**
**CASE 751B**

16

1
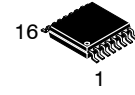
**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

16

1

## MARKING DIAGRAM

16

100LVEL34G
AWLYWW

1

16

100
VL34
ALYW ▪

1

A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100LVEL34DR2G | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |
| MC100LVEL34DTR2G | TSSOP−16 (Pb−Free) | 2500 / Tape & Reel |

**DISCONNTINUED** (Note 1)

| | | |
|---|---|---|
| MC100LVEL34DTG | TSSOP−16 (Pb−Free) | 96 / Units & Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

# MC100LVEL34
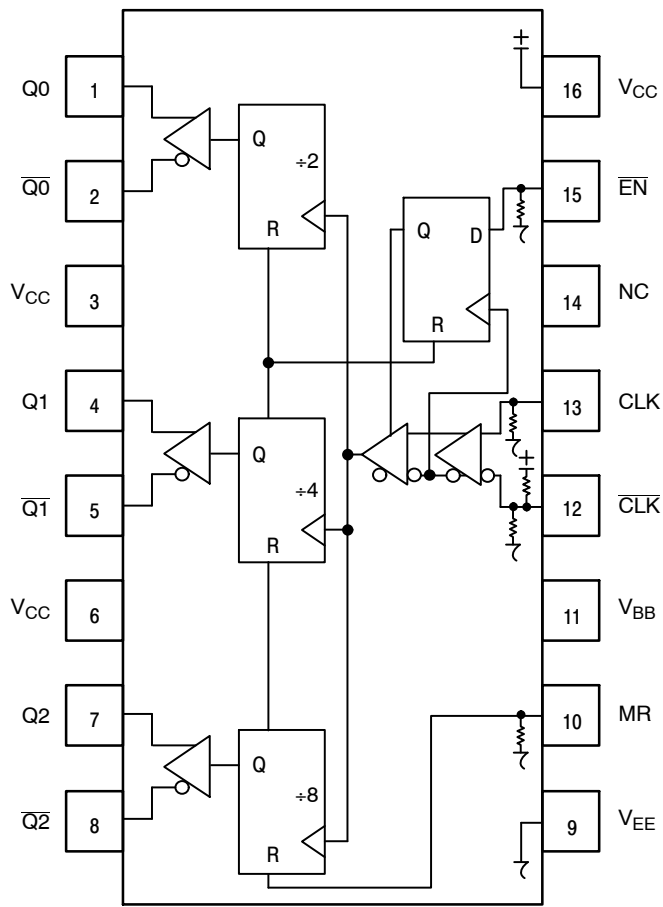


**Warning:** All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 16−Lead Pinout** (Top View) **and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| CLK*, $\overline{CLK}$** | ECL Diff Clock Inputs |
| $\overline{EN}$* | ECL Sync Enable |
| MR* | ECL Master Reset |
| Q0, $\overline{Q0}$ | ECL Diff ÷2 Outputs |
| Q1, $\overline{Q1}$ | ECL Diff ÷4 Outputs |
| Q2, $\overline{Q2}$ | ECL Diff ÷8 Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

\* Pins will default LOW when left open.

\*\*\*Pins will default to $V_{CC}/2$ when left open.

**Table 2. FUNCTION TABLE**

| CLK | $\overline{EN}$ | MR | FUNCTION |
|---|---|---|---|
| Z | L | L | Divide |
| ZZ | H | L | Hold $Q_{0-3}$ |
| X | X | H | Reset $Q_{0-3}$ |

Z = Low-to-High Transition
ZZ = High-to-Low Transition

**Table 3. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | 37.5 kΩ |
| ESD Protection<br>    Human Body Model<br>    Machine Model<br>    Charged Device Model | > 2 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb−Free Pkg |
|     SOIC−16<br>    TSSOP−16 | Level 1<br>Level 1 |
| Flammability Rating<br>    Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | 210 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

# MC100LVEL34

### Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|--------|-----------|-------------|-------------|--------|------|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE} = 0$ V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC} = 0$ V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0$ V<br>$V_{CC} = 0$ V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ±0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | SOIC−16<br>SOIC−16 | 100<br>60 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | SOIC−16 | 33 to 36 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | TSSOP−16<br>TSSOP−16 | 138<br>108 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | TSSOP−16 | 33 to 36 | °C/W |
| $T_{sol}$ | Wave Solder | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### Table 5. 100LVEL DC CHARACTERISTICS, PECL ($V_{CC} = 3.3$ V, $V_{EE} = 0$ V (Note 2))

| Symbol | Characteristic | −40°C Min | −40°C Typ | −40°C Max | 25°C Min | 25°C Typ | 25°C Max | 85°C Min | 85°C Typ | 85°C Max | Unit |
|--------|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| $I_{EE}$ | Power Supply Current | 40 | 50 | 60 | 40 | 50 | 60 | 42 | 52 | 62 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 1305 | 1570 | 1725 | 1305 | 1570 | 1725 | 1305 | 1570 | 1725 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1305 | | 1675 | 1305 | | 1675 | 1305 | | 1675 | mV |
| $V_{BB}$ | Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.5 V.
3. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

# MC100LVEL34

**Table 6. 100LVEL DC CHARACTERISTICS, NECL** ($V_{CC}$ = 0 V, $V_{EE}$ = –3.8 V to –3.0 V (Note 5))

| Symbol | Characteristic | –40°C Min | Typ | Max | 25°C Min | Typ | Max | 85°C Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{EE}$ | Power Supply Current | 23 | 30 | 40 | 23 | 30 | 40 | 23 | 30 | 40 | mA |
| $I_{EE}$ | Power Supply Current | 40 | 50 | 60 | 40 | 50 | 60 | 42 | 52 | 62 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | –1145 | –1020 | –895 | –1145 | –1020 | –895 | –1145 | –1020 | –895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | –1995 | –1700 | –1575 | –1995 | –1700 | –1575 | –1995 | –1700 | –1575 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single–Ended) | –1225 | | –880 | –1225 | | –880 | –1225 | | –880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single–Ended) | –1995 | | –1625 | –1995 | | –1625 | –1995 | | –1625 | mV |
| $V_{BB}$ | Output Voltage Reference | –1525 | –1425 | –1325 | –1525 | –1425 | –1325 | –1525 | –1425 | –1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | $V_{EE}$ + 1.2 | | 0.0 | $V_{EE}$ + 1.2 | | 0.0 | $V_{EE}$ + 1.2 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current  D  $\overline{D}$ | 0.5 –150 | | | 0.5 –150 | | | 0.5 –150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
5. Input and output parameters vary 1:1 with $V_{CC}$.
6. All loading with 50 Ω to $V_{CC}$ – 2.0 V.
7. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 7. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = –3.0 V to –5.5 V  or  $V_{CC}$ = 3.0 V to 5.5 V; $V_{EE}$ = 0 V (Note 8)

| Symbol | Characteristic | –40°C Min | Typ | Max | 25°C Min | Typ | Max | 85°C Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Toggle Frequency (Figure 4) | 1.5 | | | 1.5 | | | 1.5 | | | GHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay to Output  CLK to Q0, Q1, Q2  MR to Q | 550 500 | 650 600 | 1000 1000 | 600 550 | 700 650 | 1000 1000 | 650 600 | 750 700 | 1000 1000 | ps |
| $t_{JITTER}$ | Cycle–to–Cycle Jitter (Figure 4) | | < 1 | | | < 1 | | | < 1 | | ps |
| $t_S$ | Setup Time $\overline{EN}$ | 150 | 50 | | 150 | 50 | | 150 | 50 | | ps |
| $t_H$ | Hold Time $\overline{EN}$ | 200 | 100 | | 200 | 100 | | 200 | 100 | | ps |
| $t_{RR}$ | Set/Reset Recovery | 300 | 200 | | 300 | 200 | | 300 | 200 | | ps |
| $V_{PP}$ | Input Swing (Note 9) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times Q (20% – 80%) | 120 | 170 | 400 | 140 | 180 | 400 | 160 | 200 | 400 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to VCC – 2.0 V.
9. VPP(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC100LVEL34

There are two distinct functional relationships between the Master Reset and Clock:

Internal Clock Disabled   Internal Clock Enabled

MR

CLK

Q0

Q1

Q2

$\overline{EN}$
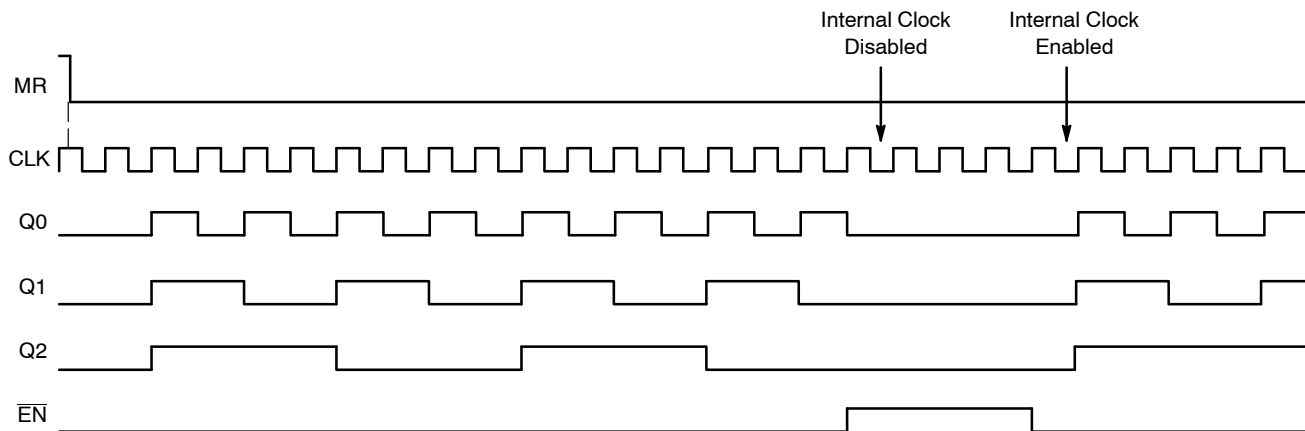
**CASE 1: If the MR is Deasserted (H−L), while the Clock is Still High,
the Outputs will Follow the Second Ensuing Clock Rising Edge**

Internal Clock Disabled   Internal Clock Enabled

MR

CLK

Q0

Q1

Q2

$\overline{EN}$
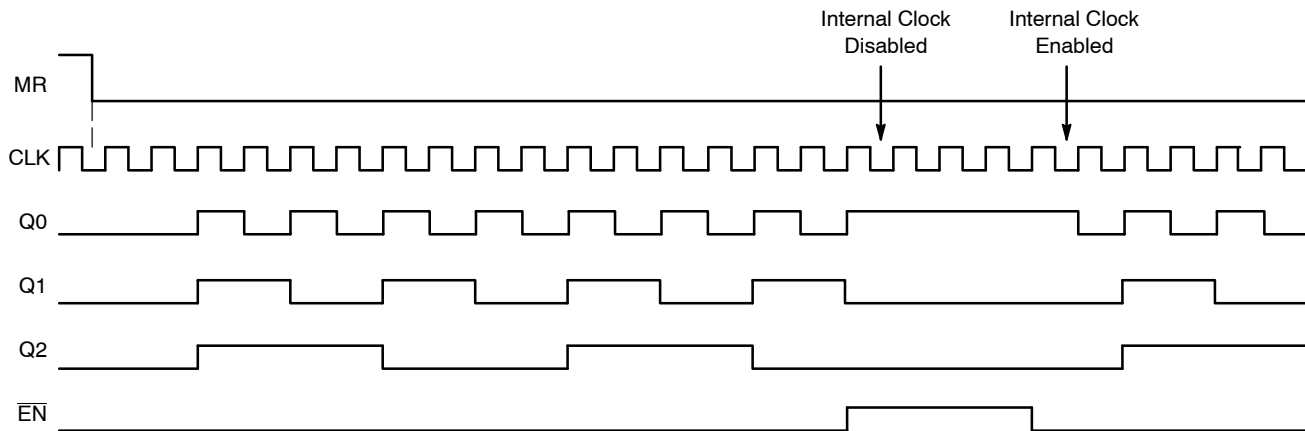
**CASE 2: If the MR is Deasserted (H−L), after the Clock has Transitioned Low,
the Outputs will Follow the Third Ensuing Clock Rising Edge**

**Figure 2. Timing Diagrams**

The $\overline{EN}$ signal will "freeze" the internal divider flip−flops on the first falling edge of CLK after its assertion. The internal divider flip−flops will maintain their state during the freeze. When $\overline{EN}$ is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip−flops will "unfreeze" and continue to their next state count with proper phase relationships.

$T_{RR}$

CLOCK

MR

OUTPUT

**CASE 1**

$T_{RR}$

CLOCK

MR

OUTPUT

**CASE 2**
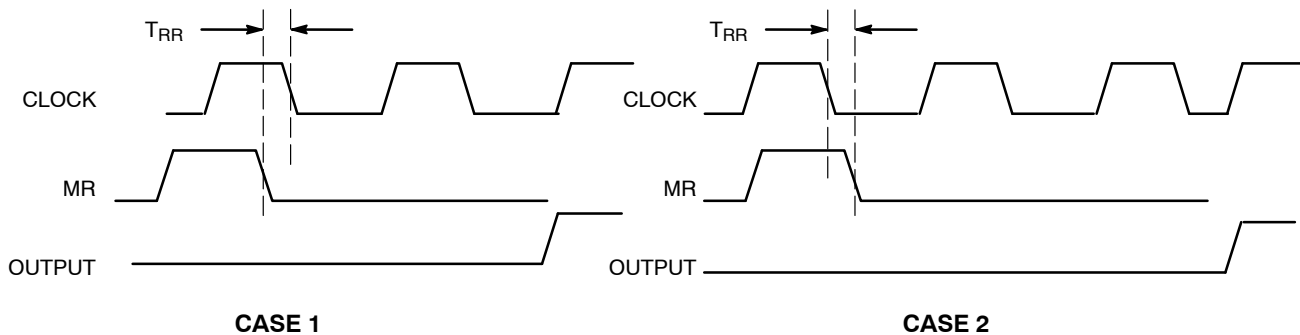
**Figure 3. Reset Recovery Time**

# MC100LVEL34
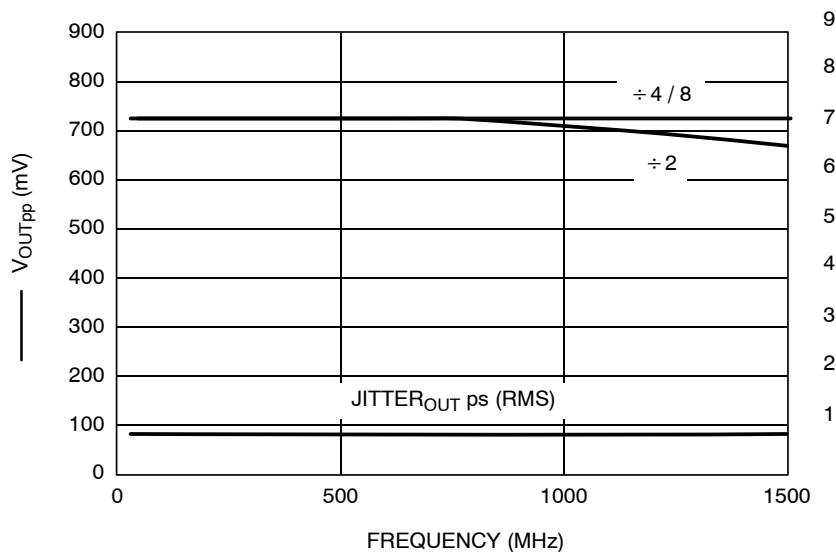


**Figure 4. $F_{max}$/Jitter**



$V_{TT}$
$V_{TT} = V_{CC} - 2.0\ V$
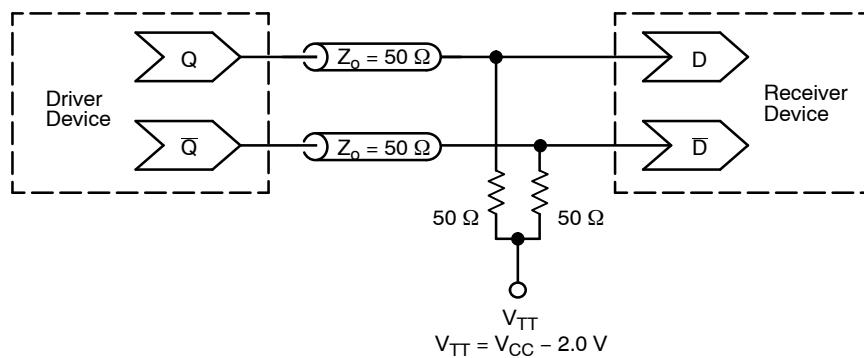
**Figure 5. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

**Resource Reference of Application Notes**

**AN1405/D**   –   ECL Clock Distribution Techniques

**AN1406/D**   –   Designing with PECL (ECL at +5.0 V)

**AN1503/D**   –   ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D**   –   Metastability and the ECLinPS Family

**AN1568/D**   –   Interfacing Between LVDS and ECL

**AN1672/D**   –   The ECL Translator Guide

**AND8001/D**  –   Odd Number Counters Design

**AND8002/D**  –   Marking and Date Codes

**AND8020/D**  –   Termination of ECL Logic Devices

**AND8066/D**  –   Interfacing with ECLinPS

**AND8090/D**  –   AC Characteristics of ECL Devices

**MECHANICAL CASE OUTLINE**
**PACKAGE DIMENSIONS**
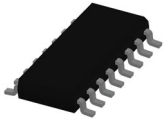
**SOIC−16 9.90x3.90x1.37 1.27P**
**CASE 751B**
**ISSUE M**

**DATE 18 OCT 2024**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
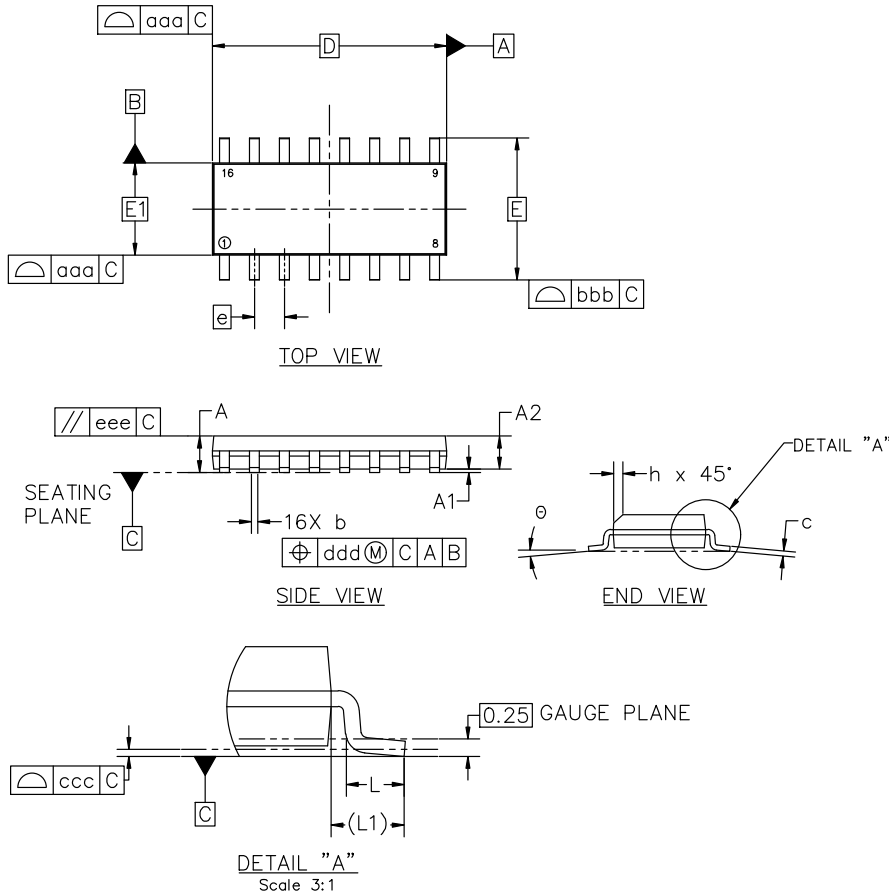
| DIM | MILLIMETERS | | |
|-----|------|------|------|
|     | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | 1.25 | 1.37 | 1.50 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | ––– | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| Θ | 0° | ––– | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE

DETAIL "A"

8X
6.40

1.270
PITCH

16X
0.58

1.120
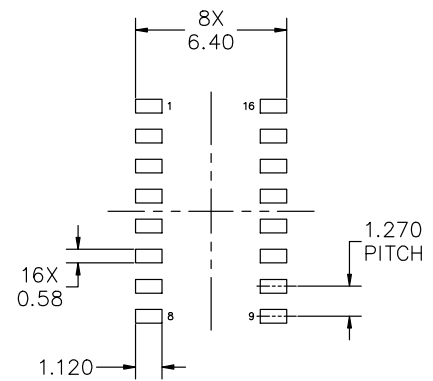
RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

| **DOCUMENT NUMBER:** | **98ASB42566B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.37 1.27P** | | **PAGE 1 OF 2** |

**SOIC−16 9.90x3.90x1.37 1.27P**
CASE 751B
ISSUE M

DATE 18 OCT 2024

**GENERIC**
**MARKING DIAGRAM\***

```
16 ┌─────────────────┐
   │ XXXXXXXXXXXXG  │
   │ XXXXXXXXXXXXX  │
 ○ │     AWLYWW     │
 1 └─────────────────┘
```
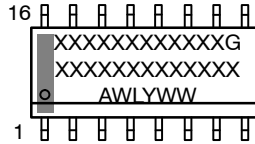
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |

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|---|---|---|---|
| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.37 1.27P** | | **PAGE 2 OF 2** |

**onsemi**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

**SCALE 2:1**

16X **K** REF

$\oplus$ | 0.10 (0.004) (M) | T U (S) V (S)

$\triangle$ | 0.15 (0.006) | T U (S)

2X **L/2**

16          9

**L**

**B**
**−U−**

PIN 1
IDENT.

1          8

$\triangle$ | 0.15 (0.006) | T U (S)

**A**
**−V−**

**C**

$\triangle$ | 0.10 (0.004)
**−T−** SEATING
PLANE

**D**          **G**          **H**

**K**
**K1**

**J1**

**J**

**SECTION N−N**

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

−W−

**DETAIL E**
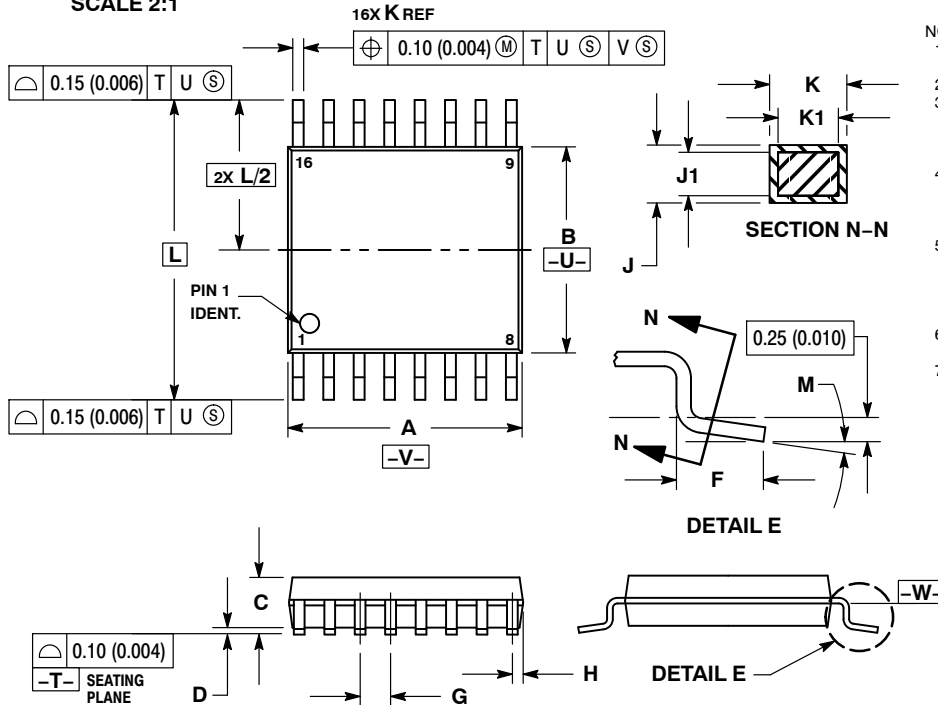
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX |
|---|---|---|---|---|
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED
## SOLDERING FOOTPRINT*

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

## GENERIC
## MARKING DIAGRAM*

16

XXXX
XXXX
ALYW

1
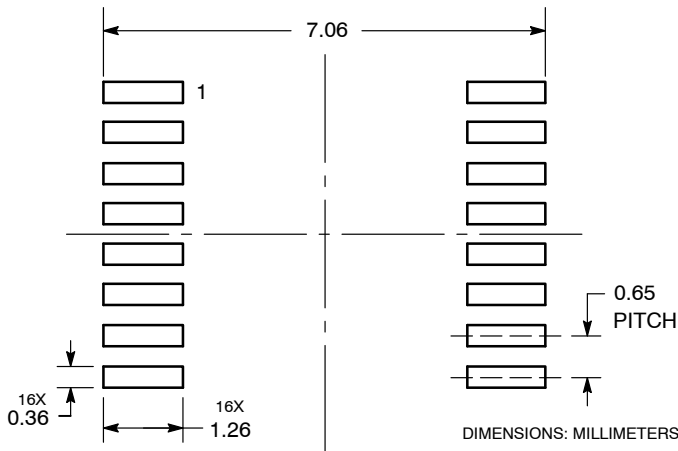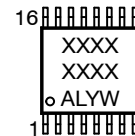
XXXX  = Specific Device Code
A     = Assembly Location
L     = Wafer Lot
Y     = Year
W     = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98ASH70247A | | |
|---|---|---|---|
| DESCRIPTION: | TSSOP−16 | | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

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