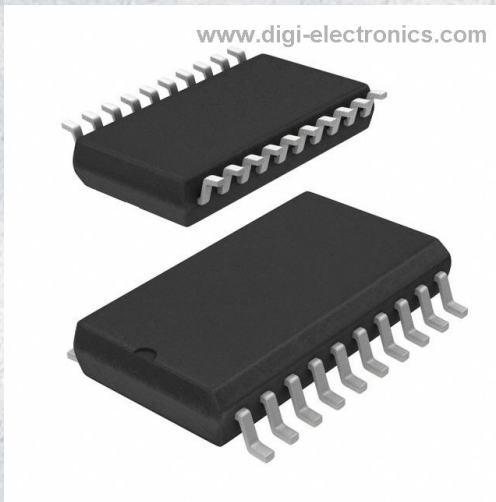


MC100LVEL39DWR2G Datasheet



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | MC100LVEL39DWR2G-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | MC100LVEL39DWR2G |
| Description | IC CLOCK GENERATOR 20SOIC |
| Detailed Description | Clock Generator IC 1GHz 1 20-SOIC (0.295", 7.50mm Width) |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

MC100LVEL39DWR2G

Series:

100LVEL

DiGi-Electronics Programmable:

Not Verified

PLL:

No

Output:

ECL

Ratio - Input:Output:

1:4

Frequency - Max:

1GHz

Voltage - Supply:

3V ~ 3.8V

Mounting Type:

Surface Mount

Supplier Device Package:

20-SOIC

Manufacturer:

onsemi

Product Status:

Active

Type:

Clock Generator

Input:

LVDS, NECL, PECL

Number of Circuits:

1

Differential - Input:Output:

Yes/Yes

Divider/Multiplier:

Yes/No

Operating Temperature:

-40°C ~ 85°C

Package / Case:

20-SOIC (0.295", 7.50mm Width)

Base Product Number:

MC100

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

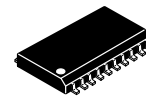
3 (168 Hours)

ECCN:

EAR99

3.3 V ECL $\div 2/4$, $\div 4/6$ Clock Generation Chip

MC100LVEL39



SOIC-20 WB
DW SUFFIX
CASE 751D

Description

The MC100LVEL39 is a low skew $\div 2/4$, $\div 4/6$ clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device.

The common enable (\overline{EN}) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

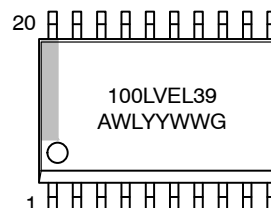
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the Master Reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the $\div 2/4$ and the $\div 4/6$ outputs of a single device.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: Human Body Model; > 2 kV
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
 $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
 $V_{CC} = 0 \text{ V with } V_{EE} = -3.0 \text{ V to } -3.8 \text{ V}$
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
 - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in,
Oxygen Index: 28 to 34

MARKING DIAGRAM*



| | |
|----|---------------------|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

*For additional marking information, refer to Application Note [AND8002/D](#).

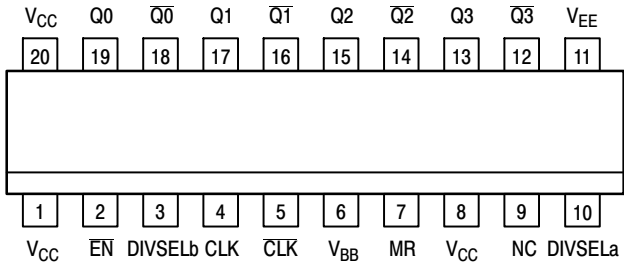
ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|-------------------------|-----------------------|
| MC100LVEL39DWR2G | SOIC-20 WB (Pb-Free) | 1000/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

- Transistor Count = 419 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MC100LEVEL39



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: SOIC-20 WB (Top View)

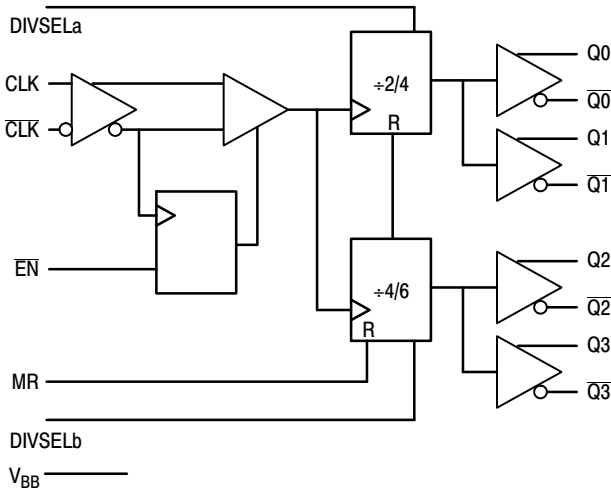


Figure 2. Logic Diagram

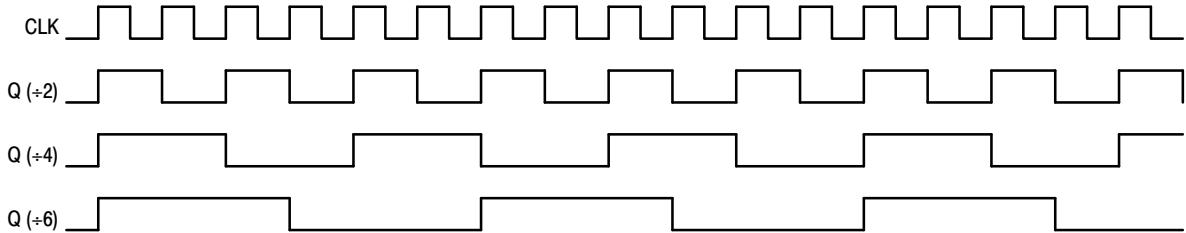


Figure 3. Timing Diagrams

Table 1. PIN DESCRIPTION

| Column Head | |
|--|-----------------------------|
| CLK, \overline{CLK} | ECL Diff Clock Inputs |
| $Q_0, Q_1; \overline{Q_0}, \overline{Q_1}$ | ECL Diff $\pm 2/4$ Outputs |
| $Q_2, Q_3; \overline{Q_2}, \overline{Q_3}$ | ECL Diff $\pm 4/6$ Outputs |
| DIVSELa, DIVSELb | ECL Frequency Select Inputs |
| EN | ECL Sync Enable |
| MR | ECL Master Reset |
| V_{BB} | Reference Voltage Output |
| V_{CC} | Positive Supply |
| V_{EE} | Negative Supply |
| NC | No Connect |

Table 2. FUNCTION TABLE

| CLK | EN | MR | Function |
|-----|----|----|------------|
| Z | L | L | Divide |
| ZZ | H | L | Hold Q0-3 |
| X | X | H | Reset Q0-3 |

Z = Low-to-High Transition
 ZZ = High-to-Low Transition
 X = Don't Care

| DIVSELa | Q_0, Q_1 Outputs |
|---------|--------------------|
| L | Divide by 2 |
| H | Divide by 4 |

| DIVSELb | Q_2, Q_3 Outputs |
|---------|--------------------|
| L | Divide by 4 |
| H | Divide by 6 |

MC100LVEL39

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------------|------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 to 0 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -8 to 0 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 to 0 -6 to 0 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA |
| I _{BB} | V _{BB} Sink/Source | | | ± 0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-20 WB | 90 60 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-20 WB | 30 to 35 | °C/W |
| T _{sol} | Wave Solder (Pb-Free) | < 2 to 3 sec @ 260°C | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------|--|------------|------|------------|------------|------|------------|------------|------|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Power Supply Current | | 50 | 59 | | 50 | 59 | | 54 | 61 | mA |
| V _{OH} | Output HIGH Voltage (Note 2) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V _{OL} | Output LOW Voltage (Note 2) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V _{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V _{IL} | Input LOW Voltage (Single-Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V _{BB} | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| V _{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 6) V _{PP} < 500 mV V _{PP} ≥ 500 mV | 1.3 1.5 | | 2.9 2.9 | 1.2 1.4 | | 2.9 2.9 | 1.2 1.4 | | 2.9 2.9 | V |
| I _{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I _{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1.0 V.

MC100LVEL39**Table 5. LVNECL DC CHARACTERISTICS** ($V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 4))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|--------------|-------|--------------|--------------|-------|--------------|--------------|-------|--------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 50 | 59 | | 50 | 59 | | 54 | 61 | mA |
| V_{OH} | Output HIGH Voltage (Note 5) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 5) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$ | -2.0 -1.8 | | -0.4 -0.4 | -2.1 -1.9 | | -0.4 -0.4 | -2.1 -1.9 | | -0.4 -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

4. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.

5. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

6. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1.0 V .

Table 6. AC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 7))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|-------------------|-----|---------------------|-------------------|-----|---------------------|-------------------|-----|---------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | 1000 | | | 1000 | | | 1000 | | | MHz |
| t_{PLH} t_{PHL} | Propagation Delayed Output CLK to Q (Diff) CLK to Q (S.E.) MR to Q | 850 850 600 | | 1150 1150 900 | 900 900 610 | | 1200 1200 910 | 950 950 630 | | 1250 1250 930 | ps |
| t_{SKEW} | Within-Device Skew (Note 8) Part-to-Part $Q_0 - Q_3$ $Q_0 - Q_3$ (Diff) | | | 50 200 | | | 50 200 | | | 50 200 | ps |
| t_{JITTER} | Random CLOCK Jitter (RMS) @ 1000 MHz | | 2.0 | 3.0 | | 2.0 | 3.0 | | 2.0 | 3.0 | ps |
| t_S | Setup Time EN to CLK DIVSEL to CLK | 250 400 | | | 250 400 | | | 250 400 | | | ps |
| t_H | Hold Time CLK to EN CLK to Div_Sel | 100 150 | | | 100 150 | | | 100 150 | | | ps |
| V_{PP} | Input Swing (Note 9) CLK | 250 | | 1000 | 250 | | 1000 | 250 | | 1000 | mV |
| t_{RR} | Reset Recovery Time | | | 100 | | | 100 | | | 100 | ps |
| t_{PW} | Minimum Pulse Width CLK MR | 500 700 | | | 500 700 | | | 500 700 | | | ps |
| t_r, t_f | Output Rise/Fall Times Q (20% – 80%) | 280 | | 550 | 280 | | 550 | 280 | | 550 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

7. V_{EE} can vary $\pm 0.3\text{ V}$. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

8. Skew is measured between outputs under identical transitions.

9. $V_{PP(min)}$ is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV .

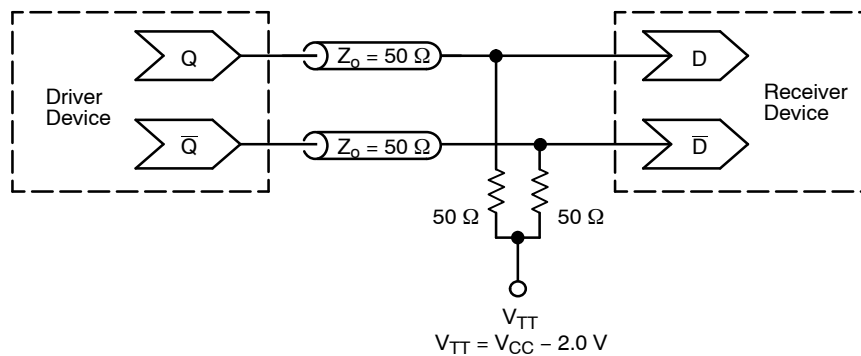
MC100LVEL39

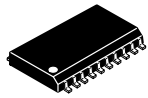
Figure 4. Typical Termination for Output Driver and Device Evaluation
 (See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

| | | |
|---------------------------|---|--------------------------------------|
| AN1405/D | - | ECL Clock Distribution Techniques |
| AN1406/D | - | Designing with PECL (ECL at +5.0 V) |
| AN1503/D | - | ECLinPS™ I/O SPiCE Modeling Kit |
| AN1504/D | - | Metastability and the ECLinPS Family |
| AN1568/D | - | Interfacing Between LVDS and ECL |
| AN1672/D | - | The ECL Translator Guide |
| AND8001/D | - | Odd Number Counters Design |
| AND8002/D | - | Marking and Date Codes |
| AND8020/D | - | Termination of ECL Logic Devices |
| AND8066/D | - | Interfacing with ECLinPS |
| AND8090/D | - | AC Characteristics of ECL Devices |



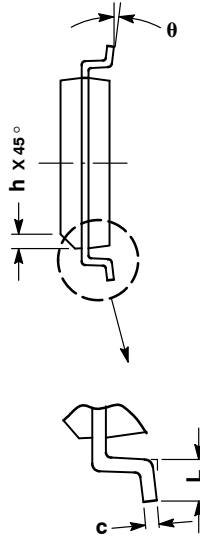
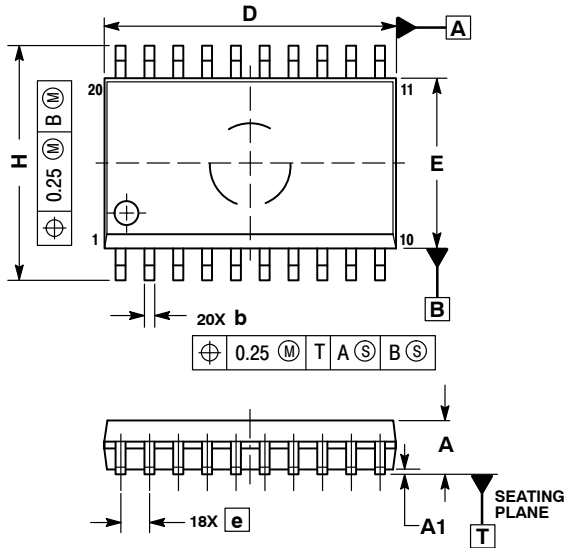
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

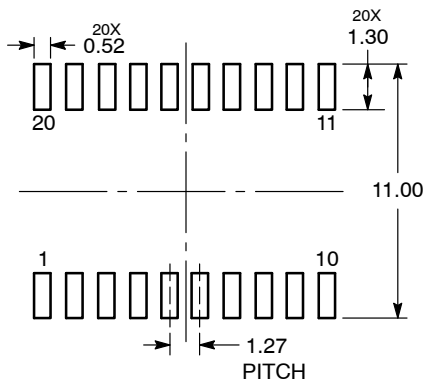


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

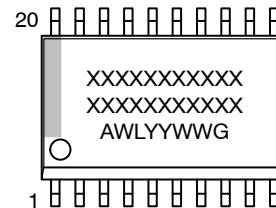
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------|---|
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| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

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