# MC100LVEL91DWR2G Datasheet


| | |
|---|---|
| DiGi Electronics Part Number | MC100LVEL91DWR2G-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | MC100LVEL91DWR2G |
| Description | IC TRANSLATOR UNIDIR 20SOIC |
| Detailed Description | Mixed Signal Translator Unidirectional 1 Circuit 3 C hannel 20-SOIC |

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| MC100LVEL91DWR2G | onsemi |
| Series: | Product Status: |
| 100LVEL | Obsolete |
| Translator Type: | Channel Type: |
| Mixed Signal | Unidirectional |
| Number of Circuits: | Channels per Circuit: |
| 1 | 3 |
| Input Signal: | Output Signal: |
| LVPECL | ECL |
| Output Type: | Data Rate: |
| Differential | - |
| Operating Temperature: | Features: |
| -40°C ~ 85°C (TA) | - |
| Mounting Type: | Package / Case: |
| Surface Mount | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package: | Base Product Number: |
| 20-SOIC | 100LVEL91 |

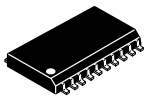
## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| ROHS3 Compliant | 3 (168 Hours) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

DATA SHEET
www.onsemi.com

# 3.3 V Triple LVPECL Input to -3.3 V to -5.0 V ECL Output Translator

# MC100LVEL91



SOIC-20 WB
DW SUFFIX
CASE 751D

## Description

The MC100LVEL91 is a triple LVPECL input to ECL output translator. The device receives low voltage differential PECL signals, determined by the $V_{CC}$ supply level, and translates them to differential –3.3 V to –5.0 V ECL output signals.

To accomplish the level translation the LVEL91 requires three power rails. The $V_{CC}$ supply should be connected to the positive supply, and the $V_{EE}$ pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both $V_{EE}$ and $V_{CC}$ should be bypassed to ground via 0.01 μF capacitors.

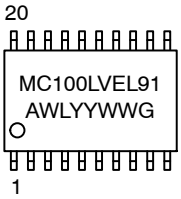
Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

## Features

- 620 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC}$ = 3.8 V to 3.0 V; $V_{EE}$ = –3.0 V to –5.5 V; GND = 0 V
- Q Output will Default LOW with Inputs Open or at GND
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

## MARKING DIAGRAM*




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100LVEL91DWG | SOIC-20 WB (Pb-Free) | 38 Units/Tube |
| **DISCONTINUED** (Note 1) | | |
| MC100LVEL91DWR2G | SOIC-20 WB (Pb-Free) | 1000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

# MC100LVEL91

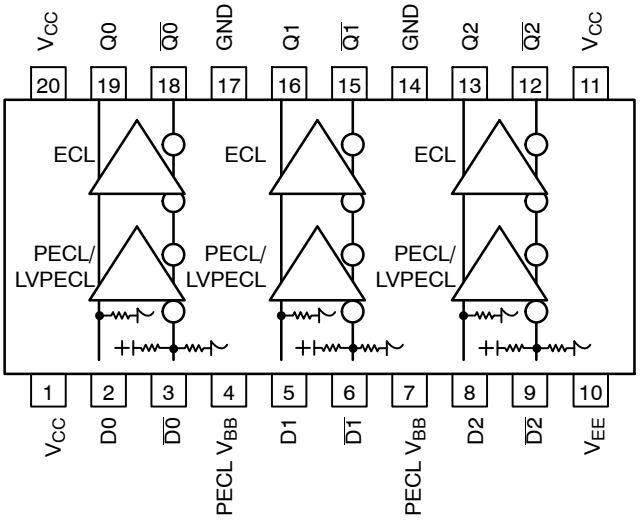



**Figure 1. SO-20 Pinout** (Top View) **and Logic Diagram**

* All $V_{CC}$ pins are tied together on the die.

Warning: All $V_{CC}$, $V_{EE}$, and GND pins must be externally connected to Power Supply to guarantee proper operation.

**Table 1. PIN DESCRIPTION**

| Pin | Function |
|---|---|
| Dn, $\overline{Dn}$ | PECL/LVPECL Inputs |
| Qn, $\overline{Qn}$ | ECL Outputs |
| PECL $V_{BB}$ | PECL Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| GND | Ground |

**Table 2. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | 75 kΩ |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 2 kV<br>> 100 V<br>> 2 kV |
| Moisture Sensitivity, (Note 2):<br>Pb-Free | Level 3 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 282 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

2. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Power Supply | GND = 0 V | | 3.8 | V |
| $V_{EE}$ | NECL Power Supply | GND = 0 V | | −6.0 | V |
| $V_I$ | PECL Input Voltage | GND = 0 V | $V_I \le V_{CC}$ | 3.8 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $I_{BB}$ | PECL $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC−20 WB | 90<br>60 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−20 WB | 30 to 35 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. LVPECL INPUT DC CHARACTERISTICS** ($V_{CC}$ = 3.3 V; $V_{EE}$ = −3.3 V to −5.0 V; GND = 0 V (Note 3))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{CC}$ | $V_{CC}$ Power Supply Current | | | 11 | | 6 | 11 | | | 11 | mA |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| LVPECL $V_{BB}$ | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)<br>$V_{PP}$ < 500 mV<br>$V_{PP}$ ≥ 500 mV | <br>1.0<br>1.2 | | <br>2.9<br>2.9 | <br>0.9<br>1.1 | | <br>2.9<br>2.9 | <br>0.9<br>1.1 | | <br>2.9<br>2.9 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | <br>0.5<br>−600 | | | <br>0.5<br>−600 | | | <br>0.5<br>−600 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Input parameters vary 1:1 with $V_{CC}$. $V_{CC}$ can vary +0.5 / −0.3 V.
4. $V_{IHCMR}$ min varies 1:1 with GND. $V_{IHCMR}$ max varies 1:1 with $V_{CC}$.

**Table 5. NECL OUTPUT DC CHARACTERISTICS** ($V_{CC}$ = 3.3 V; $V_{EE}$ = −3.3 V to −5.0 V; GND = 0 V (Note 5))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{EE}$ | $V_{EE}$ Power Supply Current | | | 27 | | 21 | 27 | | | 29 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | −1085 | −1005 | −880 | −1025 | −955 | −880 | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | −1830 | −1695 | −1555 | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Output parameters vary 1:1 with GND. $V_{CC}$ can vary +0.3 V / −0.5 V.
6. All loading with 50 Ω resistor to GND − 2.0 V.

**Table 6. AC CHARACTERISTICS** ($V_{CC}$ = 3.3 V; $V_{EE}$ = −3.0 V to −5.5 V; GND = 0 V (Note 7))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency | | 600 | | | 600 | | | 600 | | MHz |
| $T_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Differential Configuration<br>D to Q<br>Select-Ended | 490<br>440 | 590<br>590 | 690<br>740 | 520<br>470 | 620<br>620 | 720<br>770 | 560<br>510 | 660<br>660 | 760<br>810 | ps |
| $t_{SKEW}$ | Skew<br>Output-to-Output (Note 8)<br>Part-to-Part (Differential Configuration) (Note 8)<br>Duty Cycle (Differential Configuration) (Note 9) | | 40<br><br>25 | 100<br>200 | | 40<br><br>25 | 100<br>200 | | 40<br><br>25 | 100<br>200 | ps |
| $V_{PP}$ | Input Swing (Note 10) | 200 | | 1000 | 200 | | 1000 | 200 | | 1000 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q<br>(20% − 80%) | 320 | 400 | 580 | 320 | 400 | 580 | 320 | 400 | 580 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. $V_{CC}$ can vary +0.5 V / −0.3 V.
8. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
9. Duty cycle skew is the difference between a $T_{PLH}$ and $T_{PHL}$ propagation delay through a device.
10. $V_{PP}$(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40.

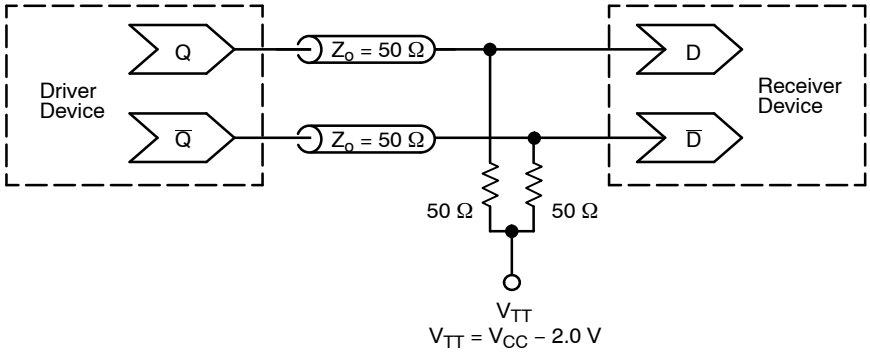



**Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

# MC100LVEL91

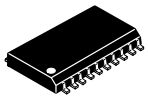
## Resource Reference of Application Notes

| | | |
|---|---|---|
| AN1405/D | – | ECL Clock Distribution Techniques |
| AN1406/D | – | Designing with PECL (ECL at +5.0 V) |
| AN1503/D | – | ECLinPS™ I/O SPiCE Modeling Kit |
| AN1504/D | – | Metastability and the ECLinPS Family |
| AN1568/D | – | Interfacing Between LVDS and ECL |
| AN1672/D | – | The ECL Translator Guide |
| AND8001/D | – | Odd Number Counters Design |
| AND8002/D | – | Marking and Date Codes |
| AND8020/D | – | Termination of ECL Logic Devices |
| AND8066/D | – | Interfacing with ECLinPS |
| AND8090/D | – | AC Characteristics of ECL Devices |

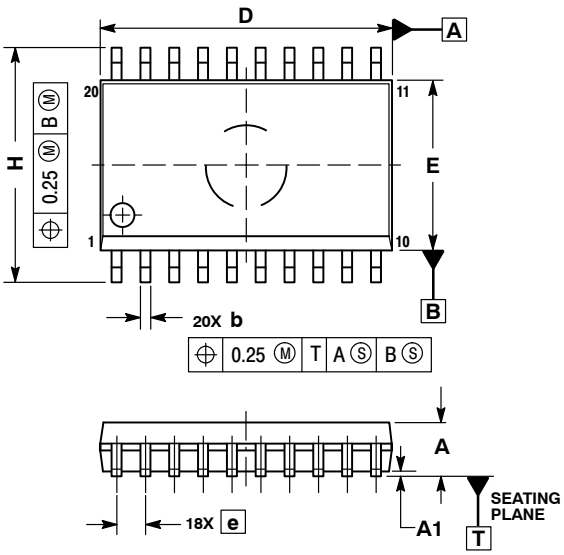
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



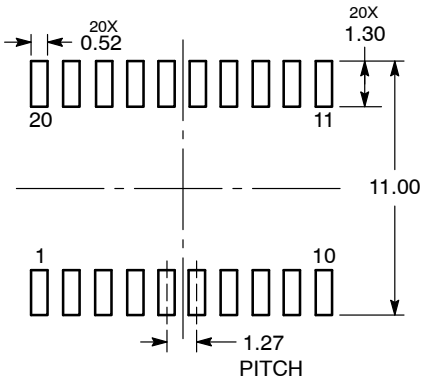
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

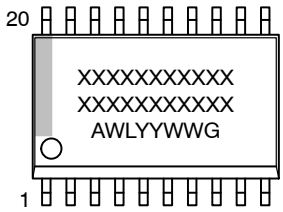
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42343B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOIC−20 WB** | | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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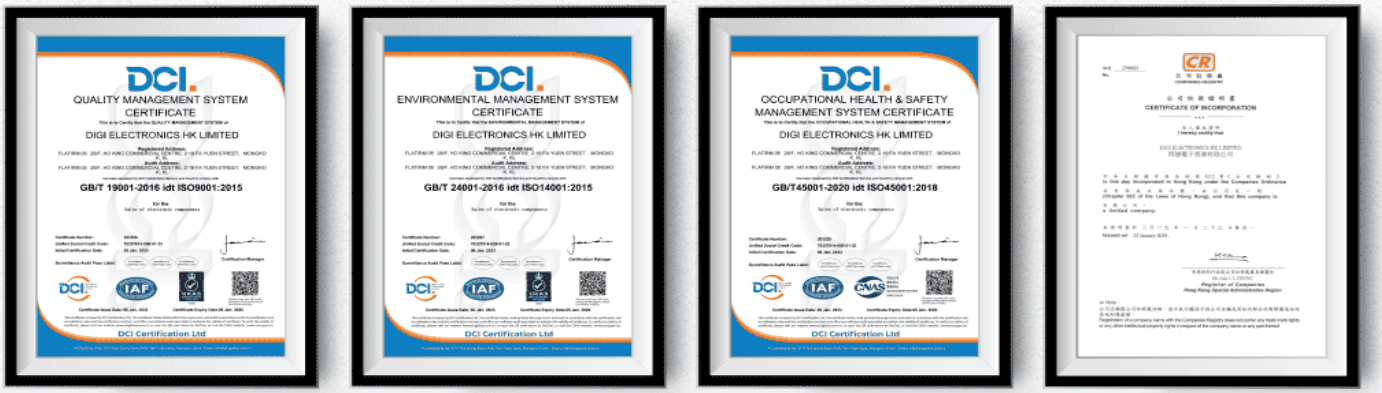



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