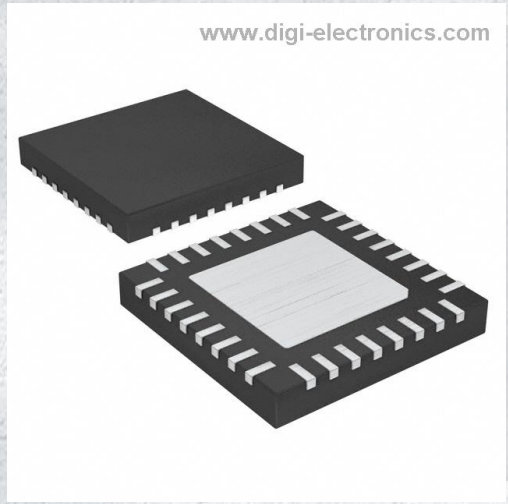
MC100LVEP210MNG Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MC100LVEP210MNG-DG
Manufacturer	onsemi
Manufacturer Product Number	MC100LVEP210MNG
Description	IC CLK BUFFER 1:5 3GHZ 32QFN
Detailed Description	Clock Fanout Buffer (Distribution) IC 1:5 3 GHz 32-V FQFN Exposed Pad

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MC100LVEP210MNG	onsemi
Series:	Product Status:
100LVEP	Obsolete
Type:	Number of Circuits:
Fanout Buffer (Distribution)	2
Ratio - Input:Output:	Differential - Input:Output:
1:5	Yes/Yes
Input:	Output:
ECL, HSTL, LVDS, PECL	ECL, PECL
Frequency - Max:	Voltage - Supply:
3 GHz	2.375V ~ 3.8V
Operating Temperature:	Mounting Type:
-40°C ~ 85°C	Surface Mount
Package / Case:	Supplier Device Package:
32-VFQFN Exposed Pad	32-QFN (5x5)
Base Product Number:	
MC100LV	

Environmental & Export classification

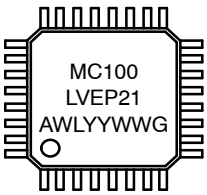
Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001

2.5 V / 3.3 V 1:5 Dual Differential ECL/PECL/HSTL Clock Driver

MC100LVEP210

LQFP−32
FA SUFFIX
CASE 561AB

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

The MC100LVEP210 is a low skew 1−to−5 dual differential driver, designed with clock distribution in mind. The ECL/PECL input signals can be either differential or single−ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs. HSTL inputs can be used when the EP210 is operating in PECL mode.

The LVEP210 specifically guarantees low output−to−output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

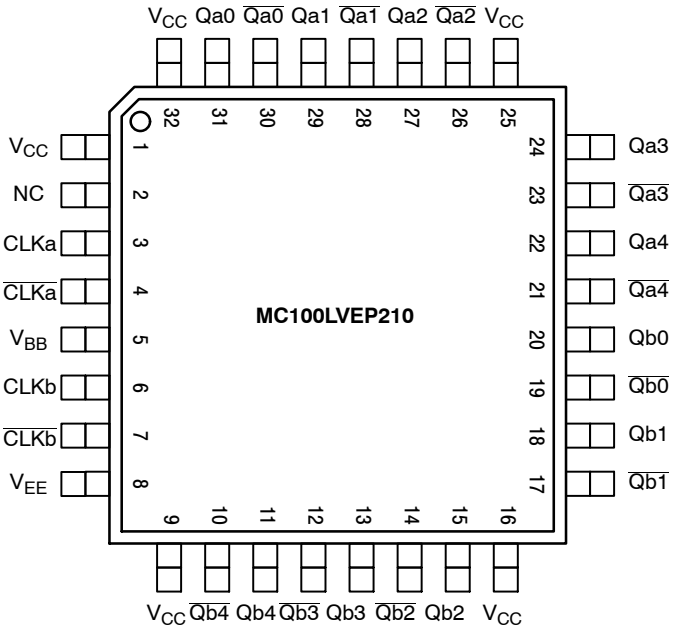
The MC100LVEP210, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP210 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single−ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in ECL mode.

Designers can take advantage of the LVEP210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D.

Features

- 85 ps Typical Device−to−Device Skew
- 20 ps Typical Output−to−Output Skew
- V_{BB} Output
- Jitter Less than 1 ps RMS
- 350 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.8 V
- Open Input Default State
- LVDS Input Compatible
- Fully Compatible with MC100EP210
- These are Pb−Free Devices

MC100LVEP210



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP−32 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLKn*, $\overline{\text{CLKn}}$**	ECL/PECL/HSTL CLK Inputs
Qn0:4, $\overline{\text{Qn0:4}}$	ECL/PECL Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

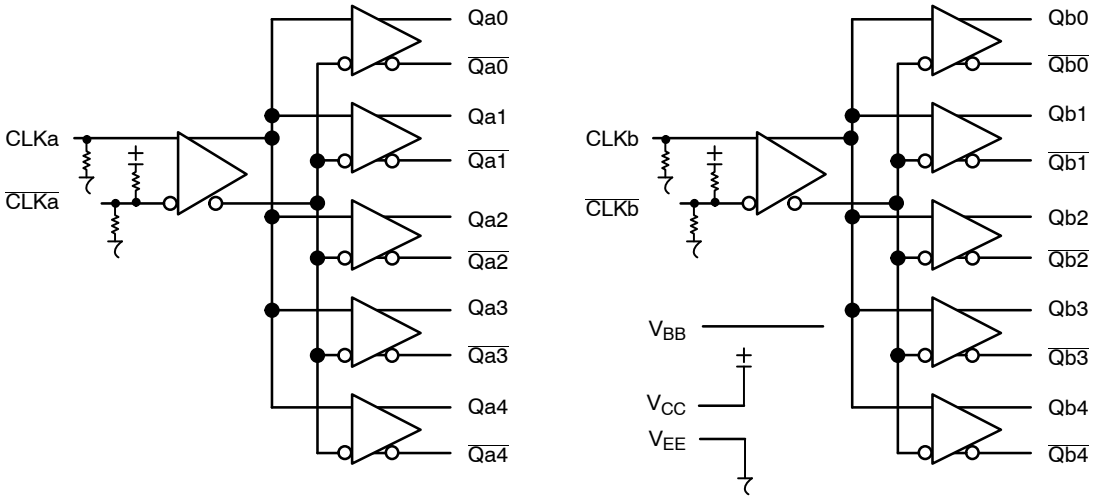


Figure 2. Logic Diagram

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pull−up Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)		Pb−Free Pkg Level 2
	LQFP−32	
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		461 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	LQFP−32	12 to 17	°C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. PECL DC CHARACTERISTICS V_{CC} = 2.5 V; V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	55	70	90	55	70	90	55	70	90	mA
V_{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 3)	505	680	900	505	680	900	505	680	900	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{IL}	Input LOW Voltage (Single−Ended)	505		900	505		900	505		900	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary + 0.125 V to −1.3 V.
3. All loading with 50 Ω to V_{EE}.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. PECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	55	70	90	55	70	90	55	70	90	mA
V_{OH}	Output HIGH Voltage (Note 6)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 6)	1305	1480	1700	1305	1480	1700	1305	1480	1700	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1305		1700	1305		1700	1305		1700	mV
V_{BB}	Output Reference Voltage (Note 7)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary + 0.925 V to −0.5 V.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. Single−ended input operation is limited $V_{CC} \geq$ 3.0 V in PECL mode.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. NECL DC CHARACTERISTICS V_{CC} = 0 V, V_{EE} = −2.375 V to −3.8 V (Note 9)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	55	70	90	55	70	90	55	70	90	mA
V_{OH}	Output HIGH Voltage (Note 10)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 10)	−1995	−1820	−1600	−1995	−1820	−1600	−1995	−1820	−1600	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1995		−1600	−1995		−1600	−1995		−1600	mV
V_{BB}	Output Reference Voltage (Note 11)	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. Input and output parameters vary 1:1 with V_{CC}.
10. All loading with 50 Ω to V_{CC} − 2.0 V.
11. Single−ended input operation is limited $V_{EE} \le$ −3.0V in NECL mode.
12. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. HSTL DC CHARACTERISTICS V_{CC} = 2.375 to 3.8 V, V_{EE} = 0 V

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			1200			mV
V_{IL}	Input LOW Voltage			400			400			400	mV
V_{CM}	Input Crossover Voltage	680		900	680		900	680		900	mV
I_{CC}	Power Supply Current (Outputs Open)	55	70	90	55	70	90	55	70	90	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 8. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −2.375 to −3.8 V or V_{CC} = 2.375 to 3.8 V; V_{EE} = 0 V (Note 13)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{maxPECL/HSTL}$	Maximum Frequency (Figure 3)		3			3			3		GHz
t_{PLH}/t_{PHL}	Propagation Delay @ 2.5 V Propagation Delay @ 3.3 V	220 220	300 300	380 380	270 270	350 350	430 430	300 330	400 410	500 490	ps
t_{skew}	Within−Device Skew (Note 14) Device−to−Device Skew (Note 15)		20 85	25 160		20 85	25 160		20 85	35 160	ps
t_{JITTER}	CLOCK Random Jitter (RMS) @ ≤0.5 GHz @ ≤1.0 GHz @ ≤1.5 GHz @ ≤2.0 GHz @ ≤2.5 GHz @ ≤3.0 GHz		 0.184 0.190 0.178 0.196 0.239 0.336	 0.3 0.3 0.3 0.3 0.4 0.5		 0.207 0.200 0.197 0.233 0.301 0.422	 0.3 0.3 0.3 0.4 0.4 0.5		 0.271 0.252 0.259 0.308 0.399 0.572	 0.4 0.4 0.4 0.5 0.5 0.9	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%−80%)	100	170	250	120	190	270	150	280	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

13. Measured with 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
14. Skew is measured between outputs under identical transitions of similar paths through a device.
15. Device−to−Device skew for identical transitions at identical V_{CC} levels.

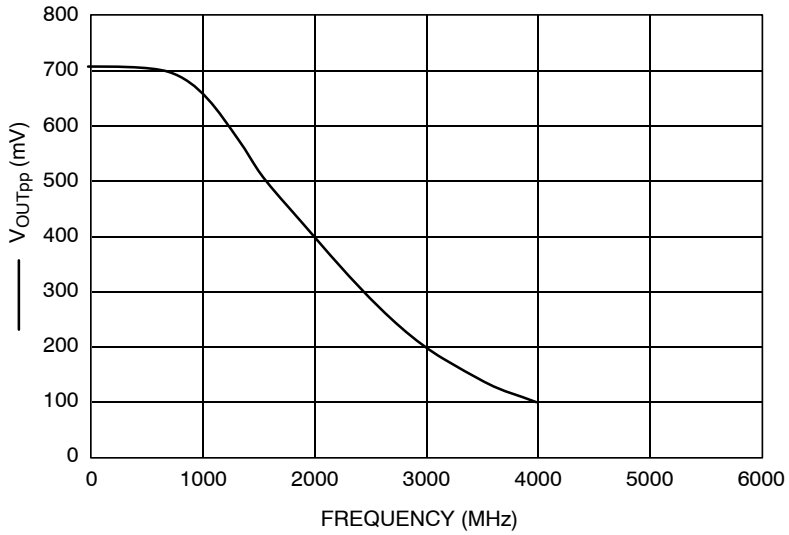


Figure 3. F_{max} Typical

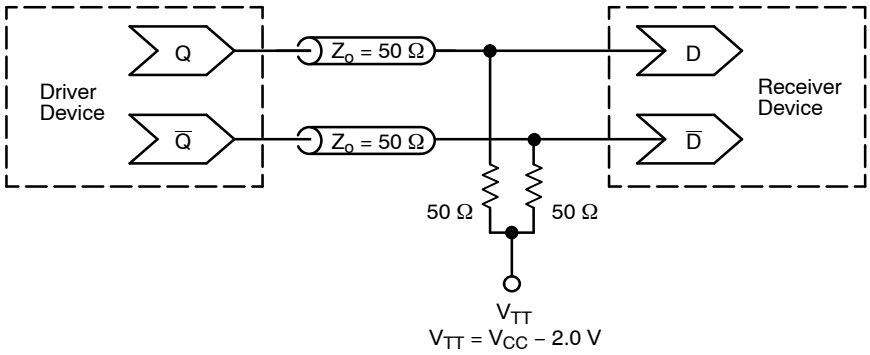


Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEP210FAG	LQFP (Pb−Free)	250 Units / Tray
MC100LVEP210FARG	LQFP (Pb−Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

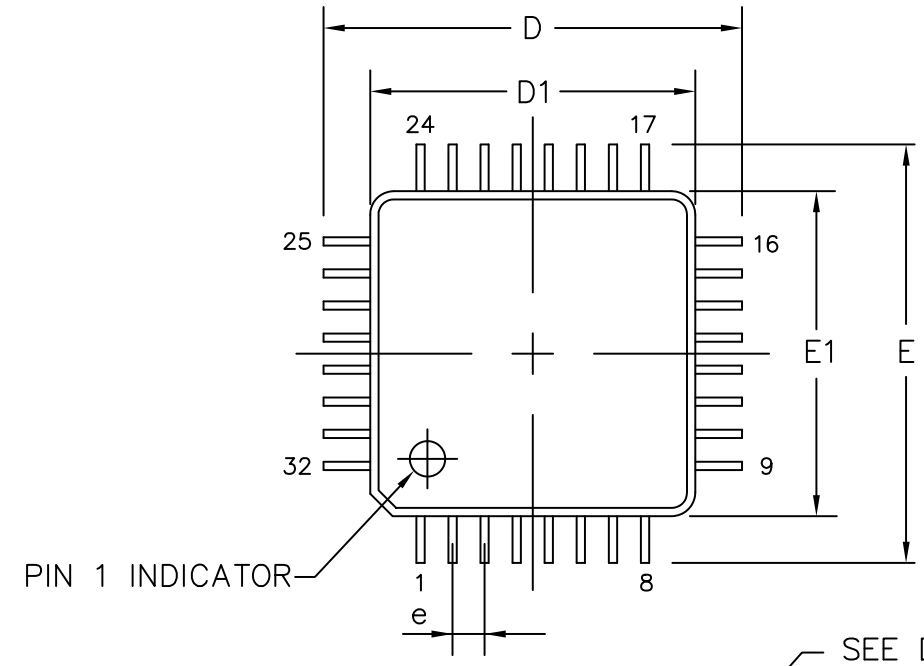
Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques
AN1406/D – Designing with PECL (ECL at +5.0 V)
AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D – Metastability and the ECLinPS Family
AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide
AND8001/D – Odd Number Counters Design
AND8002/D – Marking and Date Codes
AND8020/D – Termination of ECL Logic Devices
AND8066/D – Interfacing with ECLinPS
AND8090/D – AC Characteristics of ECL Devices

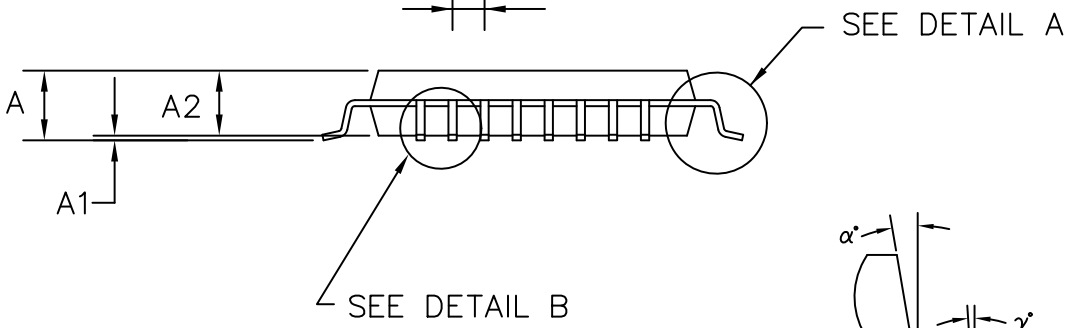
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

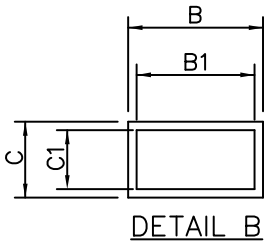
LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 2008

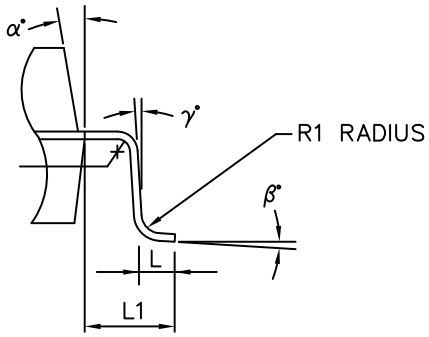


SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–





DETAIL B



DETAIL A

ALL DIMENSIONS IN MM

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DESCRIPTION:	**32 LEAD LQFP, 7X7**	**PAGE 1 OF 1**

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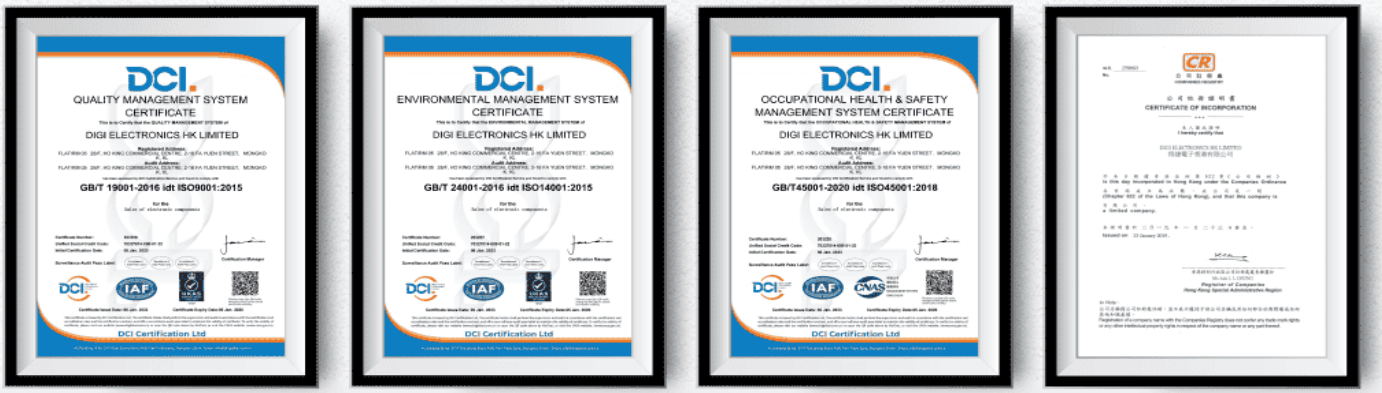

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