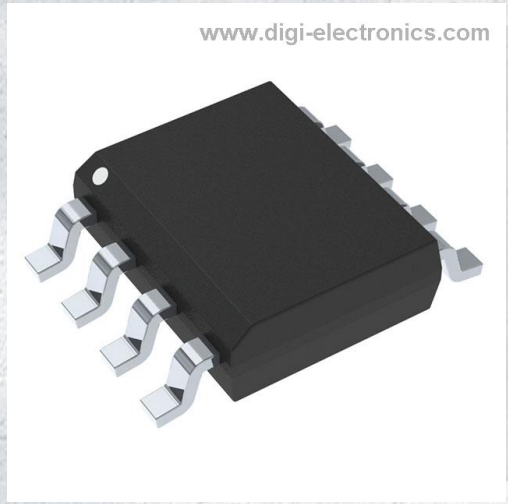
MC12026ADR2G Datasheet



DiGi Electronics Part Number	MC12026ADR2G-DG
Manufacturer	onsemi
Manufacturer Product Number	MC12026ADR2G
Description	IC PRESCALER 8SOIC
Detailed Description	Prescaler IC 1.1GHz 1 8-SOIC (0.154", 3.90mm Width)

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MC12026ADR2G	onsemi
Series:	Product Status:
-	Active
DiGi-Electronics Programmable:	Type:
Not Verified	Prescaler
PLL:	Input:
No	CMOS, TTL
Output:	Number of Circuits:
ECL	1
Ratio - Input:Output:	Differential - Input:Output:
1:1	No/No
Frequency - Max:	Divider/Multiplier:
1.1GHz	Yes/No
Voltage - Supply:	Operating Temperature:
4.5V ~ 5.5V	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
8-SOIC	MC12026

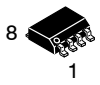
Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

DATA SHEET
www.onsemi.com

1.1 GHz Dual Modulus Prescaler

MC12026A



SOIC−8 NB
D SUFFIX
CASE
751−07

Description

The MC12026A is a high frequency, low voltage dual modulus prescaler used in phase-locked loop (PLL) applications.

The MC12026A can be used with CMOS synthesizers requiring positive edges to trigger internal counters in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of an 8/9 or 16/17 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

Features

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of −40 to 85°C
- The MC12026 is Pin Compatible with the MC12022
- Short Setup Time (t_{set}) 6.0 ns Typical @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Table 1. FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	8
H	L	9
L	H	16
L	L	17

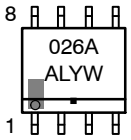
1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

Table 2. MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to 7.0	Vdc
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Modulus Control Input, Pin 6	MC	−0.5 to 6.5	Vdc
Maximum Output Current, Pin 4	I_O	10.0	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
NOTE: ESD data available upon request.

MARKING DIAGRAM

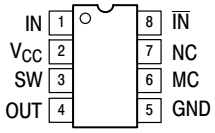


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MC12026ADR2G	SOIC−8 NB (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

MC12026ADG	SOIC−8 NB (Pb-Free)	98 Units/Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

Table 3. ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5; T_A = −40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sin Wave)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	–	4.0	5.3	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	–
Output Voltage Swing (R_L = 560 Ω; I_O = 5.5 mA) (Note 1) (R_L = 1.1 kΩ; I_O = 2.9 mA) (Note 2)	V_{out}	1.0	1.6	–	V_{pp}
Modulus Setup Time MC to Out (Note 3)	t_{SET}	–	6.0	9.0	ns
Input Voltage Sensitivity 100–250 MHz 250–1100 MHz	V_{in}	 400 100	 – –	 1000 1000	mVpp

1. Divide Ratio of ÷8/9 at 1.1 GHz, C_L = 8.0 pF.
2. Divide Ratio of ÷16/17 at 1.1 GHz, C_L = 8.0 pF.
3. Assuming R_L = 560 Ω at 1.1 GHz.

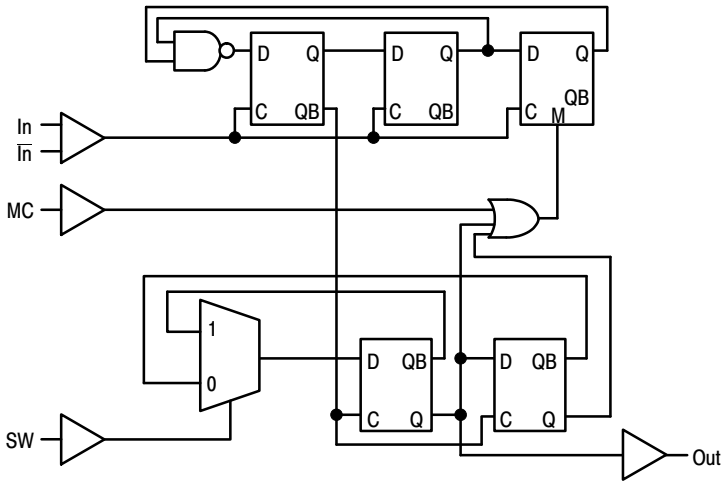
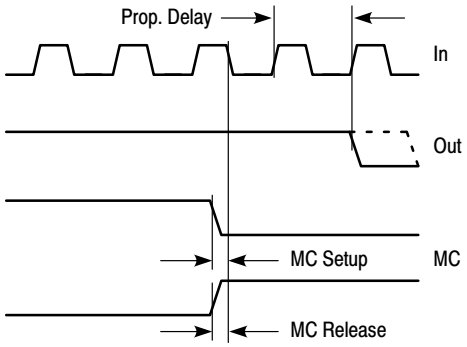


Figure 1. Logic Diagram (MC12026A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

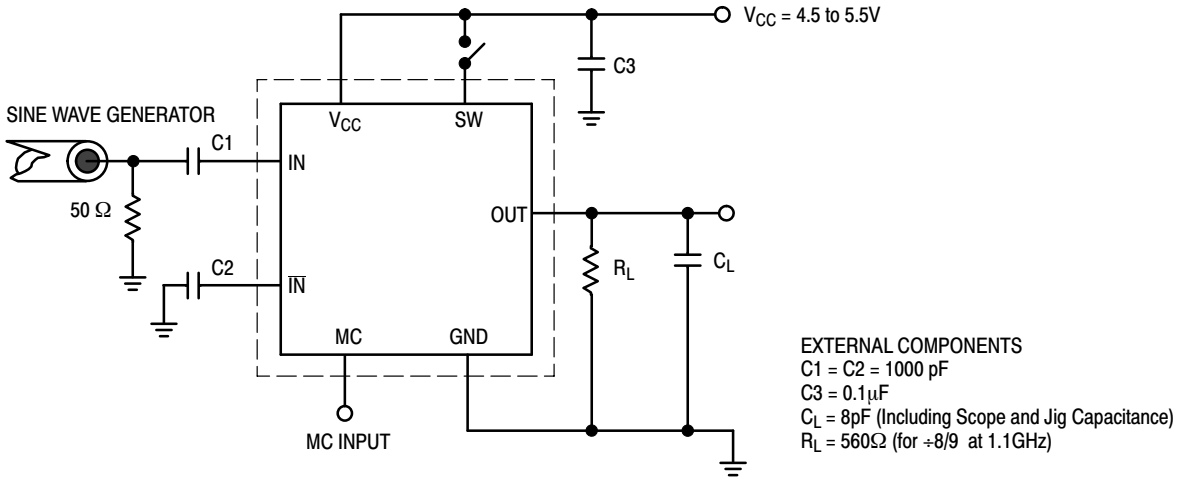
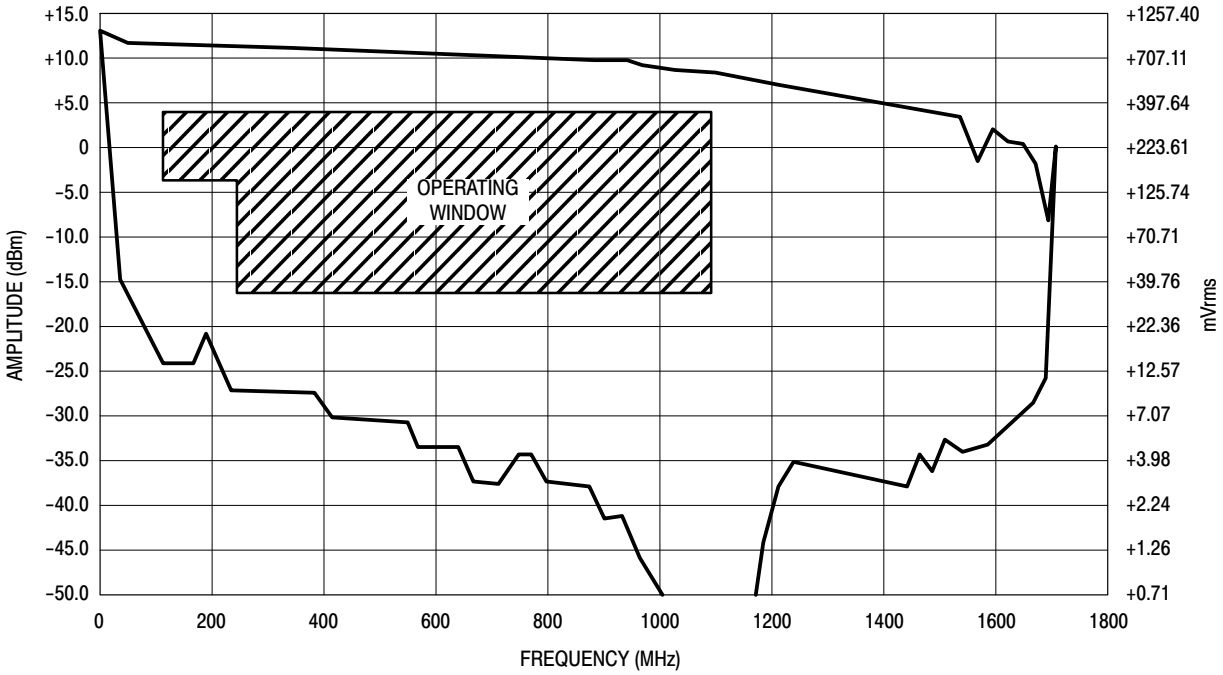


Figure 3. AC Test Circuit



Divide Ratio = 8; V_{CC} = 5.0 V; T_A = 25°C

Figure 4. Input Signal Amplitude Versus Input Frequency

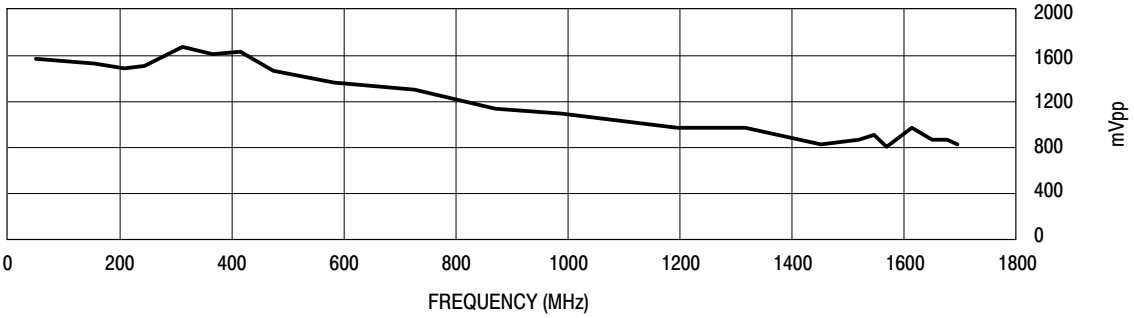
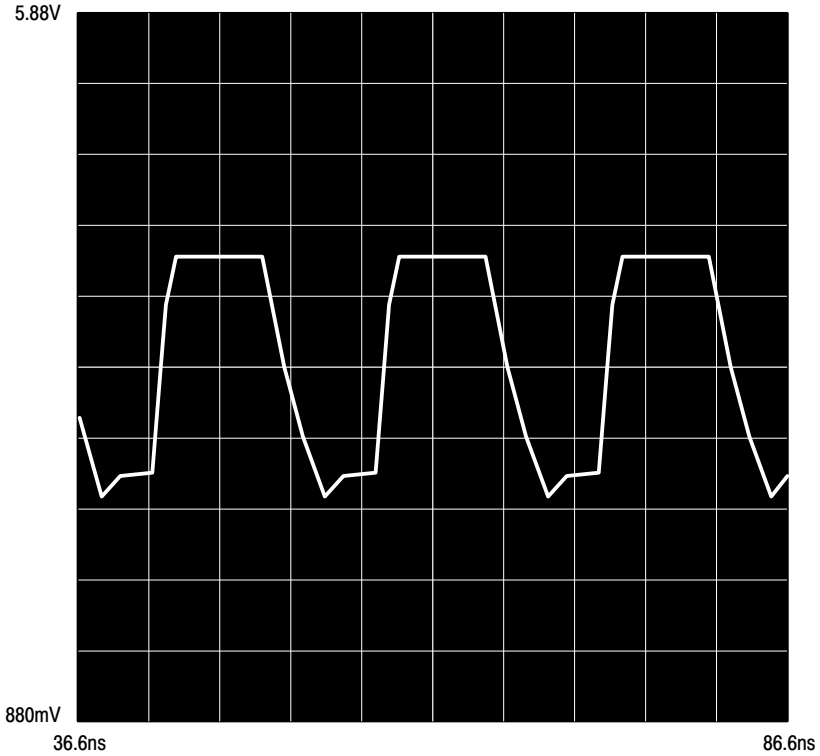


Figure 5. Output Amplitude Versus Input Frequency



(÷8, 1.1 GHz Input Frequency, V_{CC} = 5.0, T_A = 25°C, Output Loaded With 8.0pF)

Figure 6. Typical Output Waveform

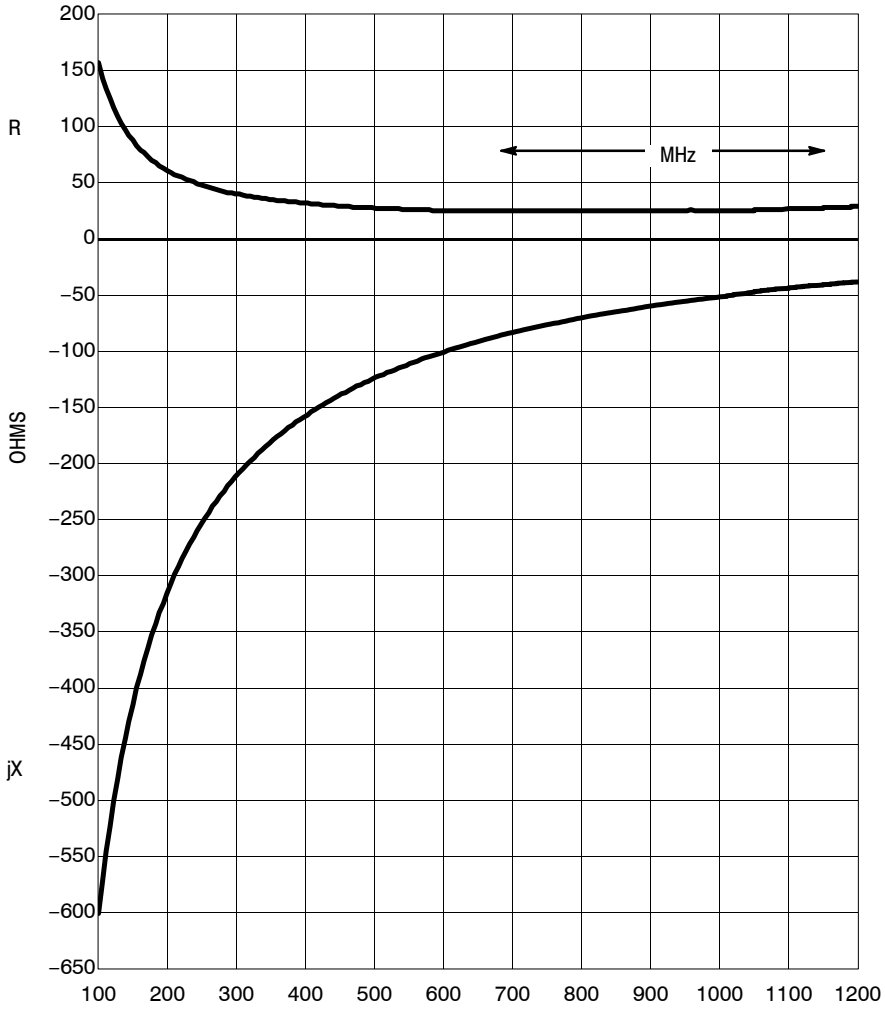


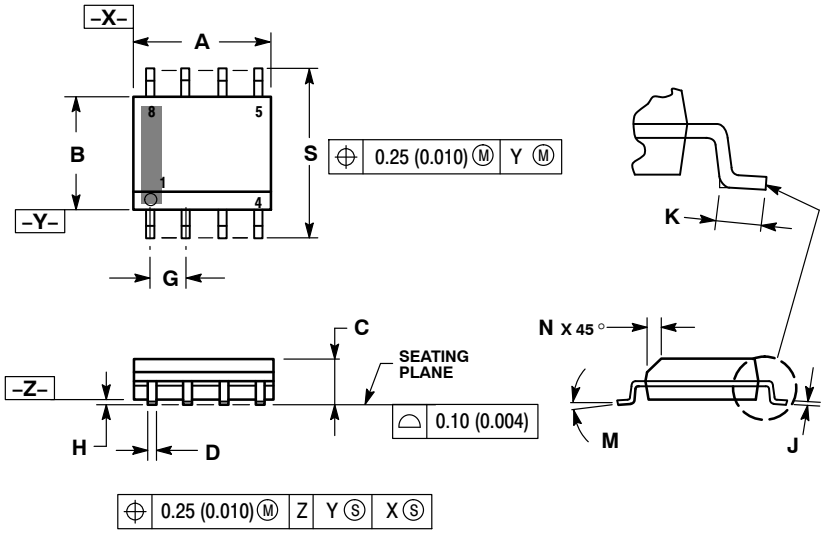
Figure 7. Typical Input Impedance Versus Input Frequency

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

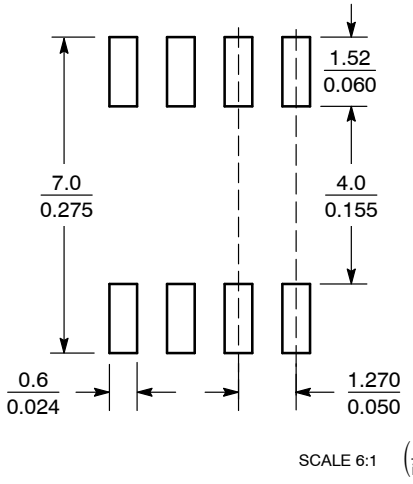
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

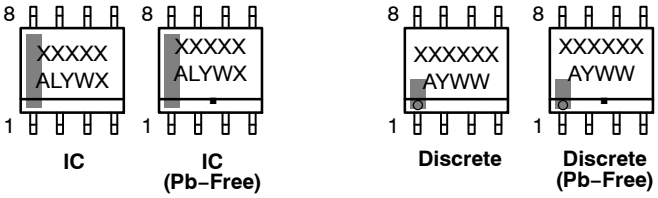
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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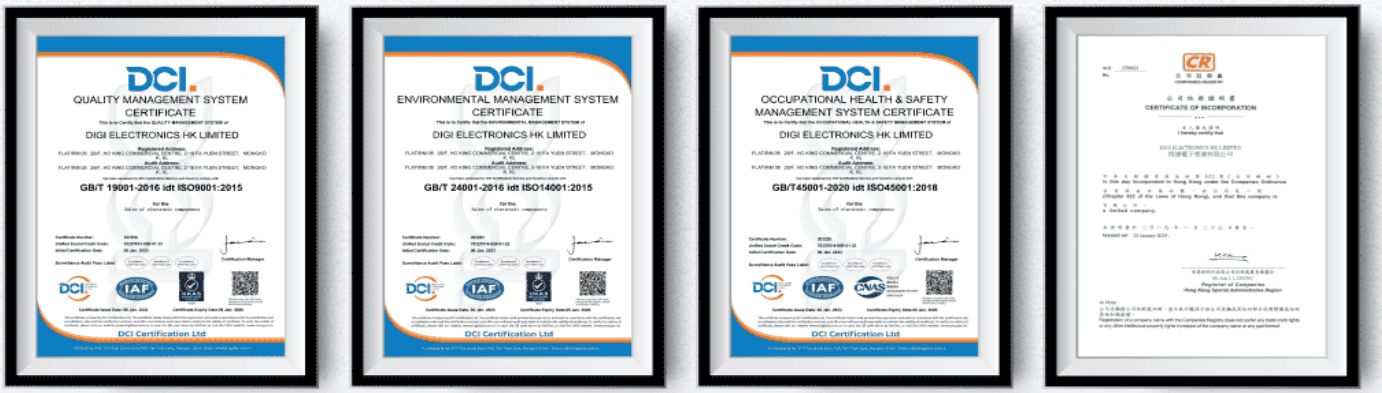

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