

MC1489ADR2 Datasheet



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DiGi Electronics Part Number

MC1489ADR2-DG

Manufacturer

onsemi

Manufacturer Product Number

MC1489ADR2

Description

IC RECEIVER 0/4 14SOIC

Detailed Description

0/4 Receiver RS232 14-SOIC



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RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MC1489ADR2	onsemi
Series:	Product Status:
	Obsolete
Type:	Protocol:
Receiver	RS232
Number of Drivers/Receivers:	Voltage - Supply:
0/4	4.5V ~ 5.5V
Mounting Type:	Package / Case:
Surface Mount	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
14-SOIC	MC1489

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

8542.39.0001

Quad Line EIA-232D Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA–232D.

Features

- Input Resistance 3.0 k to 7.0 k Ω
- Input Signal Range ± 30 V
- Input Threshold Hysteresis Built In
- Response Control
 - a) Logic Threshold Shifting
 - b) Input Noise Filtering
- Pb-Free Packages are Available

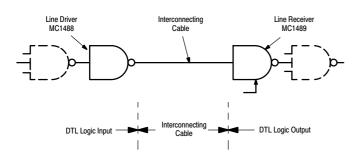


Figure 1. Simplified Application

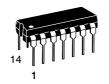


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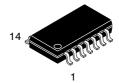
http://onsemi.com



SOIC-14 D SUFFIX CASE 751A

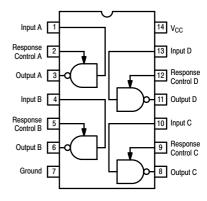


PDIP-14 P SUFFIX CASE 646



SOEIAJ-14 M SUFFIX CASE 965

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

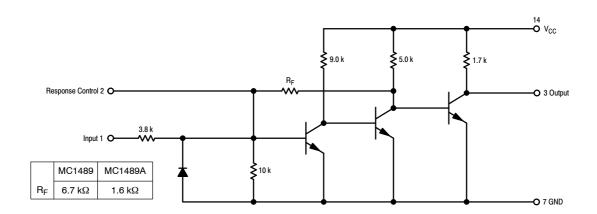


Figure 2. Representative Schematic Diagram (1/4 of Circuit Shown)

MAXIMUM RATINGS ($T_A = +25^{\circ}C$, unless otherwise noted)

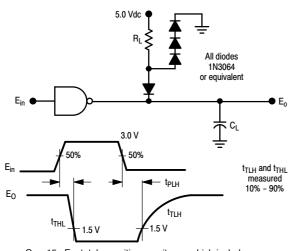
Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	10	Vdc
Input Voltage Range	V _{IR}	± 30	Vdc
Output Load Current	ΙL	20	mA
Power Dissipation (Package Limitation, SOIC–14 and Plastic Dual In–Line Package) Derate above T _A = + 25°C	P _D 1/ _{θJA}	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T _A	0 to + 75	°C
Storage Temperature Range	T _{stg}	– 65 to + 175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (Response control pin is open.) $(V_{CC} = +5.0 \text{ Vdc} \pm 10\%, T_A = 0 \text{ to } +75^{\circ}\text{C}, \text{ unless otherwise noted})$

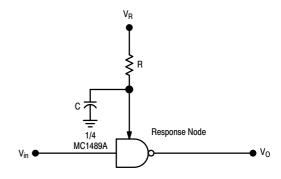
Characteristics		Symbol	Min	Тур	Max	Unit
Positive Input Current	(V _{IH} = + 25 Vdc) (V _{IH} = + 3.0 Vdc)	I _{IH}	3.6 0.43	- -	8.3 -	mA
Negative Input Current	$(V_{IH} = -25 \text{ Vdc})$ $(V_{IH} = -3.0 \text{ Vdc})$	I _{IL}	- 3.6 - 0.43	1 1	- 8.3 -	mA
Input Turn–On Threshold Voltage $(T_A = +25^{\circ}C, V_{OL} \le 0.45 \text{ V})$	MC1489 MC1489A	V _{IH}	1.0 1.75	- 1.95	1.5 2.25	Vdc
Input Turn–Off Threshold Voltage $(T_A = +25^{\circ}C, V_{OH} \ge 2.5 \text{ V}, I_L = -0.5 \text{ mA})$	MC1489 MC1489A	V _{IL}	0.75 0.75	- 0.8	1.25 1.25	Vdc
Output Voltage High $(V_{IH} = 0.75 V, (Input Open Ci$	$I_L = -0.5 \text{ mA}$) rcuit, $I_L = -0.5 \text{ mA}$)	V _{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low $(V_{IL} = 3.0 \text{ V}, I_L)$	= 10 mA)	V _{OL}	_	0.2	0.45	Vdc
Output Short-Circuit Current		I _{OS}	-	- 3.0	- 4.0	mA
Power Supply Current (All Gates "on," Iout = 0 m	A, V _{IH} = + 5.0 Vdc)	I _{CC}	-	16	26	mA
Power Consumption	(V _{IH} = + 5.0 Vdc)	P _C	_	80	130	mW
SWITCHING CHARACTERISTICS (V _{CC} = 5	.0 Vdc ± 1%, T _A = + 25°C, S	See Figure 3.)				
Propagation Delay Time	$(R_L = 3.9 \text{ k}\Omega)$	t _{PLH}	_	25	85	ns
Rise Time	$(R_L = 3.9 \text{ k}\Omega)$	t _{TLH}	-	120	175	ns
Propagation Delay Time	(R _L = 390 kΩ)	t _{PHL}	-	25	50	ns
Fall Time	(R _L = 390 kΩ)	t _{THL}	_	10	20	ns

TEST CIRCUITS



 $\mbox{C}_{L} =$ 15 pF = total parasitic capacitance which includes probe and wiring capacitances

Figure 3. Switching Response



C, capacitor is for noise filtering. R, resistor is for threshold shifting.

Figure 4. Response Control Node

TYPICAL CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted)

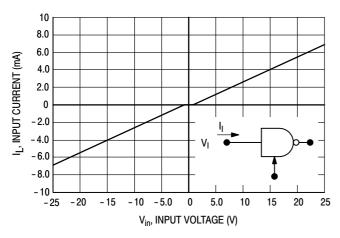


Figure 5. Input Current

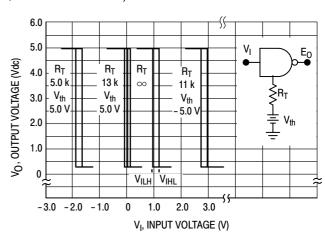


Figure 6. MC1489 Input Threshold Voltage Adjustment

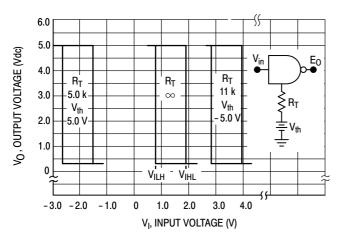


Figure 7. MC1489A Input Threshold Voltage Adjustment

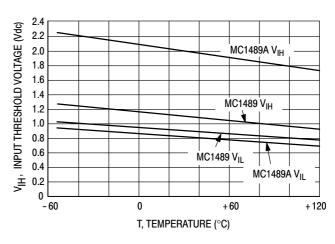


Figure 8. Input Threshold Voltage versus Temperature

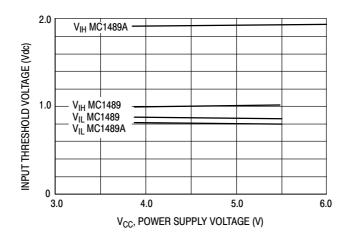


Figure 9. Input Threshold versus Power Supply Voltage

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between $3000~\Omega$ and $7000~\Omega$ for input voltages between 3.0 and 25~V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0~V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} .

The receiver shall detect a voltage between -3.0 and $-25\,\mathrm{V}$ as a Logic "1" and inputs between 3.0 and 25 V as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical

turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 4, 6 and 7 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 10 and 11 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and DTL/TTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 12).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 13 where two receivers are slaved to the same line that must still meet the EIA–232D impedance requirement.

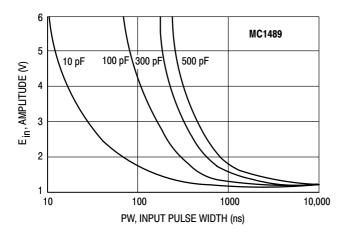


Figure 10. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

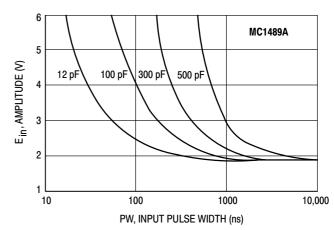


Figure 11. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

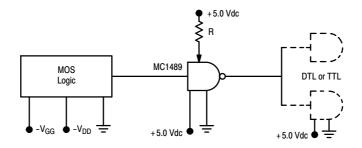


Figure 12. Typical Translator Application - MOS to DTL or TTL

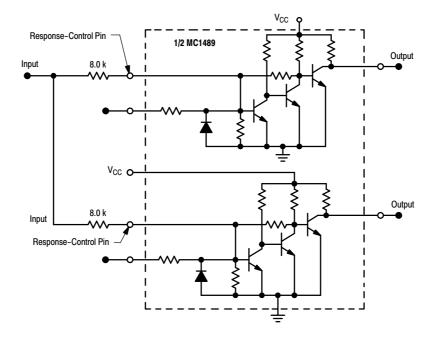


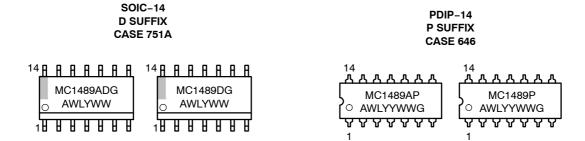
Figure 13. Typical Paralleling of Two MC1489, A Receivers to Meet EIA-232D

ORDERING INFORMATION

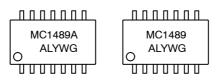
Device	Package	Operating Temperature Range	Shipping [†]
MC1489D	SOIC-14		
MC1489DG	SOIC-14		55 Units/Rail
	(Pb-Free)		
MC1489DR2	SOIC-14		
MC1489DR2G	SOIC-14		2500 Tape & Reel
	(Pb-Free)		
MC1489AD	SOIC-14		
MC1489ADG	SOIC-14		55 Units/Rail
	(Pb-Free)		
MC1489ADR2	SOIC-14		
MC1489ADR2G	SOIC-14		2500 Tape & Reel
	(Pb-Free)		
MC1489P	PDIP-14	1	
MC1489PG	PDIP-14	1	
	(Pb-Free)	T _A = 0 to +75°C	OF Unito/Dail
MC1489AP	PDIP-14	1 _A = 0 to +75 C	25 Units/Rail
MC1489APG	PDIP-14	1	
	(Pb-Free)		
MC1489M	SOEIAJ-14]	
MC1489MG	SOEIAJ-14	1	50 Units/Rail
	(Pb-Free)		
MC1489MEL	SOEIAJ-14]	
MC1489MELG	SOEIAJ-14	1	2000 Tape & Reel
	(Pb-Free)		
MC1489AM	SOEIAJ-14]	
MC1489AMG	SOEIAJ-14	1	50 Units/Rail
	(Pb-Free)		
MC1489AMEL	SOEIAJ-14]	
MC1489AMELG	SOEIAJ-14	1	2000 Tape & Reel
	(Pb-Free)		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



SOEIAJ-14 M SUFFIX CASE 965



A = Assembly Location

 $\begin{array}{lll} WL,\,L &= Wafer\,Lot\\ YY,\,Y &= Year\\ WW,\,W &= Work\,Week\\ G &= Pb-Free\,Package \end{array}$



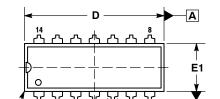
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



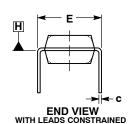
PDIP-14 CASE 646-06 **ISSUE S**

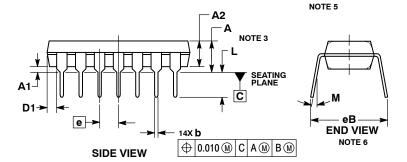
DATE 22 APR 2015



TOP VIEW

NOTE 8





В

NOTES:

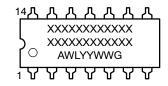
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3. DIMENSIONS D, D1 AND E1 D0 NOT INCLUDE MOLD FLASH
- OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
- DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
 DIMENSION & B IS MEASURED AT THE LEAD TIPS WITH THE
- DIMENSION BY IS MEASURED AT THE LEAD TIFS WITH THE LEADS UNCONSTRAINED.

 DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.

 PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α		0.210		5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060	TYP	1.52	TYP
С	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
е	0.100 BSC		2.54	BSC
eВ		0.430		10.92
L	0.115	0.150	2.92	3.81
M		10°		10°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week = Pb-Free Package G

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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PDIP-14 CASE 646-06 ISSUE S

DATE 22 APR 2015

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. DRAIN 2. SOURCE 3. GATE 4. NO CONNECTION 5. GATE 6. SOURCE 7. DRAIN 8. DRAIN 9. SOURCE 10. GATE 11. NO CONNECTION 12. GATE 13. SOURCE 14. DRAIN
STYLE 5: PIN 1. GATE 2. DRAIN 3. SOURCE 4. NO CONNECTION 5. SOURCE 6. DRAIN 7. GATE 8. GATE 9. DRAIN 10. SOURCE 11. NO CONNECTION 12. SOURCE 13. DRAIN 14. GATE	STYLE 6: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 7: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 8: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 9: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE	STYLE 10: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 11: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 12: PIN 1. COMMON CATHODE 2. COMMON ANODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. COMMON ANODE 7. COMMON CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. ANODE/CATHODE 14. ANODE/CATHODE 14. ANODE/CATHODE

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MECHANICAL CASE OUTLINE

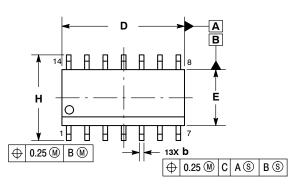
PACKAGE DIMENSIONS

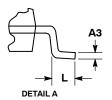


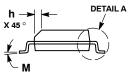
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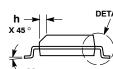
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016





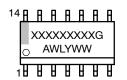




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
- MAXIMUM MATERIAL CONDITION.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE

	MILLIMETERS		MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX		
Α	1.35	1.75	0.054	0.068		
A1	0.10	0.25	0.004	0.010		
АЗ	0.19	0.25	0.008	0.010		
b	0.35	0.49	0.014	0.019		
D	8.55	8.75	0.337	0.344		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.019		
Ĺ	0.40	1.25	0.016	0.049		
М	0 °	7°	0 °	7°		

GENERIC MARKING DIAGRAM*

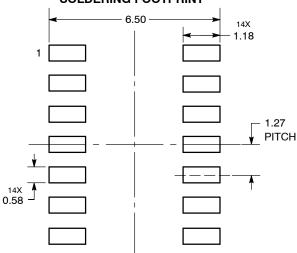


XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

C SEATING PLANE

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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DESCRIPTION:	SOIC-14 NB		PAGE 2 OF 2

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS





DATE 29 FEB 2008

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
- PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
 PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT
 INCLUDE DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
 TOTAL IN EXCESS OF THE LEAD WIDTH
 DEFINISHED AND MANUFER METERIAL CONDITION. DIMENSION AT MAXIMUM MATERIAL CONDITION.

 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE
 BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z		1.42		0.056

14	M° Q ₁ DETAIL P
VIEW A A D O.13 (0.005) O.10 (0.004)	° C

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