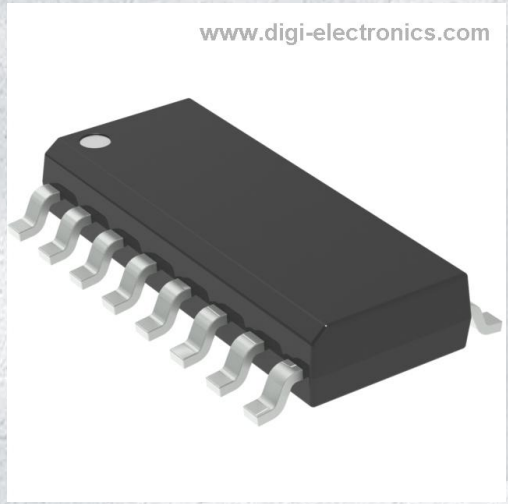
MC74AC4040DR2G Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MC74AC4040DR2G-DG
Manufacturer	onsemi
Manufacturer Product Number	MC74AC4040DR2G
Description	IC BINARY COUNTER 12-BIT 16SOIC
Detailed Description	Counter IC Binary Counter 1 Element 12 Bit Negative Edge 16-SOIC

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MC74AC4040DR2G	onsemi
Series:	Product Status:
74AC	Active
Logic Type:	Direction:
Binary Counter	Up
Number of Elements:	Number of Bits per Element:
1	12
Reset:	Timing:
Asynchronous	-
Count Rate:	Trigger Type:
140 MHz	Negative Edge
Voltage - Supply:	Operating Temperature:
2 V ~ 6 V	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package:	Base Product Number:
16-SOIC	74AC4040

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

onsemi

DATA SHEET
www.onsemi.com

12-Stage Binary Ripple Counter

MC74AC4040

The MC74AC4040 consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4040 for some designs.

Features

- 140 MHz Typ. Clock
- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity
- These are Pb−Free Devices

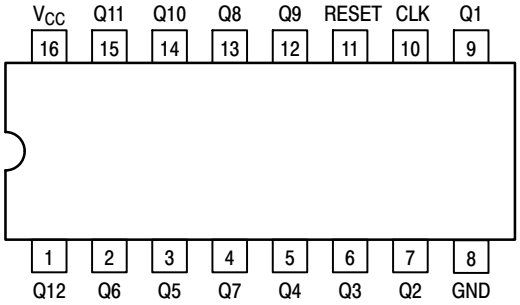
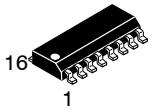


Figure 1. Pinout: 16−Lead Packages Conductors
(Top View)

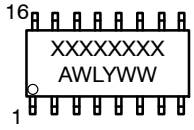
FUNCTION TABLE

Clock	Reset	Output State
⌐	L	No Change
¬	L	Advance to next state
X	H	All Outputs are low



SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



XXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

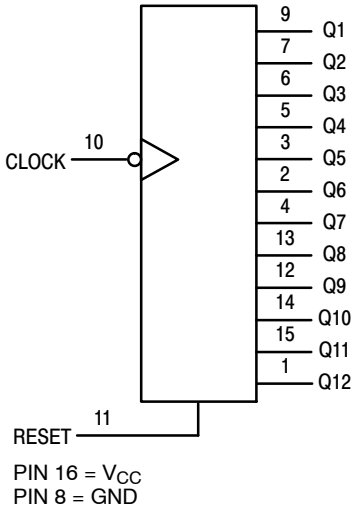


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage		$-0.5 \le V_{CC} +0.5$	V
V_O	DC Output Voltage (Note 1)		$-0.5 \le V_{CC} +0.5$	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±50	mA
I_O	DC Output Sink/Source Current		±50	mA
I_{CC}	DC Supply Current per Output Pin		±50	mA
I_{GND}	DC Ground Current per Output Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		126	°C/W
P_D	Power Dissipation in Still Air at 25°C		995	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	> 2000 > 1000	V
$I_{Latch-Up}$	Latch−Up Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}/V_{OUT}	Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	−
T_A	Operating Temperature, All Package Types		−40	+85	°C
t_r/t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 5.5 V	0 0 0	150 40 25	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74AC4040

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Conditions	Value	Unit
I_{CC}	Maximum Quiescent Supply Voltage	V_{in} = V_{CC} or GND V_{CC} = 5.5 V, T_A = Worst Case	80	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND V_{CC} = 5.5 V, T_A = 25°C	8.0	μA

DC CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	74AC T_A = +25°C Typ	74AC T_A = −40°C to +85°C Guaranteed Limits		Unit
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	3.0 4.5 5.5	– – –	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	3.0 4.5 5.5	– – –	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = −50 μA	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN} = V_{IL} or V_{IH} −12 mA I_{OH} −24 mA −24 mA	 3.0 4.5 5.5	 – – –	 2.56 3.86 4.86	 2.46 3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 μA	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA	 3.0 4.5 5.5	 – – –	 0.36 0.36 0.36	 0.44 0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC}, GND	5.5	–	±0.1	±1.0	μA
I_{OLD}	Minimum Dynamic Output Current†	V_{OLD} = 1.65 V Max	5.5	–	–	75	mA
I_{OHD}		V_{OHD} = 3.85 V Min	5.5	–	–	−75	mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC4040

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	Conditions	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF Min	Typ	Max	74AC T_A = –40°C to +85°C, C_L = 50 pF Min	Max	Unit
f_{max}	Maximum Clock Frequency		3.3 5.0	110 130	120 140	– –	100 120	– –	MHz
n_{CP} to Q1	Propagation Delay n_{CP} to Q1		3.3 5.0	2.0 2.0	– –	11 8.0	2.0 2.0	14 10	ns
Q_n to Q_n +1	Propagation Delay Q_n to Q_n +1		3.3 5.0	0 0	– –	5.5 3.5	0 0	6.5 4.5	ns
MR to Q t_{HL}	Propagation Delay MR to Q		3.3 5.0	3.0 3.0	– –	12 10	3.0 3.0	15 12	ns
t_{rec} n_{CP} to MR	Recovery Time		3.3 5.0	0 0	–2.5 –1.5	– –	0 0	– –	ns
t_w n_{CP}	Minimum Pulse Width Clock Pin		3.3 5.0	4.0 3.0	3.5 2.5	– –	4.5 3.5	– –	ns
t_w MR	Minimum Pulse Width Master Reset		3.3 3.0	4.0 3.0	3.5 2.5	– –	4.5 3.5	– –	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

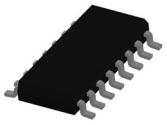
CAPACITANCE

Symbol	Parameter	Conditions	Value Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.0 V	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V	50	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74AC4040DR2G	AC4040G	SOIC–16 (Pb–Free)	2,500 Tape & Reel

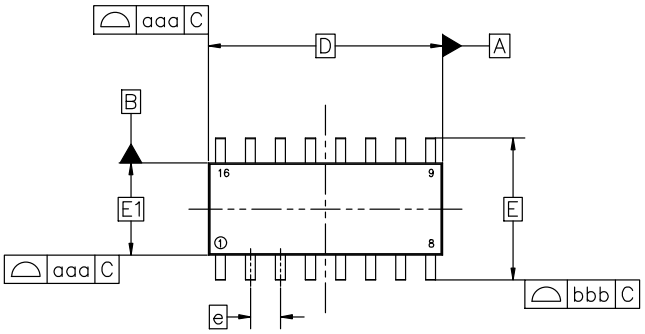
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



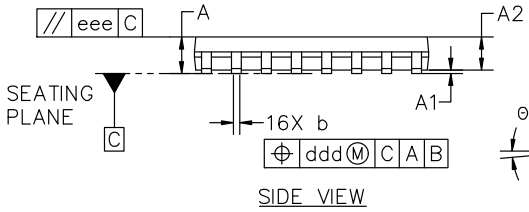
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

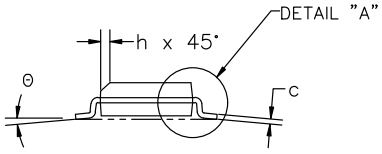
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



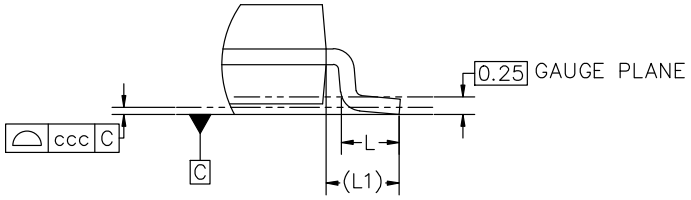
TOP VIEW



SIDE VIEW

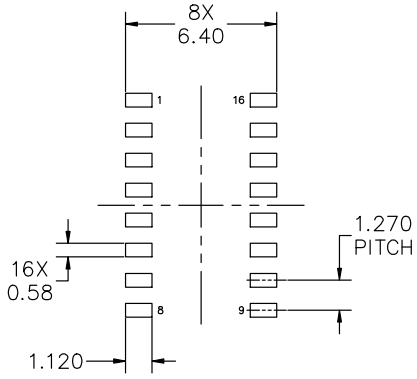


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

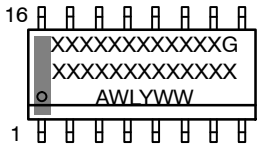
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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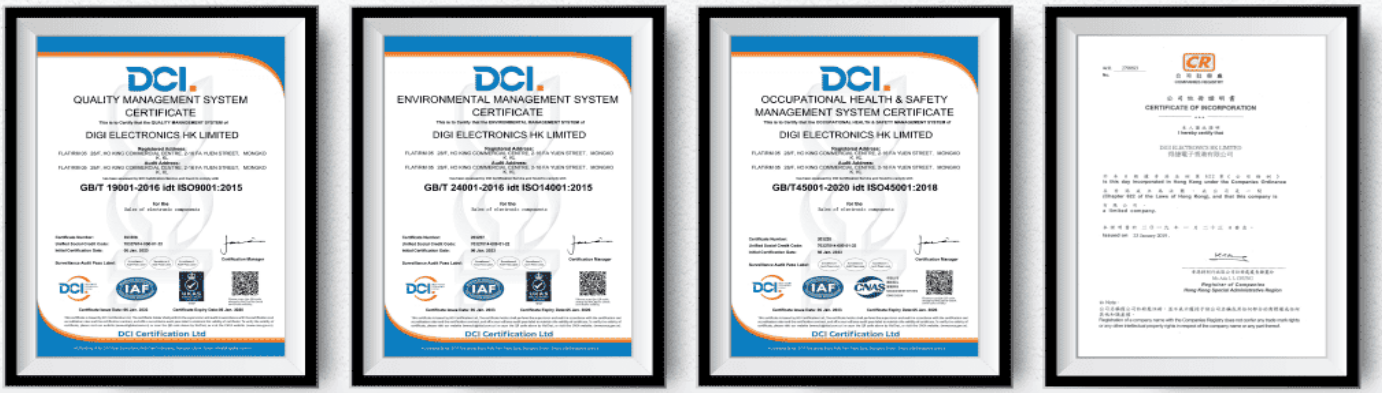

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