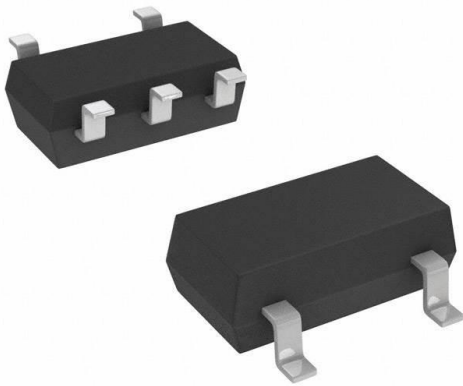


MC74HC1G08DFT1 Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	MC74HC1G08DFT1-DG
Manufacturer	onsemi
Manufacturer Product Number	MC74HC1G08DFT1
Description	IC GATE AND 1CH 2-INP SC88A
Detailed Description	AND Gate IC 1 Channel SC-88A (SC-70-5/SOT-353)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

MC74HC1G08DFT1

Series:

74HC

Logic Type:

AND Gate

Number of Inputs:

2

Voltage - Supply:

2V ~ 6V

Current - Output High, Low:

2.6mA, 2.6mA

Input Logic Level - High:

1.5V ~ 4.2V

Operating Temperature:

-55°C ~ 125°C

Supplier Device Package:

SC-88A (SC-70-5/SOT-353)

Base Product Number:

74HC1G08

Manufacturer:

onsemi

Product Status:

Obsolete

Number of Circuits:

1

Features:

-

Current - Quiescent (Max):

1 μ A

Input Logic Level - Low:

0.5V ~ 1.8V

Max Propagation Delay @ V, Max CL:

17ns @ 6V, 50pF

Mounting Type:

Surface Mount

Package / Case:

5-TSSOP, SC-70-5, SOT-353

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Single 2-Input AND Gate

MC74HC1G08

The MC74HC1G08 is a high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G08 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: $t_{PD} = 7$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity
- Balanced Propagation Delays ($t_{pLH} = t_{pHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL} = 2$ mA)
- Chip Complexity: < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

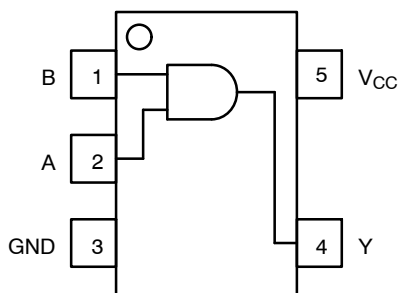


Figure 1. Pinout

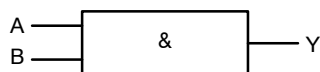


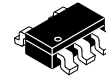
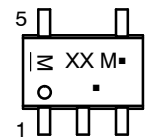
Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	B
2	A
3	GND
4	Y
5	V_{CC}

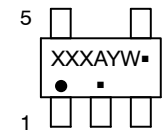
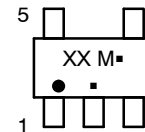


SC-88A
DF SUFFIX
CASE 419A

MARKING DIAGRAMS



TSOP-5
DT SUFFIX
CASE 483



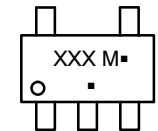
XX = Device Code
M = Date Code*
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.



SC-74A
DBV SUFFIX
CASE 318BQ



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

MC74HC1G08**MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit	
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V	
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V	
I_{IK}	DC Input Diode Current	± 20	mA	
I_{OK}	DC Output Diode Current	± 20	mA	
I_{OUT}	DC Output Source/Sink Current	± 12.5	mA	
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 25	mA	
T_{STG}	Storage Temperature Range	-65 to +150	°C	
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T_J	Junction Temperature Under Bias	+150	°C	
θ_{JA}	Thermal Resistance (Note 1)	SC-88A SC-74A	377 320	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC-88A SC-74A	332 390	mW
MSL	Moisture Sensitivity	Level 1		
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)	± 100	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow per JESD51-7.
2. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

MC74HC1G08**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	6.0	V
V _{IN}	DC Input Voltage	0.0	V _{CC}	V
V _{OUT}	DC Output Voltage	0.0	V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time			ns/V
		V _{CC} = 2.0 V	0	20
		V _{CC} = 2.3 V to 2.7 V	0	20
		V _{CC} = 3.0 V to 3.6 V	0	10
		V _{CC} = 4.5 V to 6.0 V	0	5

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

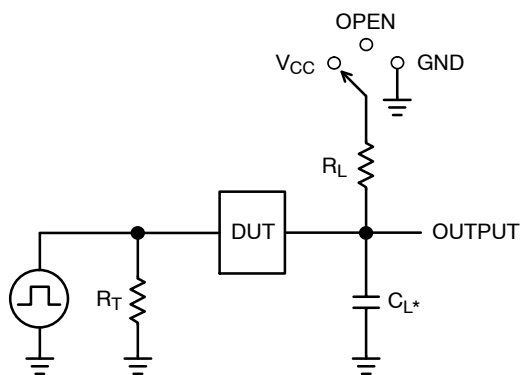
Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
V _{IH}	High-Level Input Voltage		2.0	1.5	-	-	1.5	-	1.5	-	V	
			3.0	2.1	-	-	2.1	-	2.1	-		
			4.5	3.15	-	-	3.15	-	3.15	-		
			6.0	4.20	-	-	4.20	-	4.20	-		
V _{IL}	Low-Level Input Voltage		2.0	-	-	0.5	-	0.5	-	0.5	V	
			3.0	-	-	0.9	-	0.9	-	0.9		
			4.5	-	-	1.35	-	1.35	-	1.35		
			6.0	-	-	1.80	-	1.80	-	1.80		
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -20 μA	2.0	1.9	2.0	-	1.9	-	1.9	-	V	
			3.0	2.9	3.0	-	2.9	-	2.9	-		
			4.5	4.4	4.5	-	4.4	-	4.4	-		
			6.0	5.9	6.0	-	5.9	-	5.9	-		
		4.5	I _{OH} = -2 mA I _{OH} = -2.6 mA	4.5	4.18	4.31	-	4.13	-	4.08		-
				6.0	5.68	5.80	-	5.63	-	5.58		-
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 20 μA	2.0	-	0.0	0.1	-	0.1	-	0.1	V	
			3.0	-	0.0	0.1	-	0.1	-	0.1		
			4.5	-	0.0	0.1	-	0.1	-	0.1		
			6.0	-	0.0	0.1	-	0.1	-	0.1		
		4.5	I _{OL} = 2 mA I _{OL} = 2.6 mA	4.5	-	0.17	0.26	-	0.33	-		0.40
				6.0	-	0.18	0.26	-	0.33	-		0.40
I _{IN}	Input Leakage Current	V _{IN} = 6.0 V or GND	6.0	-	-	±0.1	-	±1.0	-	±1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	6.0	-	-	1.0	-	10	-	40	μA	

MC74HC1G08**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, (A or B) to Y	V _{CC} = 5.0 V C _L = 15 pF	-	3.5	15	-	20	-	25	ns
		V _{CC} = 2.0 V C _L = 50 pF	-	20	100	-	125	-	155	
		V _{CC} = 3.0 V	-	11	27	-	35	-	90	
		V _{CC} = 4.5 V	-	8	20	-	25	-	35	
		V _{CC} = 6.0 V	-	7	17	-	21	-	26	
t _{TLH} , t _{THL}	Output Transition Time	V _{CC} = 5.0 V C _L = 15 pF	-	3	10	-	15	-	20	ns
		V _{CC} = 2.0 V C _L = 50 pF	-	25	125	-	155	-	200	
		V _{CC} = 3.0 V	-	16	35	-	45	-	60	
		V _{CC} = 4.5 V	-	11	25	-	31	-	38	
		V _{CC} = 6.0 V	-	9	21	-	26	-	32	
C _{IN}	Input Capacitance		-	5	10	-	10	-	10	pF
C _{PD}	Power Dissipation Capacitance (Note 4)	Typical @ 25°C, V_{CC} = 5.0 V								pF
		10								

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74HC1G08



*CL includes probe and jig capacitance
 RT is ZOUT of pulse generator (typically 50 W)
 f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	CL, pF	RL, Ω
tPLH / tPHL	Open	See AC Characteristics Table	X
tTLH / tTHL (Note 5)	Open		X
tPLZ / tPZL	VCC		1 k
tPHZ / tPZH	GND		1 k

X - Don't Care

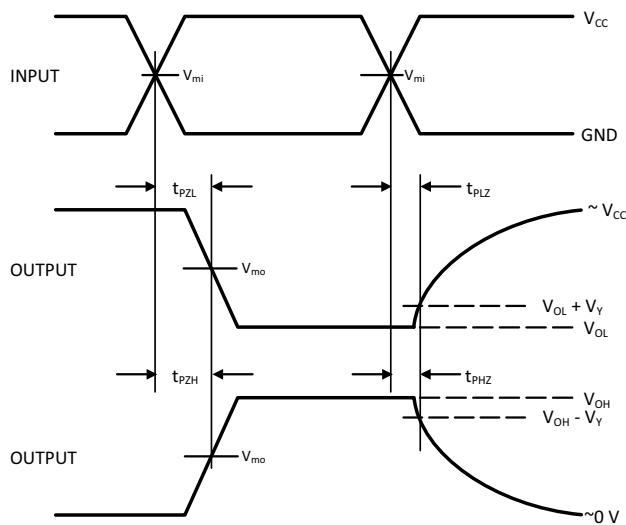
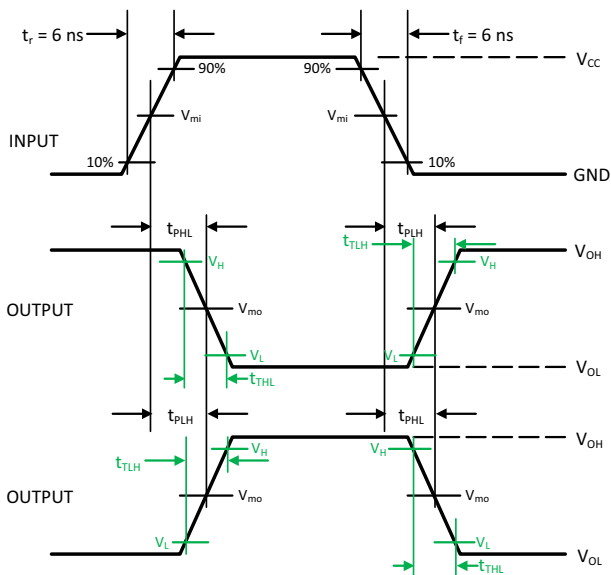


Figure 4. Switching Waveforms

VCC, V	Vmi, V	Vmo, V		VL, V	VH, V	VY, V
		tPLH, tPHL	tPZL, tPLZ, tPZH, tPHZ			
3.0 to 3.6	VCC/2	VCC/2	VCC/2	VOL + 0.1 (VOH - VOL)	VOL + 0.9 (VOH - VOL)	0.3
4.5 to 5.5	VCC/2	VCC/2	VCC/2	VOL + 0.1 (VOH - VOL)	VOL + 0.9 (VOH - VOL)	0.3

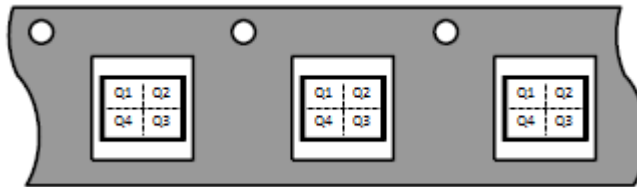
5. tTLH and tTHL are measured from 10% to 90% of (VOH - VOL), and 90% to 10% of (VOH - VOL), respectively.

MC74HC1G08**ORDERING INFORMATION**

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
MC74HC1G08DFT1G	SC-88A	H2	Q2	3000 / Tape & Reel
MC74HC1G08DFT1G-Q*	SC-88A	H2	Q2	3000 / Tape & Reel
MC74HC1G08DFT2G	SC-88A	H2	Q4	3000 / Tape & Reel
MC74HC1G08DFT2G-Q*	SC-88A	H2	Q4	3000 / Tape & Reel
MC74HC1G08DBVT1G	SC-74A	H2	Q4	3000 / Tape & Reel
MC74HC1G08DBVT1G-Q*	SC-74A	H2	Q4	3000 / Tape & Reel

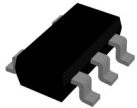
[†]For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel**Direction of Feed**

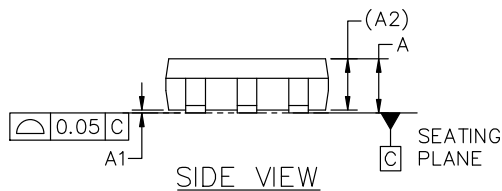
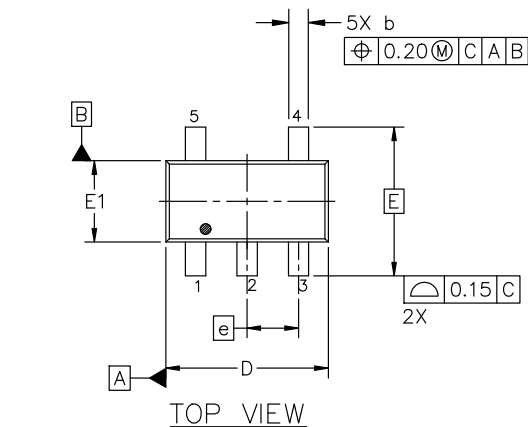


**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



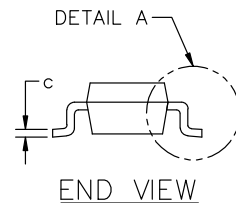
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CASE 318BQ
ISSUE C

DATE 26 FEB 2024

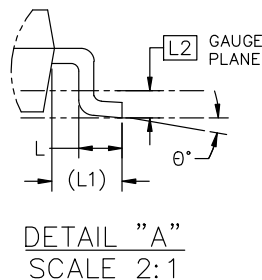


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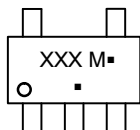
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.01	0.18	0.10
A2	0.95 REF.		
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D	2.85	3.00	3.15
E	2.75 BSC		
E1	1.35	1.50	1.65
e	0.95 BSC		
L	0.20	0.40	0.60
L1	0.62 REF.		
L2	0.25 BSC		
θ	0°	5°	10°



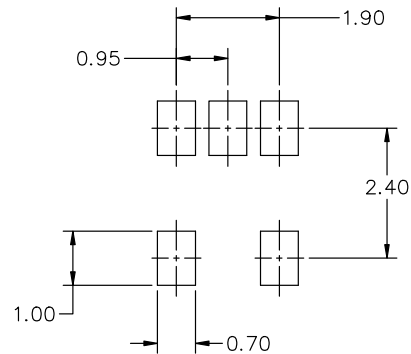
GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	SC-74A-5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

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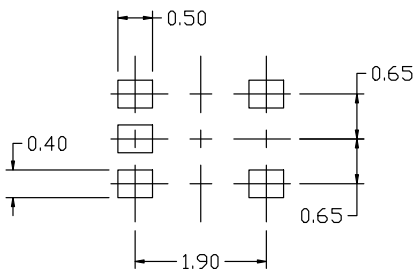
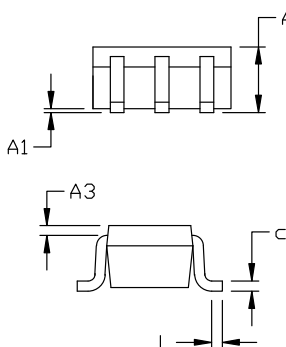
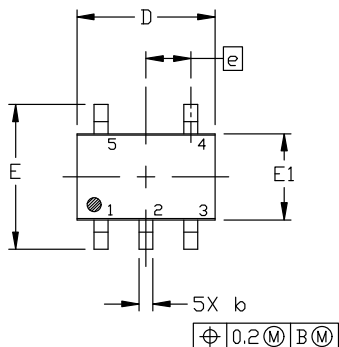
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

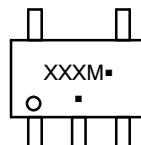
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

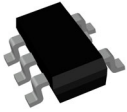
Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

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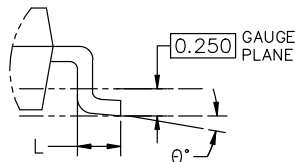
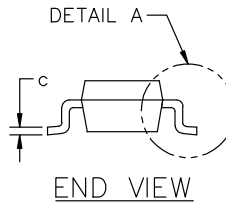
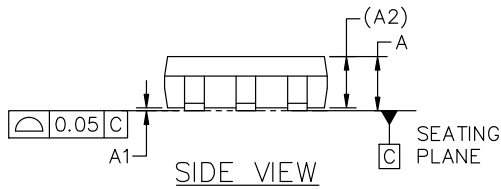
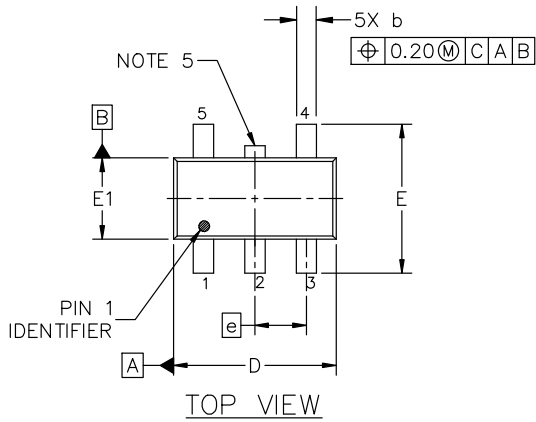


**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



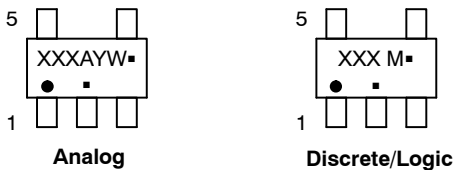
TSOP-5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024



DETAIL "A"
SCALE 2:1

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package
- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

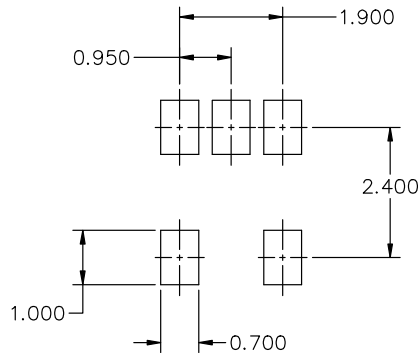
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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