

MC74LCX14DG Datasheet



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DiGi Electronics Part Number MC74LCX14DG-DG

Manufacturer onsemi

Manufacturer Product Number MC74LCX14DG

Description IC INVERT SCHMITT 6CH 1IN 14SOIC

Detailed Description Inverter IC 6 Channel Schmitt Trigger 14-SOIC



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DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MC74LCX14DG	onsemi
Series:	Product Status:
74LCX	Active
Logic Type:	Number of Circuits:
Inverter	6
Number of Inputs:	Features:
1	Schmitt Trigger
Voltage - Supply:	Current - Quiescent (Max):
2V ~ 3.6V	10 μΑ
Current - Output High, Low:	Input Logic Level - Low:
24mA, 24mA	0.4V ~ 0.6V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.7V ~ 2.2V	6.5ns @ 3.3V, 50pF
Operating Temperature:	Mounting Type:
-40°C ~ 85°C	Surface Mount
Supplier Device Package:	Package / Case:
14-SOIC	14-SOIC (0.154", 3.90mm Width)
Base Product Number:	
74LCX14	

Environmental & Export classification

8542.39.0001

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

ONSEM1,

www.onsemi.com

Low Voltage CMOS Hex Schmitt Inverter with 5 V-Tolerant Inputs

MC74LCX14

The MC74LCX14 is a high performance hex inverter with Schmitt–Trigger inputs operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers, while TTL compatible outputs offer improved switching noise performance. A $V_{\rm I}$ specification of 5.5 V allows MC74LCX14 inputs to be safely driven from 5.0 V devices.

Pin configuration and function are the same as the MC74LCX04, but the inputs have hysteresis and, with its Schmitt trigger function, the LCX14 can be used as a line receiver which will receive slow input signals.

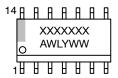
Features

- \bullet Designed for 1.65 V to 5.5 V V_{CC} Operation
- 5.0 V Tolerant Inputs Interface Capability with 5.0 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- Current Drive Capability is 24 mA at Source/Sink
- Pin and Function Compatible with Other Standard Logic Families
- ESD Performance: Human Body Model >2000 V
- Chip Complexity: 41 Equivalent Gates
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



XXXXXX = Specific Device Code
A = Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

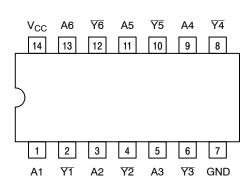


Figure 1. Pinout: 14-Lead (Top View)

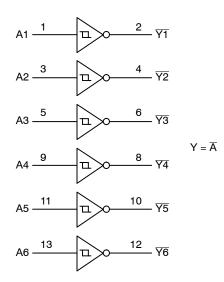


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
An	Data Inputs
₹n	Outputs

TRUTH TABLE

Inputs	Outputs
Α	Υ
L	Н
Н	L

MAXIMUM RATINGS

Symbol	Parame	ter	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
VI	DC Input Voltage (Note 1)		-0.5 to +6.5	V
Vo	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I _{IK}	DC Input Diode Current	$V_I < GND$	-50	mA
lok	DC Output Diode Current	V _O < GND	-50	mA
Ιο	DC Output Source/Sink Current		±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground	d Pin	±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 s	secs	260	°C
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150	°C/W
P _D	Power Dissipation in Still Air at 125°C	SOIC-14 QFN14 TSSOP-14	1077 962 833	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. I_O absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol		Parameter			Max	Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	3.3	5.5	V
VI	Digital Input Voltage		0	-	5.5	V
Vo	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V _{CC} = 0 V)	0 0 0	- - -	V _{CC} 5.5 5.5	V
T _A	Operating Free-Air Temperature		-40	-	+125	°C
t _r , t _f	Input Transition Rise or Fall Rate		0	_	No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

				T _A = -40°C	C to +85°C	T _A = -40°C	to +125°C	
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Min	Max	Unit
V_{T+}	Positive-Input Threshold		1.65	-	1.4	-	1.4	V
	Voltage		2.5	0.9	1.7	0.9	1.7	
			3.0	1.2	2.2	1.2	2.2	
			4.5	-	3.1	-	3.1	
			5.5	-	3.6	_	3.6	
V_{T-}	Negative-Input Threshold		1.65	0.2	-	0.2	-	V
	Voltage		2.5	0.4	1.1	0.4	1.1	
			3.0	0.6	1.5	0.6	1.5	
			4.5	1	-	1	-	
			5.5	1.2	-	1.2	-	
V _H	Hysteresis Voltage		1.65	0.1	0.9	0.1	0.9	V
			2.5	0.3	1.0	0.3	1.0	
			3.0	0.4	1.2	0.4	1.2	
			4.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.7	0.7	1.7	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}						V
		I _{OH} = -100 μA	1.65 to 5.5	V _{CC} – 0.1	-	V _{CC} – 0.1	_	
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	1.65 2.3	1.29 1.8	_	1.29 1.8	_	
		$I_{OH} = -12 \text{ mA}$	2.7	2.2	_	2.2	_	
		I _{OH} = -16 mA	3.0	2.4	_	2.4	_	
		I _{OH} = -24 mA	3.0	2.2	_	2.2	_	
		I _{OH} = -32 mA	4.5	3.7	-	3.7	-	
V _{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ or V_{IL}						V
		I _{OL} = 100 μA	1.65 to 5.5	_	0.1	-	0.1	
		$I_{OL} = 4 \text{ mA}$	1.65	_	0.24	-	0.24	
		$I_{OL} = 8 \text{ mA}$	2.3	_	0.3	-	0.3	
		I _{OL} = 12 mA	2.7	_	0.4	-	0.4	
		I _{OL} = 16 mA	3.0	_	0.4	_	0.4	
		I _{OL} = 24 mA	3.0	_	0.55	-	0.55	
		I _{OL} = 32 mA	4.5	_	0.6	-	0.6	
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	-	±5.0	-	±5.0	μΑ
I _{OFF}	Power Off Leakage Current	$V_{I} = 5.5 \text{ V or}$ $V_{O} = 5.5 \text{ V}$	0	-	10	_	10	μΑ
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	_	10	_	10	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6 V	2.3 to 3.6	-	500	-	500	μΑ
	·							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

				T _A = -40°C	C to +85°C	T _A = -40°C	to +125°C	
Symbol	Parameter	Test Condition	V _{CC} (V)	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 3 and 4	1.65 to 1.95	-	15.7	-	15.7	ns
			2.3 to 2.7	1.5	7.8	1.5	7.8	
			2.7	1.5	7.5	1.5	7.5	
			3.0 to 3.6	1.5	6.5	1.5	6.5	
			4.5 to 5.5	-	5.6	-	5.6	
toshL, toslh	Output to Output Skew		1.65 to 1.95	-	-	-	-	ns
			2.3 to 2.7	_	_	_	-	
			2.7	-	_	-	-	
			3.0 to 3.6	-	1.0	-	1.0	
			4.5 to 5.5	_	_	_	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC SWITCHING CHARACTERISTICS

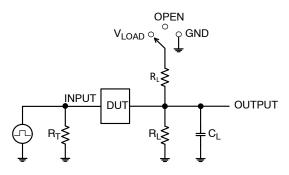
			T _A = +25°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 5)	$\begin{aligned} &V_{CC} = 3.3 \text{ V, } C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V} \\ &V_{CC} = 2.5 \text{ V, } C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V} \end{aligned}$		0.8 0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 5)	$\begin{aligned} &V_{CC} = 3.3 \text{ V, } C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V} \\ &V_{CC} = 2.5 \text{ V, } C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V} \end{aligned}$		-0.8 -0.6		V

^{5.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T _A = 25°C)	Unit
C _{IN}	Input Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	8	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	25	pF

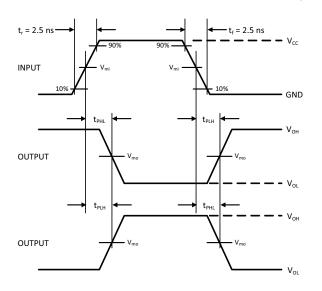
^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

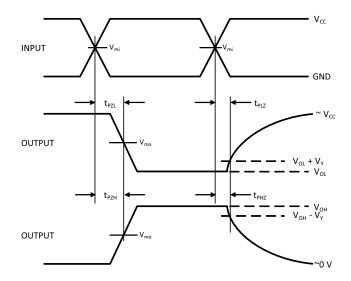


Test	Switch Position
t _{PLH} / t _{PHL}	Open
t _{PLZ} / t _{PZL}	V_{LOAD}
t _{PHZ} / t _{PZH}	GND

 C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 $\Omega)$ f = 1 MHz

Figure 3. Test Circuit





V _{CC} , V	R_L,Ω	C _L , pF	V _{LOAD}	V _m , V	V _Y , V
1.65 to 1.95	500	30	2 x V _{CC}	V _{CC} /2	0.15
2.3 to 2.7	500	30	2 x V _{CC}	V _{CC} /2	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	2 x V _{CC}	V _{CC} /2	0.3

Figure 4. Switching Waveforms

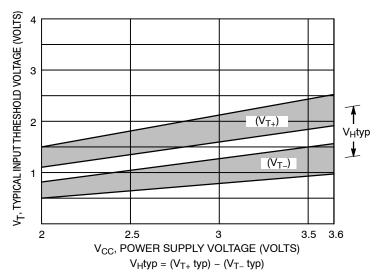


Figure 5. Typical Input Threshold, V_{T_+} , V_{T_-} versus Power Supply Voltage

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



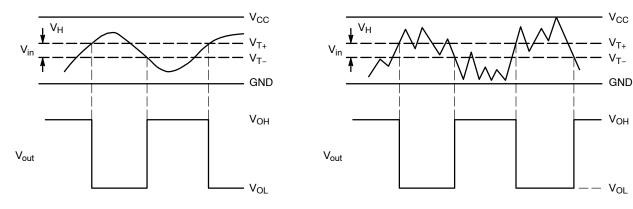


Figure 6. Typical Schmitt-Trigger Applications

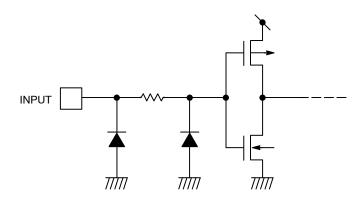


Figure 7. Input Equivalent Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74LCX14DG	LCX14G	SOIC-14	55 Units / Rail
MC74LCX14DR2G	LCX14G	SOIC-14	2500 / Tape & Reel
MC74LCX14DTG	LCX 14	TSSOP-14	96 Units / Rail
MC74LCX14DTR2G	LCX 14	TSSOP-14	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



MECHANICAL CASE OUTLINE

NOTES:
1. DIMENSIONING AND TOLERANCING PER

5. MAXIMUM MOLD PROTRUSION 0.15 PER

MILLIMETERS

MIN MAX

1.27 BSC

0.19

0.25

0.40

SIDE

Α

A1 0.10

АЗ

b 0.35

D E 8.55

e H h

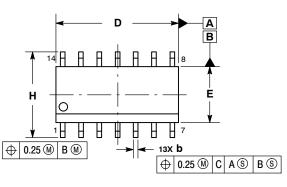
ASME Y14.5M, 1994.
CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

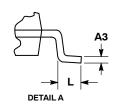
PACKAGE DIMENSIONS

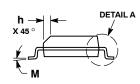


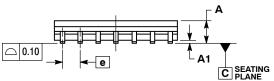
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016









GENERIC MARKING DIAGRAM*

INCHES

MIN MAX

0.050 BSC

0.068

0.019

0.054

0.25 | 0.004 | 0.010

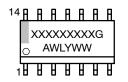
0.25 0.008 0.010

0.50 0.010 0.019

1.25 0.016 0.049

0.49 0.014

8.75 0.337 3.80 4.00 0.150 0.157



XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year = Work Week WW = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT* - 6.50 14X 1 18 1.27 **PITCH** 14X 0.58

DIMENSIONS: MILLIMETERS

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-14 NB		PAGE 1 OF 2	

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 6. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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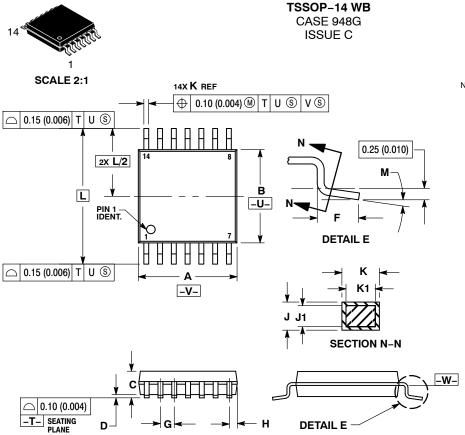
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

DATE 17 FEB 2016



- NOTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

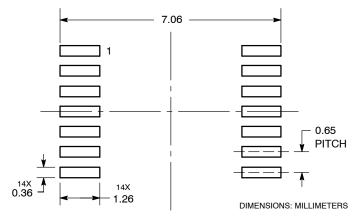
 3. DIMENSION A DOES NOT INCLUDE MOLD
- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR DEFERENCE ONLY
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	o°	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



= Assembly Location

= Wafer Lot = Year

= Work Week W

= Pb-Free Package (Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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