# MC74LVX14DTR2G Datasheet

www.digi-electronics.com
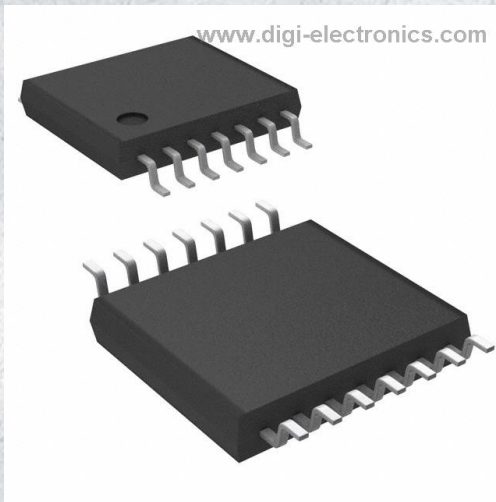
https://www.DiGi-Electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | MC74LVX14DTR2G-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | MC74LVX14DTR2G |
| Description | IC INVERTER 6CH 1-INP 14TSSOP |
| Detailed Description | Inverter IC 6 Channel Schmitt Trigger 14-TSSOP |

# Purchase and inquiry

| | |
|---|---|
| Manufacturer Product Number: | Manufacturer: |
| MC74LVX14DTR2G | onsemi |
| Series: | Product Status: |
| 74LVX | Active |
| Logic Type: | Number of Circuits: |
| Inverter | 6 |
| Number of Inputs: | Features: |
| 1 | Schmitt Trigger |
| Voltage - Supply: | Current - Quiescent (Max): |
| 2V ~ 3.6V | 2 µA |
| Current - Output High, Low: | Input Logic Level - Low: |
| 4mA, 4mA | 0.9V |
| Input Logic Level - High: | Max Propagation Delay @ V, Max CL: |
| 2.2V | 14.1ns @ 3.3V, 50pF |
| Operating Temperature: | Mounting Type: |
| -40°C ~ 85°C | Surface Mount |
| Supplier Device Package: | Package / Case: |
| 14-TSSOP | 14-TSSOP (0.173", 4.40mm Width) |
| Base Product Number: | |
| 74LVX14 | |

# Environmental & Export classification

| | |
|---|---|
| RoHS Status: | Moisture Sensitivity Level (MSL): |
| ROHS3 Compliant | 1  (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

**onsemi**

# Hex Schmitt Inverter
## With 5 V−Tolerant Inputs

## MC74LVX14

The MC74LVX14 is an advanced high speed CMOS Schmitt inverter. The inputs tolerate voltages up to 6.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74LVX14 is pin and functionally compatible to the MC74LVX04, but the inputs have hysteresis and, with its Schmitt trigger function, can be used as a line receiver which will receive slow input signals.

**Features**

- High Speed: $t_{PD}$ = 6.8 ns (Typ) at $V_{CC}$ = 3.3 V
- Low Power Dissipation: $I_{CC}$ = 2 μA (Max) at $T_A$ = 25°C
- Powerdown Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP}$ = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:  Human Body Model > 2000 V
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
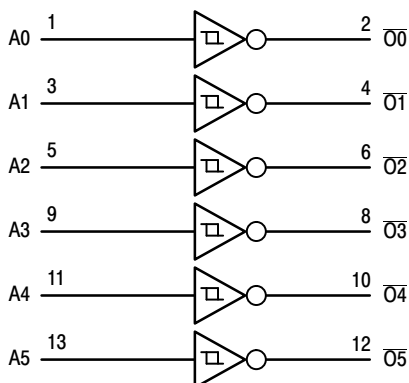- These Devices are Pb−Free and are RoHS Compliant

**SOIC−14 NB**
**D SUFFIX**
**CASE 751A**

**TSSOP−14**
**DT SUFFIX**
**CASE 948G**

### PIN ASSIGNMENT

| $V_{CC}$ | A5 | $\overline{O5}$ | A4 | $\overline{O4}$ | A3 | $\overline{O3}$ |
|----|----|----|----|----|----|----|
| 14 | 13 | 12 | 11 | 10 | 9 | 8 |

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|
| A0 | $\overline{O0}$ | A1 | $\overline{O1}$ | A2 | $\overline{O2}$ | GND |
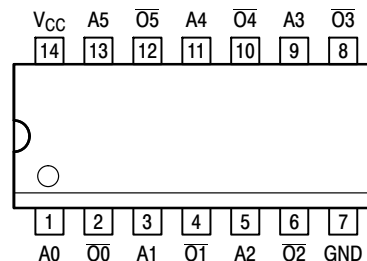
**14−Lead** (Top View)

### MARKING DIAGRAMS

14
XXXXXXG
AWLYWW
1

**SOIC−14 NB**

14
XXX
XXX
ALYW■
1
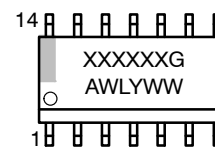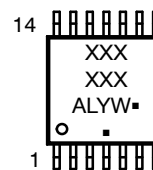
**TSSOP−14**

| XXX | = Specific Device Code |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G or ■ | = Pb−Free Package |

(Note: Microdot may be in either location)



**Figure 1. Logic Diagram**

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

**PIN NAMES**

| Pins | Function |
|---|---|
| An <br> $\overline{On}$ | Data Inputs <br> Data Outputs |

**FUNCTION TABLE**

| An | $\overline{On}$ |
|---|---|
| L | H |
| H | L |

# MC74LVX14

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{in}$ | DC Input Voltage | | −0.5 to +6.5 | V |
| $V_{out}$ | DC Output Voltage | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±50 | mA |
| $P_D$ | Power Dissipation | SOIC TSSOP | 1077 833 | mW |
| $T_{stg}$ | Storage Temperature | | −65 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 2.0 | 3.6 | V |
| $V_{in}$ | DC Input Voltage | 0 | 5.5 | V |
| $V_{out}$ | DC Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | −40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $T_A$ = 25°C | | | $T_A$ = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{T+}$ | Positive Threshold Voltage (Figure 4) | | 3.0 | | | 2.20 | | 2.20 | V |
| $V_{T−}$ | Negative Threshold Voltage (Figure 4) | | 3.0 | 0.90 | | | 0.90 | | V |
| $V_H$ | Hysteresis Voltage (Figure 4) | | 3.0 | 0.30 | | 1.20 | 0.30 | 1.20 | V |
| $V_{OH}$ | High−Level Output Voltage ($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OH}$ = −50 μA $I_{OH}$ = −50 μA $I_{OH}$ = −4 mA | 2.0 3.0 3.0 | 1.9 2.9 2.58 | 2.0 3.0 | | 1.9 2.9 2.48 | | V |
| $V_{OL}$ | Low−Level Output Voltage ($V_{in}$ = $V_{IH}$ or $V_{IL}$) | $I_{OL}$ = 50 μA $I_{OL}$ = 50 μA $I_{OL}$ = 4 mA | 2.0 3.0 3.0 | | 0.0 0.0 | 0.1 0.1 0.36 | | 0.1 0.1 0.44 | V |
| $I_{in}$ | Input Leakage Current | $V_{in}$ = 5.5 V or GND | 3.6 | | | ±0.1 | | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{in}$ = $V_{CC}$ or GND | 3.6 | | | 2.0 | | 20.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0 ns)

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C | | | $T_A$ = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, Input−to−Output | $V_{CC}$ = 2.7 V    $C_L$ = 15 pF          $C_L$ = 50 pF | | 8.7 11.2 | 16.3 19.8 | 1.0 1.0 | 19.5 23.0 | ns |
| | | $V_{CC}$ = 3.3 ± 0.3 V    $C_L$ = 15 pF          $C_L$ = 50 pF | | 6.8 9.3 | 10.6 14.1 | 1.0 1.0 | 12.5 16.0 | |
| $t_{OSHL}$ $t_{OSLH}$ | Output−to−Output Skew (Note 1) | $V_{CC}$ = 2.7 V    $C_L$ = 50 pF $V_{CC}$ = 3.3 ± 0.3 V    $C_L$ = 50 pF | | | 1.5 1.5 | | 1.5 1.5 | ns |

# MC74LVX14

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW ($t_{OSHL}$) or LOW–to–HIGH ($t_{OSLH}$); parameter guaranteed by design.
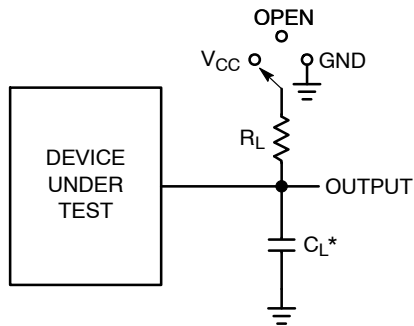
## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | $T_A = 25°C$ | | | $T_A = -40$ to $85°C$ | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| Cin | Input Capacitance | | 4 | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 2) | | 21 | | | | pF |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). $C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

| Symbol | Characteristic | $T_A = 25°C$ | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.3 | 0.5 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.3 | −0.5 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.9 | V |

# MC74LVX14

OPEN

$V_{CC}$  GND

$R_L$

DEVICE
UNDER
TEST

OUTPUT

$C_L$*

*$C_L$ Includes probe and jig capacitance

| Test | Switch Position | $C_L$ | $R_L$ |
|------|-----------------|-------|-------|
| $t_{PLH}$ / $t_{PHL}$ | Open | See AC Charac-terisitcs Table | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

**Figure 2. Test Circuit**

$t_r$ = 6 ns

$t_f$ = 6 ns

$V_{IN}$

90%          90%

INPUT          $V_m$          $V_m$

10%          10%

GND

$t_{PHL}$          $t_{PLH}$

$V_{OH}$

OUTPUT          $V_m$          $V_m$

$V_{OL}$

$t_{PLH}$          $t_{PHL}$

$V_{OH}$

90%          90%

OUTPUT          $V_m$          $V_m$

10%          $t_{TLH}$          $t_{THL}$

$V_{OL}$

$V_{IN}$

INPUT          $V_m$          $V_m$

GND

$t_{PZL}$          $t_{PLZ}$

High Impedance

OUTPUT          $V_m$

10%          $V_{OL}$

$t_{PZH}$          $t_{PHZ}$

$V_{OH}$

90%

OUTPUT          $V_m$

High Impedance
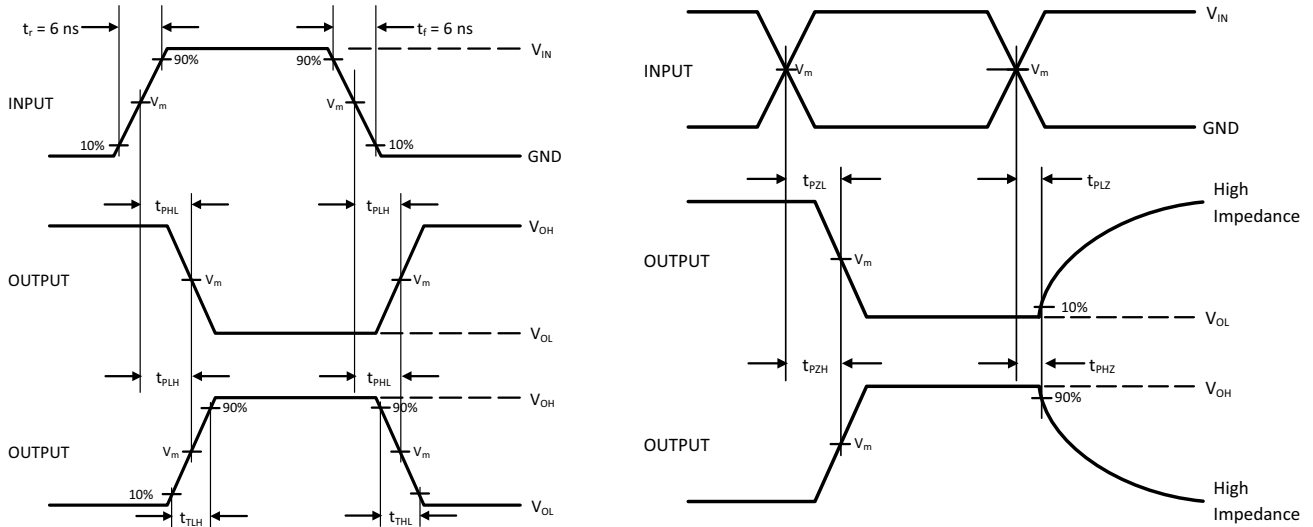
| Device | $V_{IN}$, V | $V_m$, V |
|--------|-------------|----------|
| MC74LVX14 | $V_{CC}$ | 50% x $V_{CC}$ |

**Figure 3. Switching Waveforms**
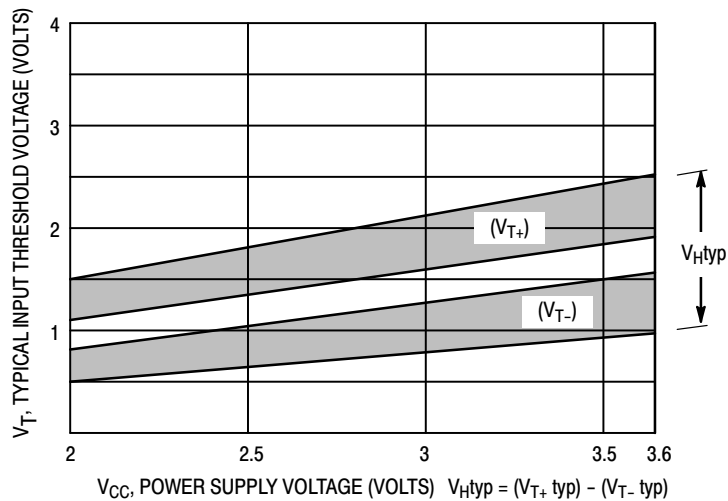
**Figure 4. Typical Input Threshold, $V_{T+}$, $V_{T-}$ versus Power Supply Voltage**
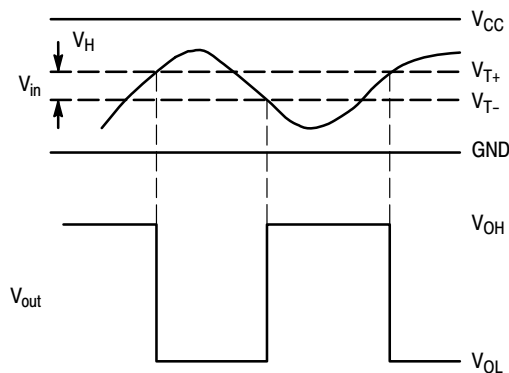


(a) A Schmitt–Trigger Squares Up Inputs With Slow Rise and Fall Times
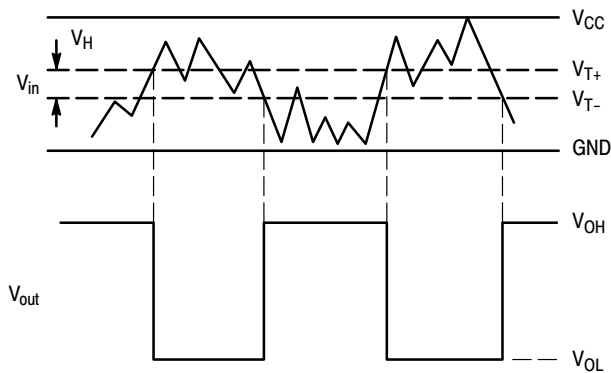


(b) A Schmitt–Trigger Offers Maximum Noise Immunity

**Figure 5. Typical Schmitt–Trigger Applications**

# MC74LVX14

**ORDERING INFORMATION**

| Device | Marking | Package | Shipping$^\dagger$ |
|---|---|---|---|
| MC74LVX14DR2G | LVX14 | SOIC−14 | 2500 Tape & Reel |
| MC74LVX14DTR2G | LVX 14 | TSSOP−14 | 2500 Tape & Reel |
| MC74LVX14DTR2G−Q* | LVX 14 | TSSOP−14 | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS
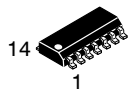
**SOIC−14 NB**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14
1
**SCALE 1:1**
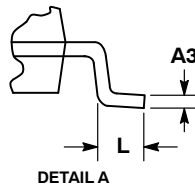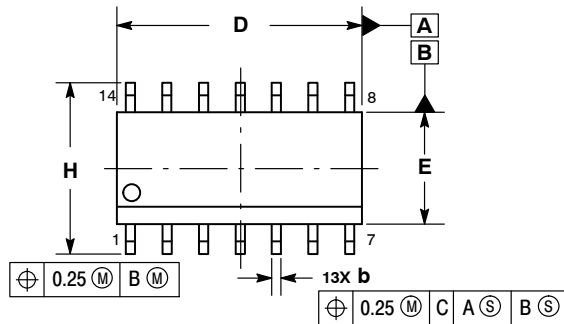
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

**DETAIL A**

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
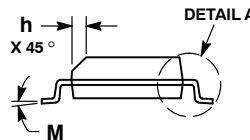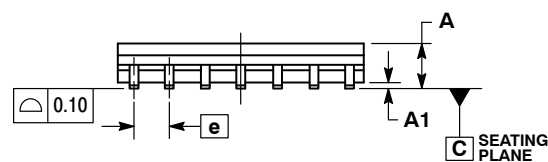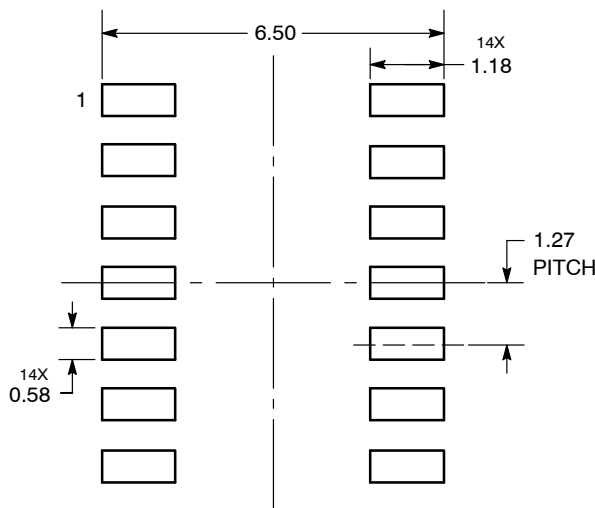
13X b
⊕ 0.25 (M) B (M)
⊕ 0.25 (M) C A (S) B (S)

△ 0.10

**SEATING PLANE**

X 45 °
**DETAIL A**

## SOLDERING FOOTPRINT*

6.50
14X
1.18
1

1.27
PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

## GENERIC
## MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1
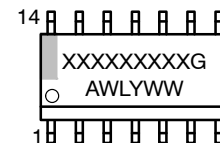
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

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|---|---|---|---|
| DESCRIPTION: | SOIC−14 NB | | PAGE 1 OF 2 |

**SOIC−14**
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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|---|---|---|---|
| DESCRIPTION: | SOIC−14 NB | | PAGE 2 OF 2 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−14 WB**
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

◯ | 0.15 (0.006) | T U Ⓢ

2X **L/2**

**L**

PIN 1 IDENT.

◯ | 0.15 (0.006) | T U Ⓢ

**A**
−V−

14    8

**B**
−U−

1    7

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

**K**

**K1**

**J  J1**

**SECTION N−N**

**C**

◯ | 0.10 (0.004)

−T−  SEATING PLANE

**D**    **G**    **H**

**DETAIL E**

−W−
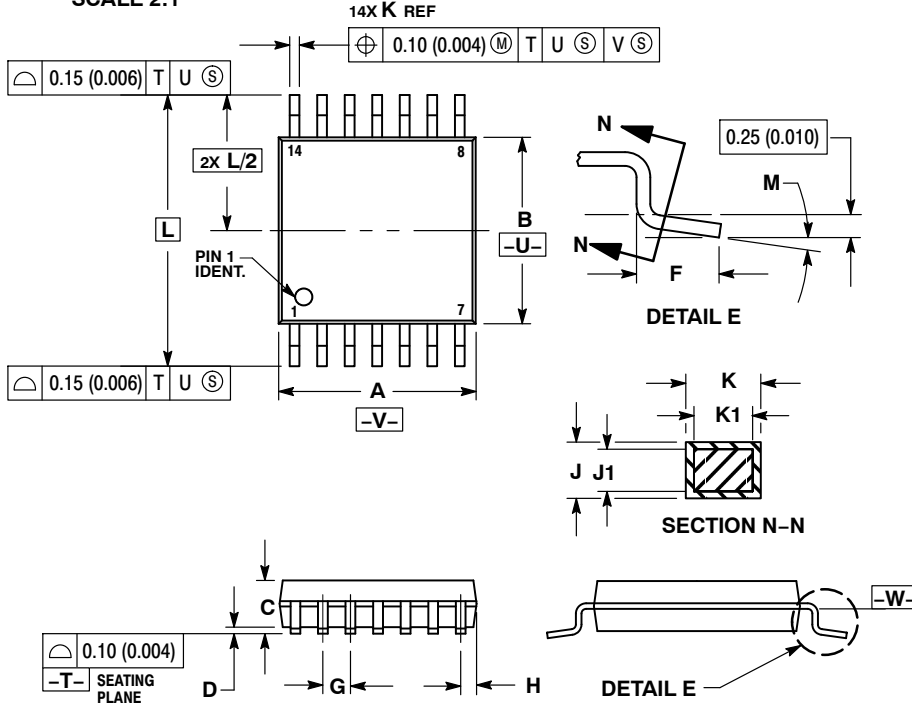
**NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|-------|-------|
|     | MIN  | MAX  | MIN   | MAX   |
| A   | 4.90 | 5.10 | 0.193 | 0.200 |
| B   | 4.30 | 4.50 | 0.169 | 0.177 |
| C   | ---  | 1.20 | ---   | 0.047 |
| D   | 0.05 | 0.15 | 0.002 | 0.006 |
| F   | 0.50 | 0.75 | 0.020 | 0.030 |
| G   | 0.65 BSC | | 0.026 BSC | |
| H   | 0.50 | 0.60 | 0.020 | 0.024 |
| J   | 0.09 | 0.20 | 0.004 | 0.008 |
| J1  | 0.09 | 0.16 | 0.004 | 0.006 |
| K   | 0.19 | 0.30 | 0.007 | 0.012 |
| K1  | 0.19 | 0.25 | 0.007 | 0.010 |
| L   | 6.40 BSC | | 0.252 BSC | |
| M   | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED SOLDERING FOOTPRINT*
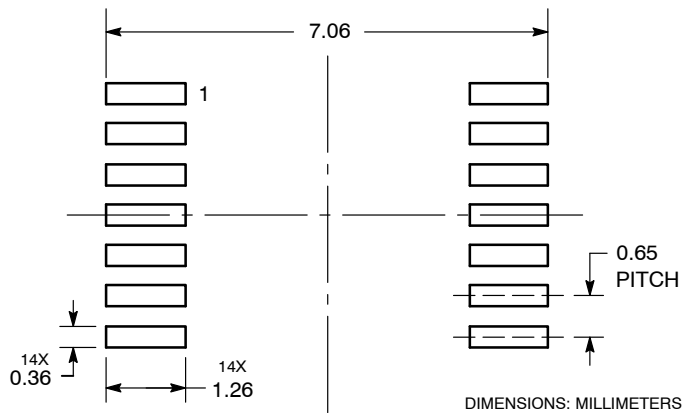
7.06

1

0.65 PITCH

14X 0.36

14X 1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*

14

XXXX
XXXX
ALYW■

1
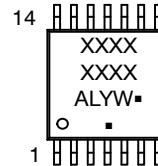
| A | = Assembly Location |
|---|---|
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ■ | = Pb−Free Package |

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|---|
| DESCRIPTION: | TSSOP−14 WB | | PAGE 1 OF 1 |

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# OUR CERTIFICATE

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