MC74LVXU04DG Datasheet

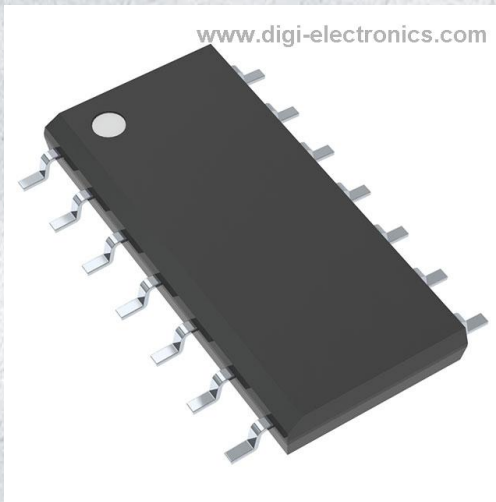www.digi-electronics.com

DiGi Electronics Part Number	MC74LVXU04DG-DG
Manufacturer	onsemi
Manufacturer Product Number	MC74LVXU04DG
Description	IC INVERTER 6CH 1-INP 14SOIC
Detailed Description	Inverter IC 6 Channel 14-SOIC

https://www.DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	**Manufacturer:**
MC74LVXU04DG	onsemi
Series:	**Product Status:**
74LVXU	Obsolete
Logic Type:	**Number of Circuits:**
Inverter	6
Number of Inputs:	**Features:**
1	-
Voltage - Supply:	**Current - Quiescent (Max):**
2V ~ 3.6V	2 µA
Current - Output High, Low:	**Input Logic Level - Low:**
4mA, 4mA	0.5V ~ 0.8V
Input Logic Level - High:	**Max Propagation Delay @ V, Max CL:**
1.5V ~ 2.4V	9.7ns @ 3.3V, 50pF
Operating Temperature:	**Mounting Type:**
-40°C ~ 85°C	Surface Mount
Supplier Device Package:	**Package / Case:**
14-SOIC	14-SOIC (0.154", 3.90mm Width)
Base Product Number:	
74LVXU04	

Environmental & Export classification

RoHS Status:	**Moisture Sensitivity Level (MSL):**
ROHS3 Compliant	1 (Unlimited)
REACH Status:	**ECCN:**
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

onsemi

Hex Inverter
(Unbuffered)
MC74LVXU04

The MC74LVX04 is an advanced high speed CMOS unbuffered hex inverter. The inputs tolerate voltages up to 6.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 4.1 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 2 µA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
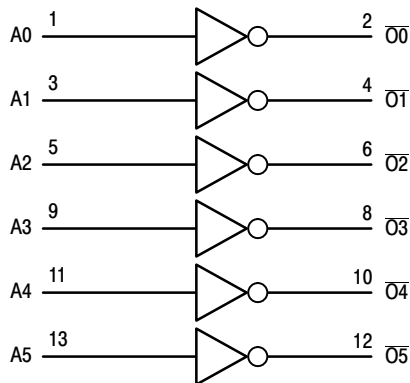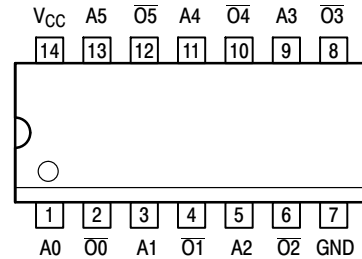- These Devices are Pb−Free and are RoHS Compliant

SOIC−14 NB
D SUFFIX
CASE 751A

TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

V_{CC}	A5	$\overline{O5}$	A4	$\overline{O4}$	A3	$\overline{O3}$
14	13	12	11	10	9	8

A0	$\overline{O0}$	A1	$\overline{O1}$	A2	$\overline{O2}$	GND
1	2	3	4	5	6	7

14−Lead (Top View)

A0 1 ▷ 2 $\overline{O0}$
A1 3 ▷ 4 $\overline{O1}$
A2 5 ▷ 6 $\overline{O2}$
A3 9 ▷ 8 $\overline{O3}$
A4 11 ▷ 10 $\overline{O4}$
A5 13 ▷ 12 $\overline{O5}$

Figure 1. Logic Diagram

MARKING DIAGRAMS

14
XXXXXXG
AWLYWW
1

SOIC−14 NB

14
XXX
XXX
ALYW■
1

TSSOP−14

XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb−Free Package

(Note: Microdot may be in either location)

PIN NAMES

Pins	Function
An	Data Inputs
$\overline{On}$	Outputs

FUNCTION TABLE

An	$\overline{On}$
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74LVXU04

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−20	mA
I_{OK}	DC Output Diode Current	V_O < GND	±20	mA
I_{OUT}	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP	116 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC TSSOP	1077 833	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94−V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Charged Device Model (Note 2)	> 2000 2000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 3)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A.
2. Tested to JESD22−C101−A.
3. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2.0	3.6	V
V_I	Input Voltage	(Note 4)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	V_{CC}	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 3.0 V ± 0.3 V	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

MC74LVXU04

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5 V or GND	3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Input to Output	V_{CC} = 2.7V	C_L = 15 pF C_L = 50 pF		5.4 7.9	10.1 13.6	1.0 1.0	12.5 16.0	ns
		V_{CC} = 3.3 ± 0.3V	C_L = 15 pF C_L = 50 pF		4.1 6.6	6.2 9.7	1.0 1.0	7.5 11.0	
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 5)	V_{CC} = 2.7V V_{CC} = 3.3 ±0.3V	C_L = 50 pF C_L = 50 pF			1.5 1.5		1.5 1.5	ns

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T_A = 25°C			T_A = −40 to 85°C		Unit
		Min	Typ	Max	Min	Max	
Cin	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 6)		18				pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = $C_{PD} \bullet V_{CC} \bullet f_{in}$ + $I_{CC}/6$ (per buffer). C_{PD} is used to determine the no−load dynamic power consumption; P_D = $C_{PD} \bullet V_{CC}^2 \bullet f_{in}$ + $I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 3.3 V, Measured in SOIC Package)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

MC74LVXU04

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		
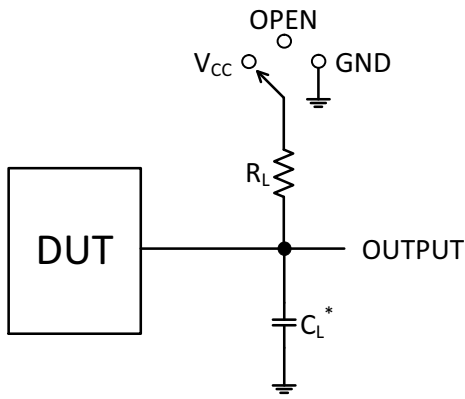
*C_L Includes probe and jig capacitance

Figure 2. Test Circuit
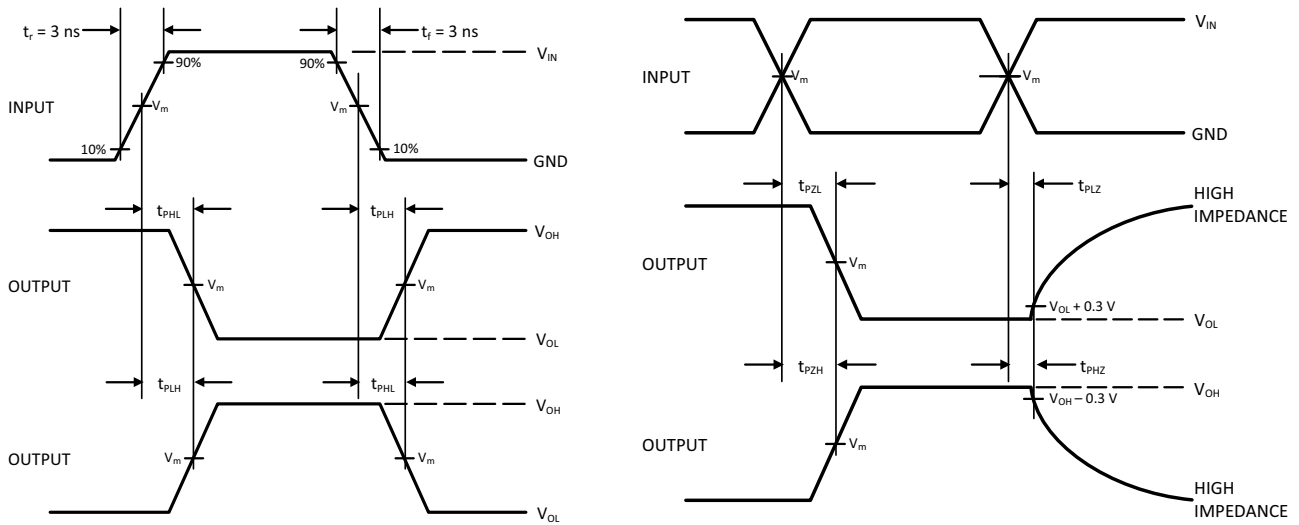
Device	V_{IN}, V	V_m, V
MC74LVXU04	V_{CC}	50% x V_{CC}

Figure 3. Switching Waveforms

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74LVXU04DR2G	LVXU04	SOIC−14 NB (Pb−Free)	2500 Tape & Reel
MC74LVXU04DTR2G	LVX U04	TSSOP−14 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14

1

SCALE 1:1
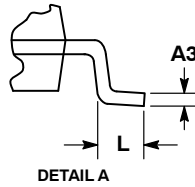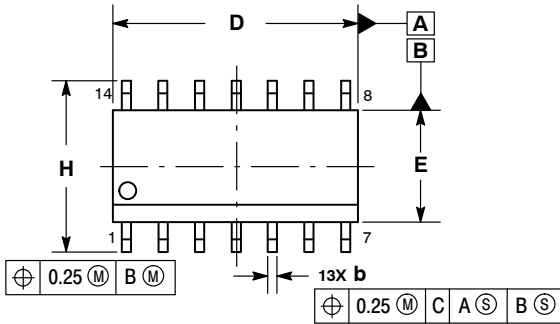
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DETAIL A

DETAIL A

X 45°

SEATING PLANE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°
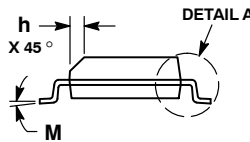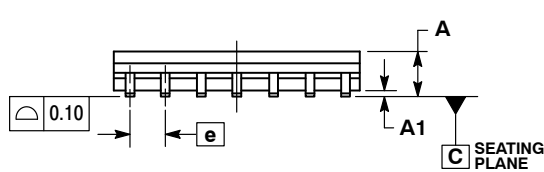
SOLDERING FOOTPRINT*
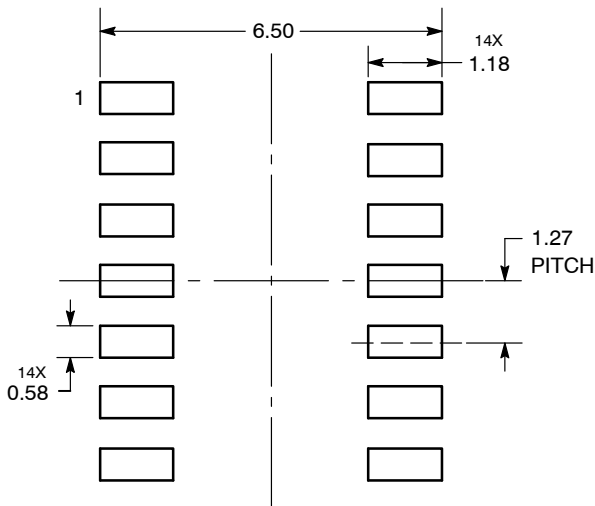
6.50

14X
1.18

1.27
PITCH

14X
0.58

1

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1
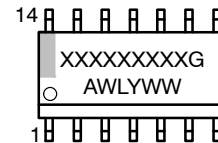
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

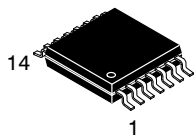| DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

onsemi

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

$\oplus$ | 0.10 (0.004) Ⓜ｜T U Ⓢ V Ⓢ

◯ | 0.15 (0.006) | T U Ⓢ

2X **L/2**

L

14

8

PIN 1 IDENT.

1

7

B
−U−

A
−V−

◯ | 0.15 (0.006) | T U Ⓢ

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1

SECTION N−N

C

◯ | 0.10 (0.004)
−T− SEATING PLANE

D

G

H

−W−

DETAIL E
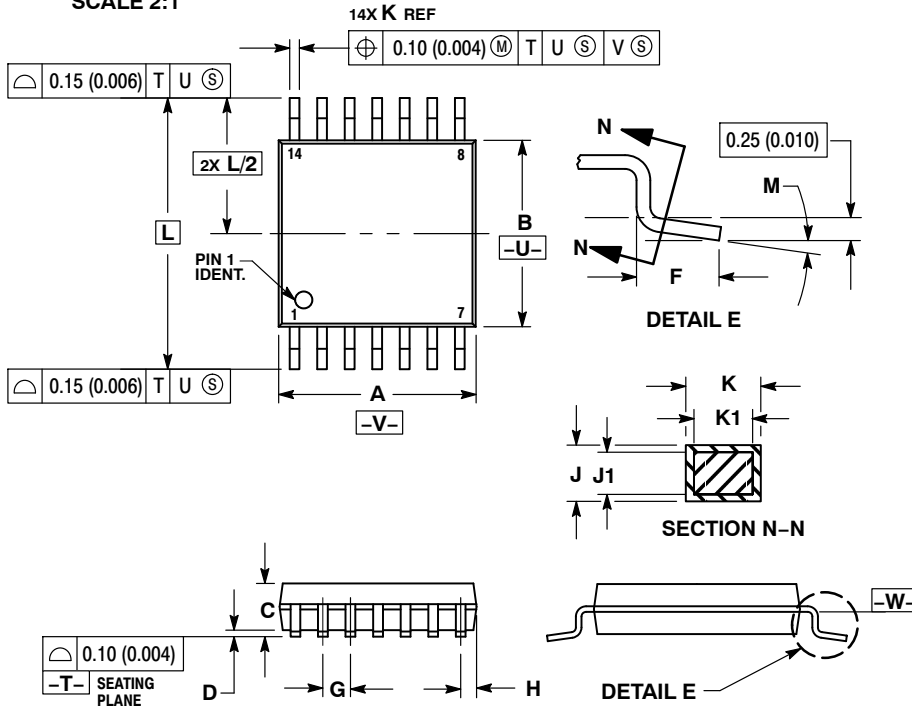
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED
SOLDERING FOOTPRINT*
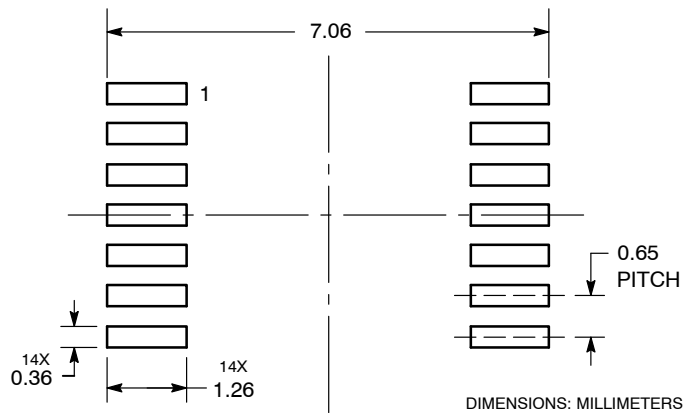
7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

14

XXXX
XXXX
ALYW▪

1
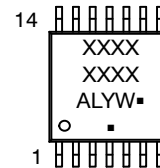
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−14 WB		PAGE 1 OF 1

ADDITIONAL INFORMATION

◊

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we striciy control the quality of products and services. Welcome your RFQ to Email: Info@DiGi-Electronics.com