

MC74VHC00DR2 Datasheet



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| | |
|------------------------------|--------------------------------|
| DiGi Electronics Part Number | MC74VHC00DR2-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | MC74VHC00DR2 |
| Description | IC GATE NAND 4CH 2-INP 14SOIC |
| Detailed Description | NAND Gate IC 4 Channel 14-SOIC |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

MC74VHC00DR2

Series:

74VHC

Logic Type:

NAND Gate

Number of Inputs:

2

Voltage - Supply:

2V ~ 5.5V

Current - Output High, Low:

8mA, 8mA

Input Logic Level - High:

1.5V

Operating Temperature:

-55°C ~ 125°C

Supplier Device Package:

14-SOIC

Base Product Number:

74VHC00

Manufacturer:

onsemi

Product Status:

Obsolete

Number of Circuits:

4

Features:

-

Current - Quiescent (Max):

2 μ A

Input Logic Level - Low:

0.5V

Max Propagation Delay @ V, Max CL:

7.5ns @ 5V, 50pF

Mounting Type:

Surface Mount

Package / Case:

14-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

Quad 2-Input NAND Gate

MC74VHC00, MC74VHCT00A

The MC74VHC00 and MC74VHCT00A are high speed CMOS quad 2-input NAND gate fabricated with silicon gate CMOS technology. These achieve high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC00 inputs are compatible with standard CMOS levels while the MC74VHCT00A inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The MC74VHC00 and MC74VHCT00A internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT00A output structures provide protection when $V_{CC} = 0$ V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

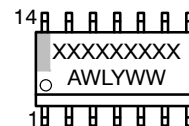
Features

- High Speed: $t_{PD} = 3.7$ ns (Typ) at $V_{CC} = 5.0$ V (VHC)
 $t_{PD} = 3.1$ ns (Typ) at $V_{CC} = 5.0$ V (VHCT)
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

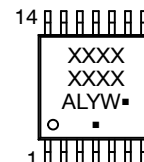
MARKING DIAGRAMS



SO-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G

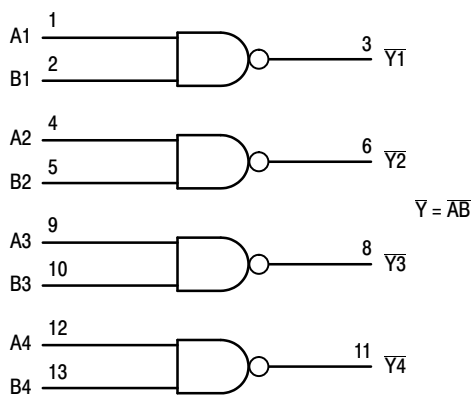
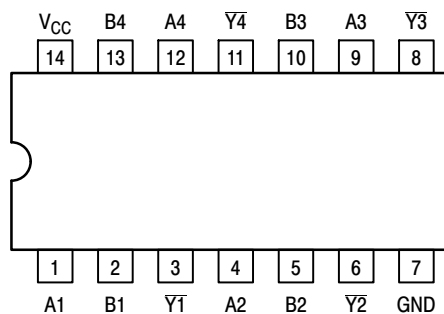


XXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

MC74VHC00, MC74VHCT00A**Figure 1. Logic Diagram****Figure 2. Pinout (Top View)****FUNCTION TABLE**

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|---|---|----------------------|
| V_{CC} | DC Supply Voltage | -0.5 to +6.5 | V |
| V_{IN} | DC Input Voltage | -0.5 to +6.5 | V |
| V_{OUT} | DC Output Voltage (MC74VHC) | -0.5 to $V_{CC} + 0.5$ | V |
| | DC Output Voltage (MC74VHCT) | Active Mode (High or Low State) Tristate Mode (Note 1) Power-Off Mode ($V_{CC} = 0$ V) | |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| I_{IK} | Input Clamp Current | -20 | mA |
| I_{OK} | Output Clamp Current | MC74VHC | ± 20 |
| | | MC74VHCT | -20 |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}$ C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | $^{\circ}$ C |
| T_J | Junction Temperature Under Bias | ± 150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance (Note 2) | SOIC-14 | 116 |
| | | TSSOP-14 | 150 |
| P_D | Power Dissipation in Still Air at 25 $^{\circ}$ C | SOIC-14 | 1077 |
| | | TSSOP-14 | 833 |
| MSL | Moisture Sensitivity | Level 1 | - |
| F_R | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| V_{ESD} | ESD Withstand Voltage (Note 3) | Human Body Model Charged Device Model | > 2000 N/A |
| $I_{LATCHUP}$ | Latchup Performance (Note 4) | ± 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

MC74VHC00, MC74VHCT00A**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|-----------------|-----------------------------|---|------------------------|------|
| MC74VHC | | | | |
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{IN} | DC Input Voltage (Note 5) | 0 | 5.5 | V |
| V_{OUT} | DC Output Voltage (Note 5) | 0 | V_{CC} | V |
| T_A | Operating Temperature Range | -55 | +125 | °C |
| t_r, t_f | Input Rise or Fall Time | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ 0 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ 0 | 100 20 | ns/V |
| MC74VHCT | | | | |
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{IN} | DC Input Voltage (Note 5) | 0 | 5.5 | V |
| V_{OUT} | DC Output Voltage (Note 5) | Active Mode (High or Low State) 0 Tristate Mode 0 Power-Off Mode ($V_{CC} = 0\text{ V}$) 0 | V_{CC} 5.5 5.5 | V |
| T_A | Operating Temperature Range | -55 | +125 | °C |
| t_r, t_f | Input Rise or Fall Time | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74VHC00, MC74VHCT00A**DC ELECTRICAL CHARACTERISTICS (MC74VHC00)**

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -55°C to 125°C | | Unit |
|-----------------|---------------------------|--|----------------------|-------------------------------|-------------------|-------------------------------|---------------------------------|-------------------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 3.0 to 5.5 | 1.50 V _{CC} × 0.7 | | | 1.50 V _{CC} × 0.7 | | V |
| V _{IL} | Low-Level Input Voltage | | 2.0 3.0 to 5.5 | | | 0.50 V _{CC} × 0.3 | | 0.50 V _{CC} × 0.3 | V |
| V _{OH} | High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OH} = -50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OH} = -4.0 mA I _{OH} = -8.0 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | |
| V _{OL} | Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0 0 0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OL} = 4.0 mA I _{OL} = 8.0 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | |
| I _{in} | Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 2.0 | | 20.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHC00)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A = ≤ 85°C | | T _A = ≤ +125°C | | Unit |
|--|---|--|---------------------|-----------------------|------------|-------------|-------------------------|-------------|---------------------------|------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, A or B to \bar{Y} | C _L = 15 pF C _L = 50 pF | 3.0 – 3.6 | | 5.5 8.0 | 7.9 11.4 | 1.0 1.0 | 9.5 13.0 | 1.0 1.0 | 10 14.5 | ns |
| | | C _L = 15 pF C _L = 50 pF | 4.5 – 5.5 | | 3.7 5.2 | 5.5 7.5 | 1.0 1.0 | 6.5 8.5 | 1.0 1.0 | 7.0 9.5 | |
| C _{in} | Input Capacitance | | | | 4.0 | 10 | | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 6) | 5.0 | Typical @ 25°C | | pF |
|-----------------|--|-----|----------------|--|----|
| | | | 19 | | |
| | | | | | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS

| Symbol | Characteristic | Test Conditions | T _A = 25°C | | Unit |
|------------------|--|---|-----------------------|------|------|
| | | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | V _{CC} = 5.0 V t _R = t _F = 3.0 ns C _L = 50 pF | 0.3 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | | -0.3 | -0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | | 3.5 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | | 1.5 | V |

MC74VHC00, MC74VHCT00A**DC ELECTRICAL CHARACTERISTICS (MC74VHCT00A)**

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = ≤ 85°C | | T _A = ≤ +125°C | | Unit | |
|-------------------|-------------------------------------|--|----------------------|-----------------------|------------|--------------------|-------------------------|--------------------|---------------------------|--------------------|------|----|
| | | | | Min | Typ | Max | Min | Max | Min | Max | | |
| V _{IH} | High-Level Input Voltage | | 3.0 4.5 5.5 | 1.4 2.0 2.0 | | | 1.4 2.0 2.0 | | 1.4 2.0 2.0 | | V | |
| V _{IL} | Low-Level Input Voltage | | 3.0 4.5 6.0 | | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | V |
| V _{OH} | High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | | | | | | V |
| | | I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | | | |
| | | I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | | | |
| V _{OL} | Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | | | | | | V |
| | | I _{OL} = 50 μA | 3.0 4.5 | | 0.0 0.0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | | |
| | | I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | | |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | | μA |
| I _{CC} | Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 2.0 | | 20 | | 40 | | μA |
| I _{CCCT} | Additional Quiescent Supply Current | V _{IN} = 3.4 V, any one input; V _{IN} = V _{CC} or GND, other inputs | 5.5 | | | 1.35 | | 1.5 | | 1.65 | | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

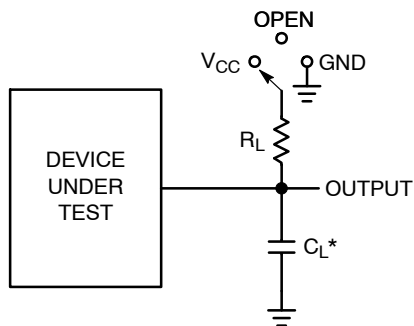
AC ELECTRICAL CHARACTERISTICS (MC74VHCT00A)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A = ≤ 85°C | | T _A = ≤ +125°C | | Unit |
|--|---|--|---------------------|-----------------------|----------------|-------------|-------------------------|-------------|---------------------------|--------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, A or B to \bar{Y} | C _L = 15 pF C _L = 50 pF | 3.0 - 3.6 | | 5.6 8.1 | 8.0 11.5 | 1.0 1.0 | 9.5 13.0 | | 12.0 16.0 | ns |
| | | C _L = 15 pF C _L = 50 pF | 4.5 - 5.5 | | 3.8 5.3 | 5.5 7.5 | 1.0 1.0 | 6.5 8.5 | | 8.5 10.5 | |
| C _{in} | Input Capacitance | | | | 4.0 | 10 | | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (Note 6) | | | 5.0 | Typical @ 25°C | | | | | pF | |
| | | | | | 17 | | | | | | |

NOISE CHARACTERISTICS

| Symbol | Characteristic | Test Conditions | T _A = 25°C | | Unit |
|------------------|--|---|-----------------------|------|------|
| | | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | V _{CC} = 5.0 V t _R = t _F = 3.0 ns C _L = 50 pF | 0.4 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | | -0.4 | -0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | | 2.0 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | | 0.8 | V |

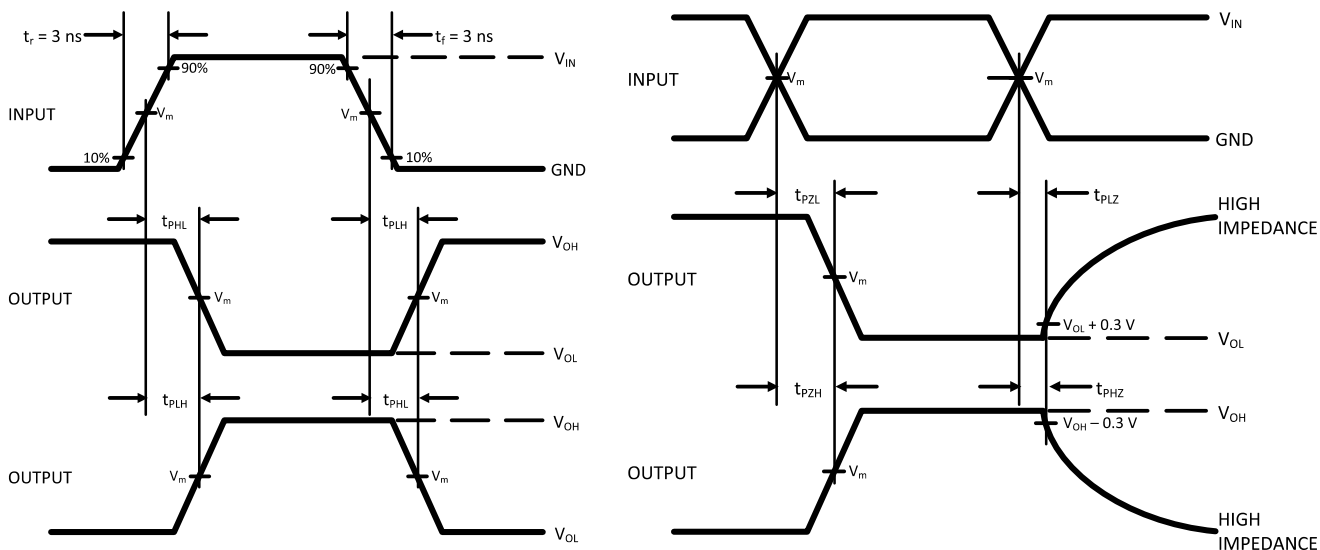
MC74VHC00, MC74VHCT00A



*C_L Includes probe and jig capacitance

| Test | Switch Position | C _L | R _L |
|-------------------------------------|-----------------|------------------------------|----------------|
| t _{PLH} / t _{PHL} | Open | See AC Characteristics table | 1 kΩ |
| t _{PLZ} / t _{PZL} | V _{CC} | | |
| t _{PHZ} / t _{PZH} | GND | | |

Figure 1. Test Circuit



| Device | V _{IN} , V | V _m , V |
|-------------|---------------------|-----------------------|
| MC74VHC00 | V _{CC} | 50% x V _{CC} |
| MC74VHCT00A | 3 V | 1.5 V |

Figure 2. Switching Waveforms

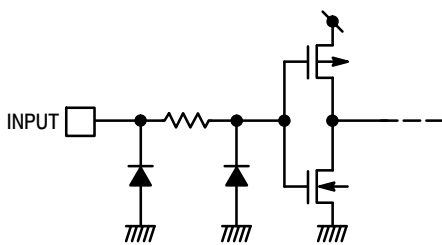


Figure 3. Input Equivalent Circuit (MC74VHC00, MC74VHCT00A)

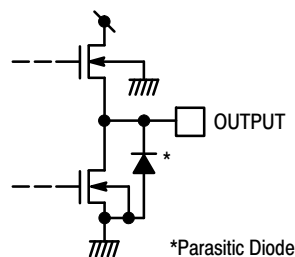


Figure 4. Output Equivalent Circuit (MC74VHCT00A)

MC74VHC00, MC74VHCT00A**ORDERING INFORMATION**

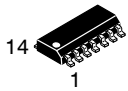
| Device | Marking | Package | Shipping[†] |
|---------------------|----------------|----------------|-----------------------------|
| MC74VHC00DR2G | VHC00G | SOIC-14 | 2500 / Tape & Reel |
| MC74VHC00DTG | VHC 00 | TSSOP-14 | 96 Units / Rail |
| MC74VHC00DTR2G | VHC 00 | TSSOP-14 | 2500 / Tape & Reel |
| MC74VHC00DTR2G-Q* | VHC 00 | TSSOP-14 | 2500 / Tape & Reel |
| MC74VHCT00ADR2G | VHCT00AG | SOIC-14 | 2500 / Tape & Reel |
| MC74VHCT00ADTR2G | VHCT 00A | TSSOP-14 | 2500 / Tape & Reel |
| MC74VHCT00ADTR2G-Q* | VHCT 00A | TSSOP-14 | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



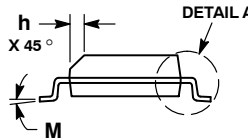
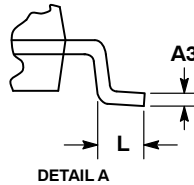
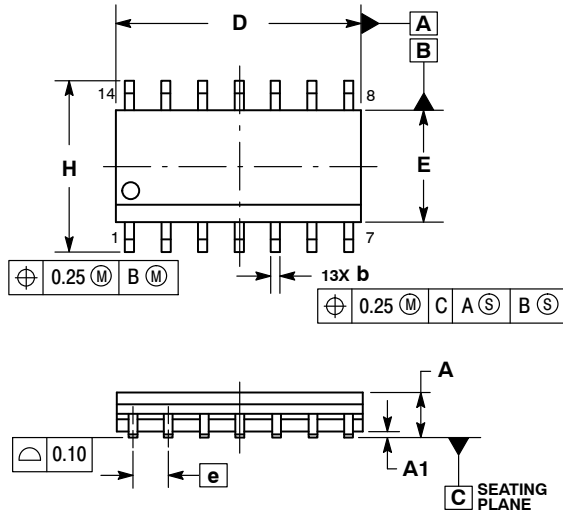
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

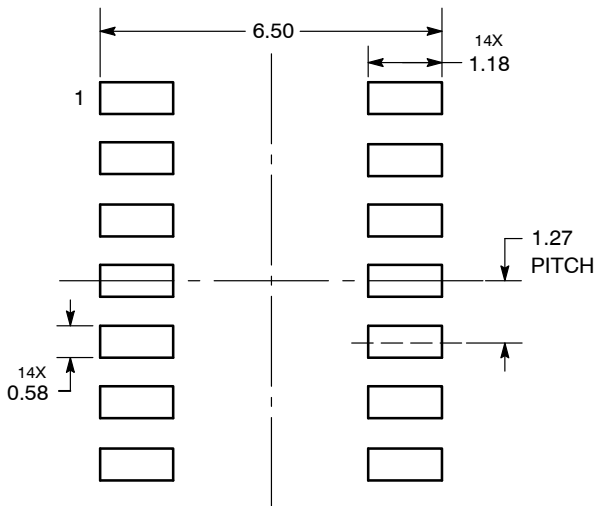


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

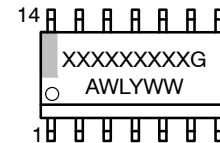
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|-------------------------|--------------------|---|
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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

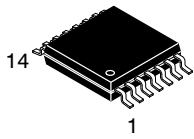
STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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| DESCRIPTION: | SOIC-14 NB | PAGE 2 OF 2 |

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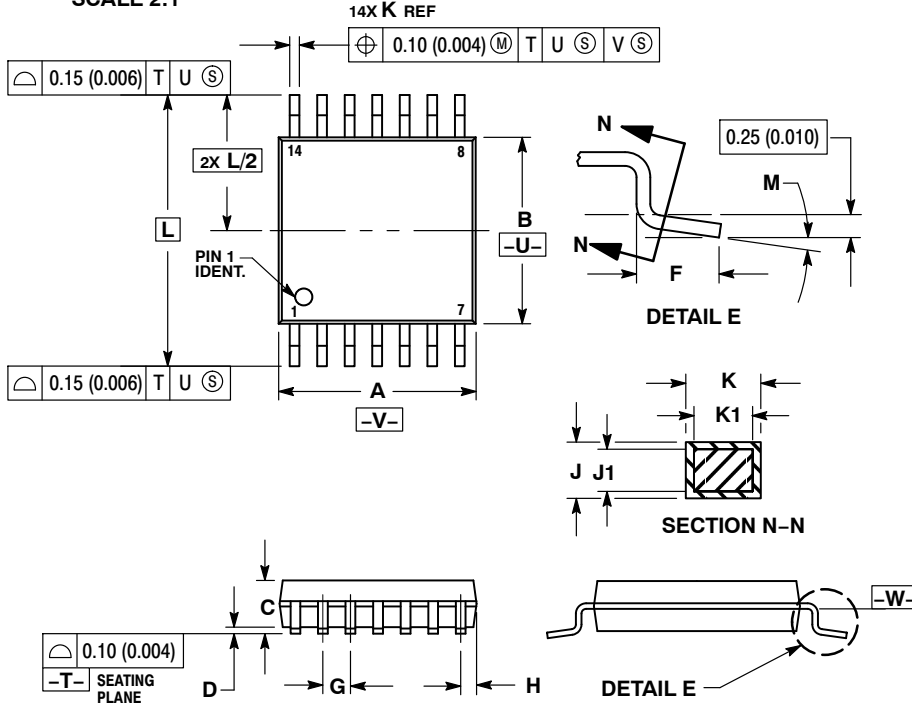
**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



**TSSOP-14 WB
CASE 948G
ISSUE C**

DATE 17 FEB 2016

SCALE 2:1

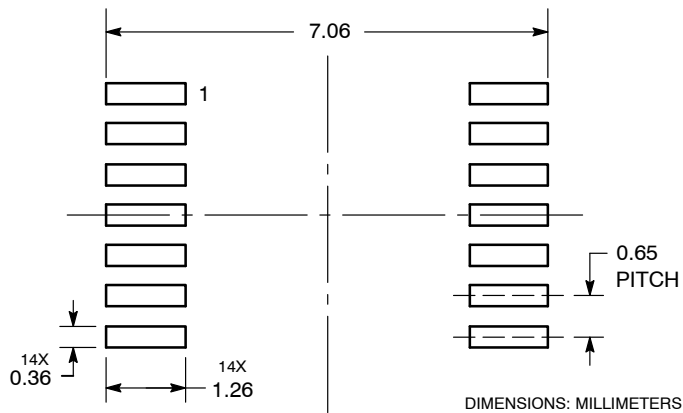


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

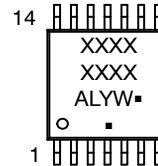
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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