MPS6729 Datasheet

DiGi Electronics Part Number	MPS6729-DG
Manufacturer	onsemi
Manufacturer Product Number	MPS6729
Description	TRANS PNP 80V 0.5A TO92
Detailed Description	Bipolar (BJT) Transistor PNP 80 V 500 mA 1 W Through Hole TO-92 (TO-226)

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MPS6729	onsemi
Series:	Product Status:
-	Obsolete
Transistor Type:	Current - Collector (Ic) (Max):
PNP	500 mA
Voltage - Collector Emitter Breakdown (Max):	Vce Saturation (Max) @ Ib, Ic:
80 V	500mV @ 10mA, 250mA
Current - Collector Cutoff (Max):	DC Current Gain (hFE) (Min) @ Ic, Vce:
100nA (ICBO)	50 @ 250mA, 1V
Power - Max:	Frequency - Transition:
1 W	-
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Through Hole
Package / Case:	Supplier Device Package:
TO-226-3, TO-92-3 Long Body	TO-92 (TO-226)
Base Product Number:	
MPS672	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS non-compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

MPS6729

Preferred Device

One Watt Amplifier Transistor

PNP Silicon

ON Semiconductor®

http://onsemi.com

Features

- Pb−Free Package is Available*

MAXIMUM RATINGS

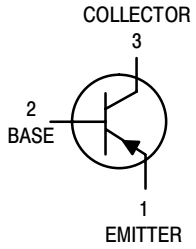
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−80	Vdc
Collector−Base Voltage	V_{CBO}	−80	Vdc
Emitter−Base Voltage	V_{EBO}	−4.0	Vdc
Collector Current − Continuous	I_C	−500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	W mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.5 20	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

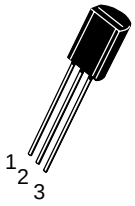
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	50	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

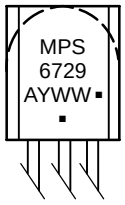
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.





TO−92 (TO−226)
CASE 29−10
STYLE 1

MARKING DIAGRAM



MPS6729 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
MPS6729	TO−92	5000 Units / Bulk
MPS6729G	TO−92 (Pb−Free)	5000 Units / Bulk

Preferred devices are recommended choices for future use and best overall value.

MPS6729

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 1) (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−80	−	Vdc
Collector−Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	−80	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector Cutoff Current (V_{CB} = −60 Vdc, I_E = 0)	I_{CBO}	−	−0.1	μAdc
Emitter Cutoff Current (V_{EB} = −5.0 Vdc, I_C = 0)	I_{EBO}	−	−10	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = −50 mAdc, V_{CE} = −1.0 Vdc) (I_C = −250 mAdc, V_{CE} = −1.0 Vdc)	h_{FE}	80 50	− 250	−
Collector−Emitter Saturation Voltage (I_C = −250 mAdc, I_B = −10 mAdc)	$V_{CE(sat)}$	−	−0.5	Vdc
Base−Emitter On Voltage (I_C = −250 mAdc, V_{CE} = −1.0 Vdc)	$V_{BE(on)}$	−	−1.2	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Collector−Base Capacitance (V_{CB} = −10 Vdc, f = 1.0 MHz)	C_{cb}	−	30	pF
Small−Signal Current Gain (I_C = 200 mA, V_{CE} = 5.0 V, f = 20 MHz)	h_{fe}	2.5	25	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

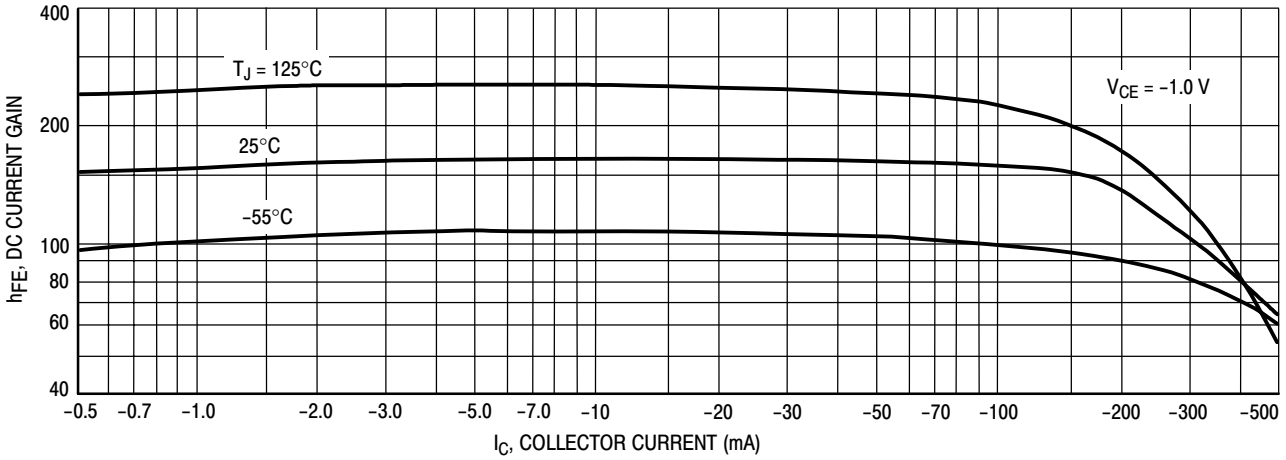


Figure 1. DC Current Gain

MPS6729

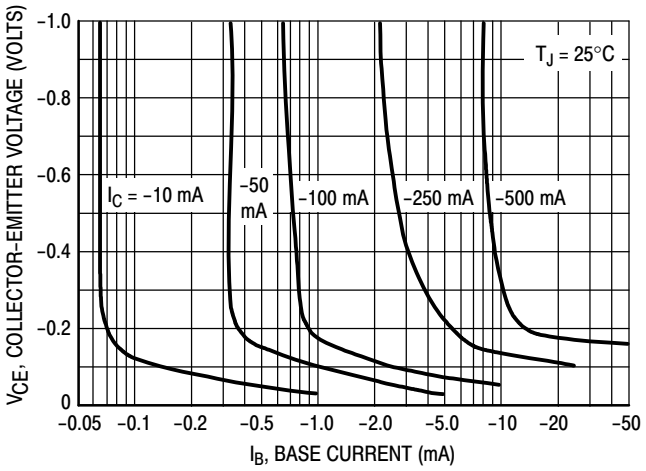


Figure 2. Collector Saturation Region

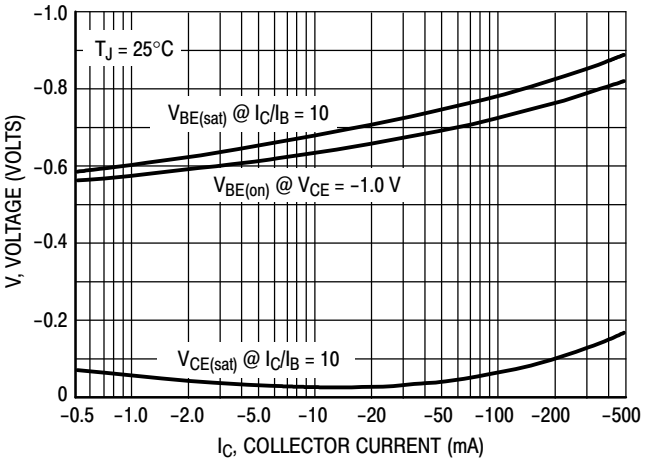


Figure 3. “On” Voltages

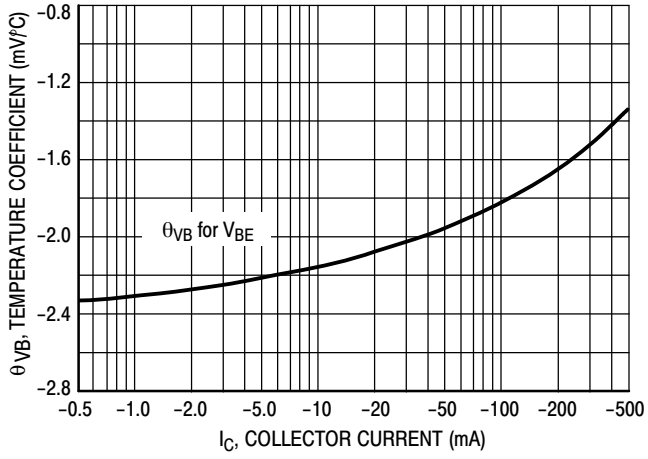


Figure 4. Base−Emitter Temperature Coefficient

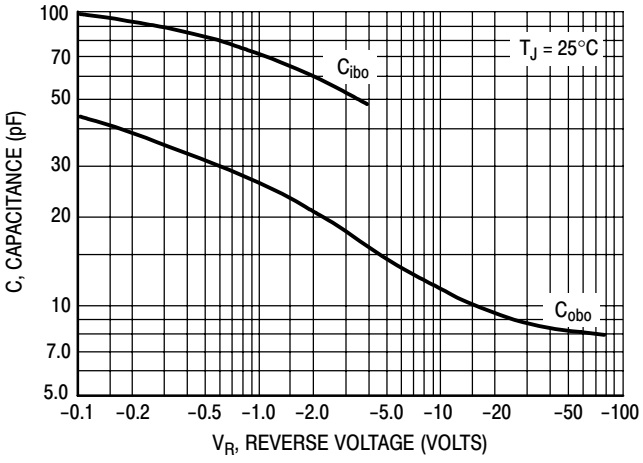


Figure 5. Capacitance

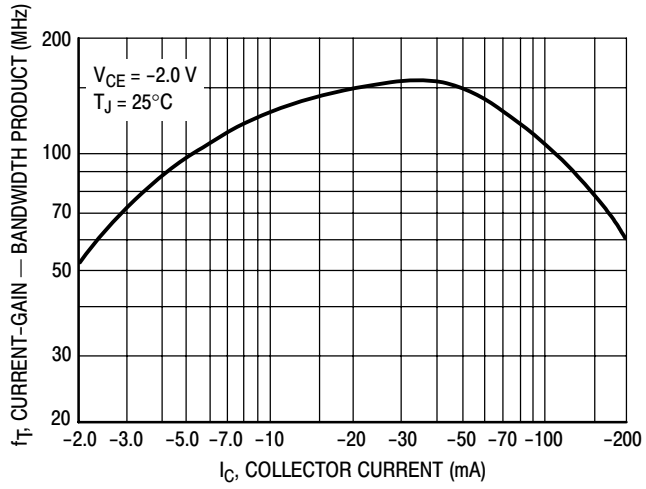


Figure 6. Current−Gain − Bandwidth Product

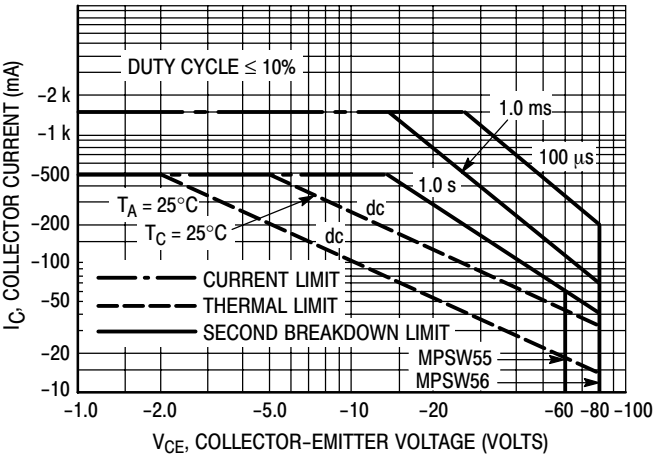


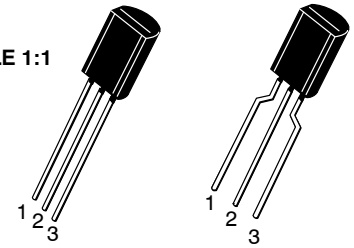
Figure 7. Active Region − Safe Operating Area

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

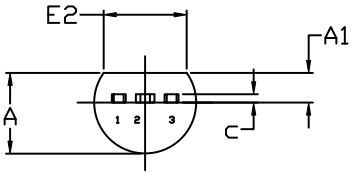
DATE 05 MAR 2021

SCALE 1:1

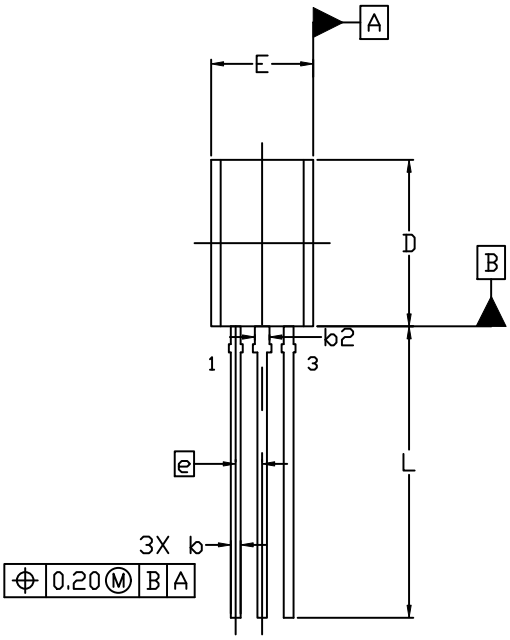


STRAIGHT LEAD BENT LEAD

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

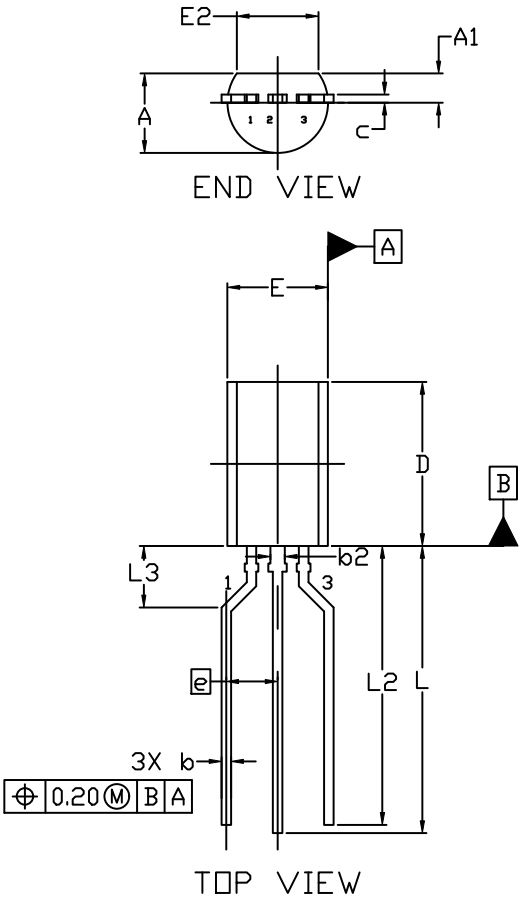
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



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D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−92 (TO−226) 1 WATT**		**PAGE 3 OF 3**

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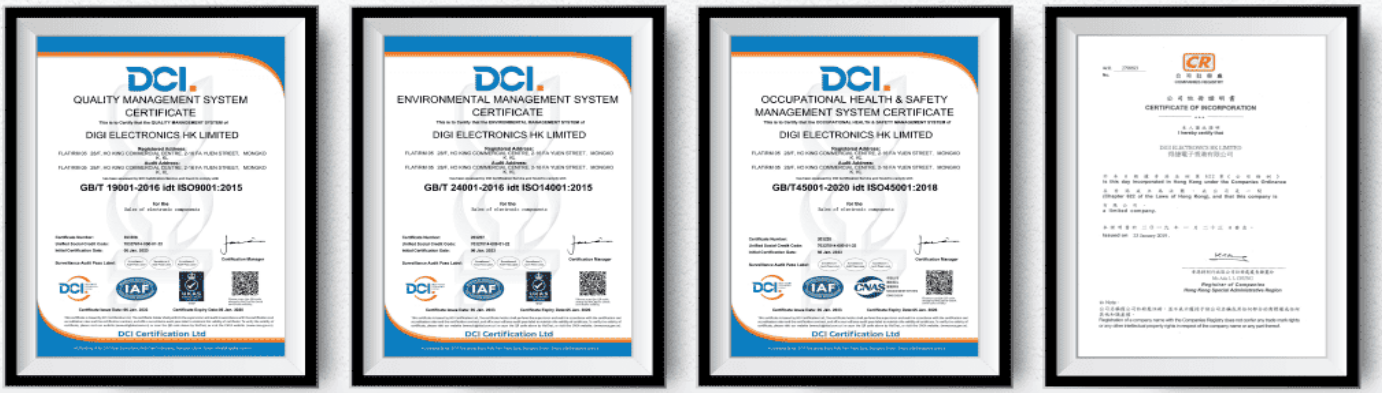

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