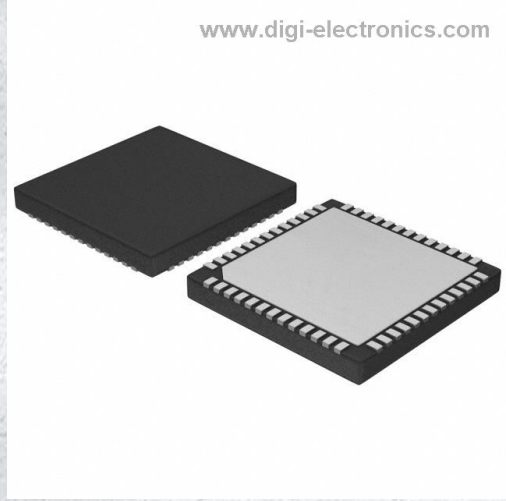
# NB100LVEP221MNG Datasheet




https://www.DiGi-Electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | NB100LVEP221MNG-DG |
| Manufacturer | onsemi |
| Manufacturer Product Number | NB100LVEP221MNG |
| Description | IC CLK BUFFER 2:20 1GHZ 52QFN |
| Detailed Description | Clock Fanout Buffer (Distribution), Multiplexer IC 2:20 1 GHz 52-VFQFN Exposed Pad |

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| NB100LVEP221MNG | onsemi |
| Series: | Product Status: |
| 100LVEP | Obsolete |
| Type: | Number of Circuits: |
| Fanout Buffer (Distribution), Multiplexer | 1 |
| Ratio - Input:Output: | Differential - Input:Output: |
| 2:20 | Yes/Yes |
| Input: | Output: |
| ECL, HSTL, LVPECL | ECL, PECL |
| Frequency - Max: | Voltage - Supply: |
| 1 GHz | 2.375V ~ 3.8V |
| Operating Temperature: | Mounting Type: |
| -40°C ~ 85°C | Surface Mount |
| Package / Case: | Supplier Device Package: |
| 52-VFQFN Exposed Pad | 52-QFN (8x8) |
| Base Product Number: | |
| NB100LV | |

## Environmental & Export classification

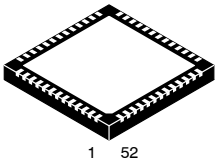
| Moisture Sensitivity Level (MSL): | REACH Status: |
| --- | --- |
| 2 (1 Year) | REACH Unaffected |
| ECCN: | HTSUS: |
| EAR99 | 8542.39.0001 |

# NB100LVEP221

# 2.5V/3.3V 2:1:20 Differential HSTL/ECL/PECL Clock Driver

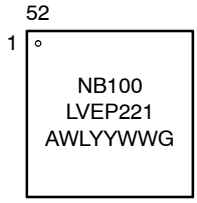
ON Semiconductor®

www.onsemi.com




**QFN52**
**MN SUFFIX**
**CASE 485M**

**MARKING DIAGRAM***




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

### Description

The NB100LVEP221 is a low skew 2:1:20 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The two clock inputs are differential ECL/PECL; CLK1/$\overline{\text{CLK1}}$ can also receive HSTL signal levels. The LVPECL input signals can be either differential configuration or single−ended (if the $V_{BB}$ output is used).

The LVEP221 specifically guarantees low output−to−output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs should be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The NB100LVEP221, as with most other ECL devices, can be operated from a positive $V_{CC}$ supply in LVPECL mode. This allows the LVEP221 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on PECL terminations, designers should refer to Application Note AND8020/D.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single−ended LVPECL input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

Single−ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in LVPECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

### Features

- 15 ps Typical Output−to−Output Skew
- 40 ps Typical Device−to−Device Skew
- Jitter Less than 2 ps RMS
- Maximum Frequency > 1.0 GHz Typical
- Thermally Enhanced 52−Lead QFN Package
- $V_{BB}$ Output
- 540 ps Typical Propagation Delay
- LVPECL and HSTL Mode Operating Range:
  $V_{CC}$ = 2.375 V to 3.8 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  $V_{CC}$ = 0 V with $V_{EE}$ = −2.375 V to −3.8 V
- Q Output will Default Low with Inputs Open or at $V_{EE}$
- Pin Compatible with Motorola MC100EP221
- These Devices are Pb−Free and are RoHS Compliant

# NB100LVEP221

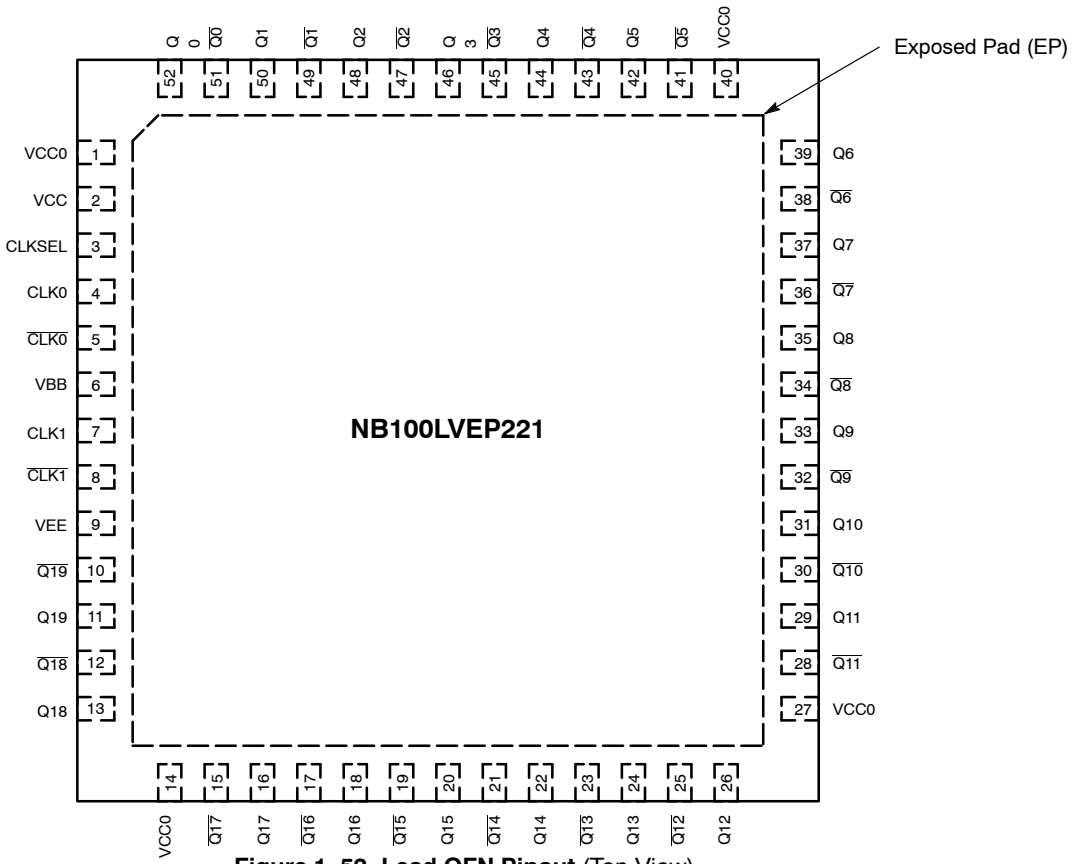



**Figure 1. 52−Lead QFN Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| CLK0*, $\overline{\text{CLK0}}$** | ECL/PECL Differential Inputs |
| CLK1*, $\overline{\text{CLK1}}$** | ECL/PECL or HSTL Differential Inputs |
| Q0:19, $\overline{\text{Q0:19}}$ | ECL/PECL Differential Outputs |
| CLK_SEL* | ECL/PECL Active Clock Select Input |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}/V_{CCO}$ | Positive Supply |
| $V_{EE}$*** | Negative Supply |

* Pins will default LOW when left open.
** Pins will default HIGH when left open.
***The thermally conductive exposed pad on the bottom of the package is electrically connected to $V_{EE}$ internally.

**Table 2. FUNCTION TABLE**

| CLK_SEL | Active Input |
|---|---|
| L | CLK0, $\overline{\text{CLK0}}$ |
| H | CLK1, $\overline{\text{CLK1}}$ |

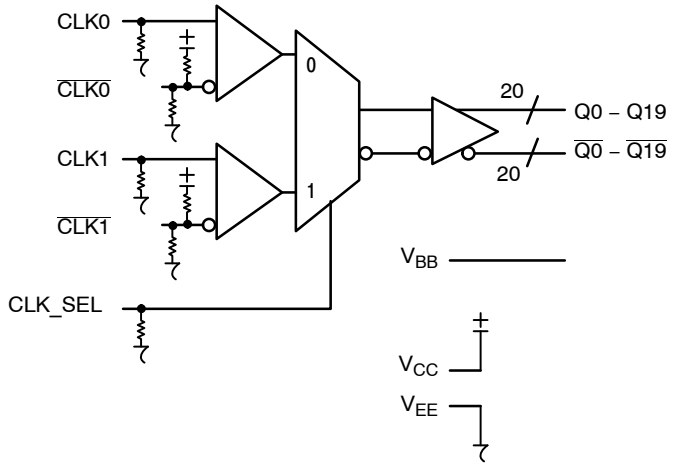



**Figure 2. Logic Diagram**

**Table 3. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ |
| Internal Input Pullup Resistor | | 37.5 kΩ |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb−Free Pkg |
| | QFN52 | Level 2 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 533 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, refer to Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note ) | 0 lfpm<br>500 lfpm | QFN52<br>QFN52 | 25<br>19.6 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) (Note ) | 2S2P | QFN52 | 21 | °C/W |
| $T_{sol}$ | Wave Solder<br>Pb<br>Pb−Free | | | 265<br>265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. LVPECL DC CHARACTERISTICS** $V_{CC}$ = 2.5 V; $V_{EE}$ = 0 V (Note 2)

| Symbol | Characteristic | –40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 100 | 125 | 150 | 104 | 130 | 156 | 116 | 145 | 174 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 555 | 680 | 900 | 555 | 680 | 900 | 555 | 680 | 900 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Note 4) | 1335 | | 1620 | 1335 | | 1620 | 1275 | | 1620 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 4) | 555 | | 900 | 555 | | 900 | 555 | | 900 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)<br>CLK0/$\overline{CLK0}$<br>CLK1/$\overline{CLK1}$ | <br>1.2<br>0.3 | | <br>2.5<br>1.6 | <br>1.2<br>0.3 | | <br>2.5<br>1.6 | <br>1.2<br>0.3 | | <br>2.5<br>1.6 | <br>V<br>V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>CLK<br>$\overline{CLK}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary + 0.125 V to −1.3 V.
3. All outputs loaded with 50 Ω to $V_{CC}$ − 2.0 V.
4. Do not use $V_{BB}$ at $V_{CC}$ < 3.0 V.
5. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 6. LVPECL DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V (Note 6)

| Symbol | Characteristic | –40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 100 | 125 | 150 | 104 | 130 | 156 | 116 | 145 | 174 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 7) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 7) | 1355 | 1480 | 1700 | 1355 | 1480 | 1700 | 1355 | 1480 | 1700 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1355 | | 1700 | 1355 | | 1700 | 1355 | | 1700 | mV |
| $V_{BB}$ | Output Reference Voltage (Note 8) | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)<br>CLK0/$\overline{CLK0}$<br>CLK1/$\overline{CLK1}$ | <br>1.2<br>0.3 | | <br>3.3<br>1.6 | <br>1.2<br>0.3 | | <br>3.3<br>1.6 | <br>1.2<br>0.3 | | <br>3.3<br>1.6 | <br>V<br>V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>CLK<br>$\overline{CLK}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary + 0.925 V to −0.5 V.
7. All outputs loaded with 50 Ω to $V_{CC}$ − 2.0 V.
8. Single−ended input operation is limited $V_{CC} \geq$ 3.0 V in LVPECL mode.
9. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 7. LVNECL DC CHARACTERISTICS** $V_{CC}$ = 0 V, $V_{EE}$ = −2.375 V to −3.8 V (Note 10)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 100 | 125 | 150 | 104 | 130 | 156 | 116 | 145 | 174 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 11) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 11) | −1945 | −1820 | −1600 | −1945 | −1820 | −1600 | −1945 | −1820 | −1600 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1945 | | −1600 | −1945 | | −1600 | −1945 | | −1600 | mV |
| $V_{BB}$ | Output Reference Voltage (Note 12) | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)<br>CLK0/$\overline{CLK0}$<br>CLK1/$\overline{CLK1}$ | <br>$V_{EE}$ + 1.2<br>$V_{EE}$ + 0.3 | | <br>0.0<br>−0.9 | <br>$V_{EE}$ + 1.2<br>$V_{EE}$ + 0.3 | | <br>0.0<br>−0.9 | <br>$V_{EE}$ + 1.2<br>$V_{EE}$ + 0.3 | | <br>0.0<br>−0.9 | <br>V<br>V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current CLK<br>$\overline{CLK}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Input and output parameters vary 1:1 with $V_{CC}$.
11. All outputs loaded with 50 Ω to $V_{CC}$−2.0 V.
12. Single−ended input operation is limited $V_{EE} \le -3.0$V in NECL mode.
13. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 8. HSTL DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{IH}$ | Input HIGH Voltage CLK1/$\overline{CLK1}$ | $V_x$+100 | | 1600 | $V_x$+100 | | 1600 | $V_x$+100 | | 1600 | mV |
| $V_{IL}$ | Input LOW Voltage CLK1/$\overline{CLK1}$ | −300 | | $V_x$−100 | −300 | | $V_x$−100 | −300 | | $V_x$−100 | mV |
| $V_X$ | Differential Configuration Cross Point Voltage | 680 | | 900 | 680 | | 900 | 680 | | 900 | mV |
| $I_{IH}$ | Input HIGH Current | −150 | | 150 | −150 | | 150 | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current CLK1<br>$\overline{CLK1}$ | −150<br>−250 | | | −150<br>−250 | | | −150<br>−250 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

**Table 9. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −2.375 to −3.8 V or $V_{CC}$ = 2.375 to 3.8 V; $V_{EE}$ = 0 V (Note 14)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{Opp}$ | Differential Output Voltage (Figure 3) $f_{out}$ < 50 MHz | 550 | 700 | | 600 | 700 | | 600 | 700 | | mV |
| | $f_{out}$ < 0.8 GHz | 550 | 700 | | 550 | 700 | | 500 | 700 | | mV |
| | $f_{out}$ < 1.0 GHz | 500 | 700 | | 500 | 700 | | 400 | 600 | | mV |
| $t_{PLH}/t_{PHL}$ | Propagation Delay (Differential Configuration) | | | | | | | | | | |
| | CLK0−Qx | | 540 | 600 | | 540 | 660 | | 540 | 750 | ps |
| | CLK1−Qx | | 590 | 640 | | 590 | 710 | | 590 | 800 | ps |
| $t_{skew}$ | Within−Device Skew (Note 15) | | 15 | 50 | | 15 | 50 | | 15 | 50 | ps |
| | Device−to−Device Skew (Note 16) | | 40 | 200 | | 40 | 200 | | 40 | 200 | ps |
| $t_{JITTER}$ | Random Clock Jitter (RMS) (Figure 3) | | 1 | 2 | | 1 | 2 | | 1 | 2 | ps |
| $V_{PP}$ | Input Swing (Differential Configuration) (Note 17) (Figure 4) CLK0 | 400 | 800 | 1200 | 400 | 800 | 1200 | 400 | 800 | 1200 | mV |
| | CLK1 HSTL | 300 | 800 | 1000 | 300 | 800 | 1000 | 300 | 800 | 1000 | mV |
| DCO | Output Duty Cycle | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | 49.5 | 50 | 50.5 | % |
| $t_r/t_f$ | Output Rise/Fall Time (20%−80%) | 100 | 200 | 300 | 100 | 200 | 300 | 150 | 250 | 350 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

14. Measured with 750 mV source (LVPECL) or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to $V_{CC}$−2 V.
15. Skew is measured between outputs under identical transitions and conditions on any one device.
16. Device−to−Device skew for identical transitions, outputs and $V_{CC}$ levels.
17. $V_{PP}$ is the differential configuration input voltage swing required to maintain AC characteristics.

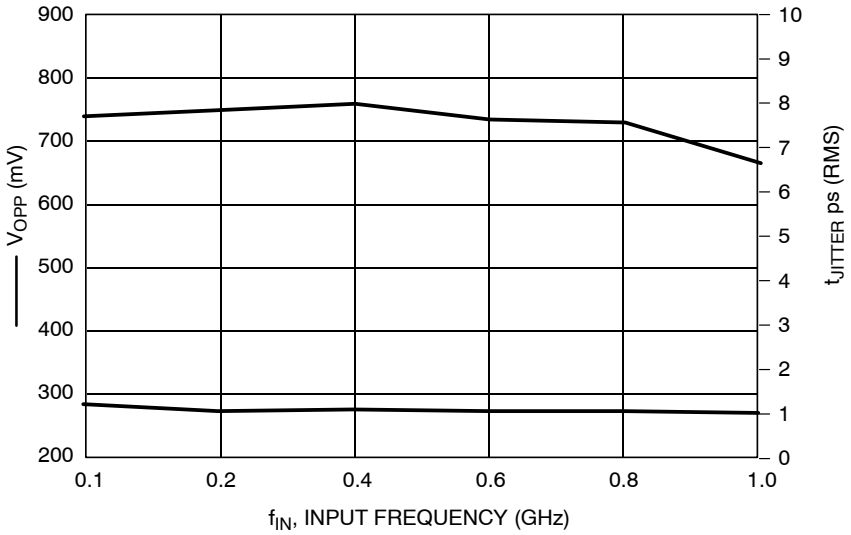



**Figure 3. Output Voltage ($V_{OPP}$)/Jitter versus Input Frequency ($V_{CC}$ – $V_{EE}$ = 3.3 V @ 25°C)**

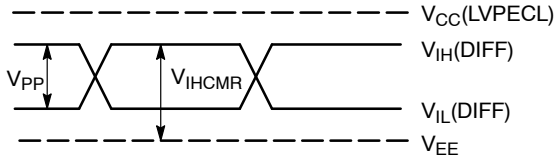



**Figure 4. LVPECL Differential Input Levels**

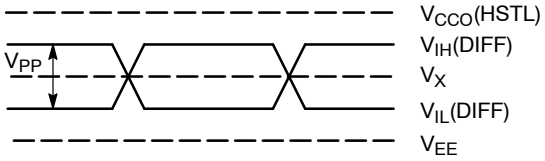



**Figure 5. HSTL Differential Input Levels**

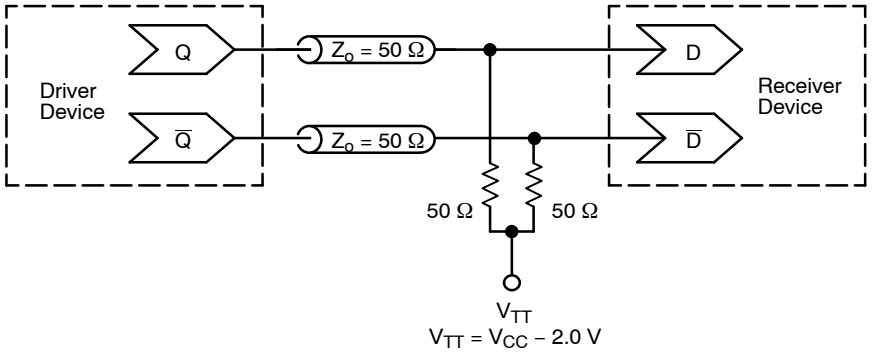



**Figure 6. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB100LVEP221MNRG | QFN52<br>(Pb−Free) | 2000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

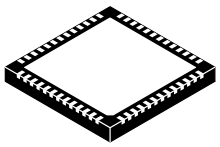
**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

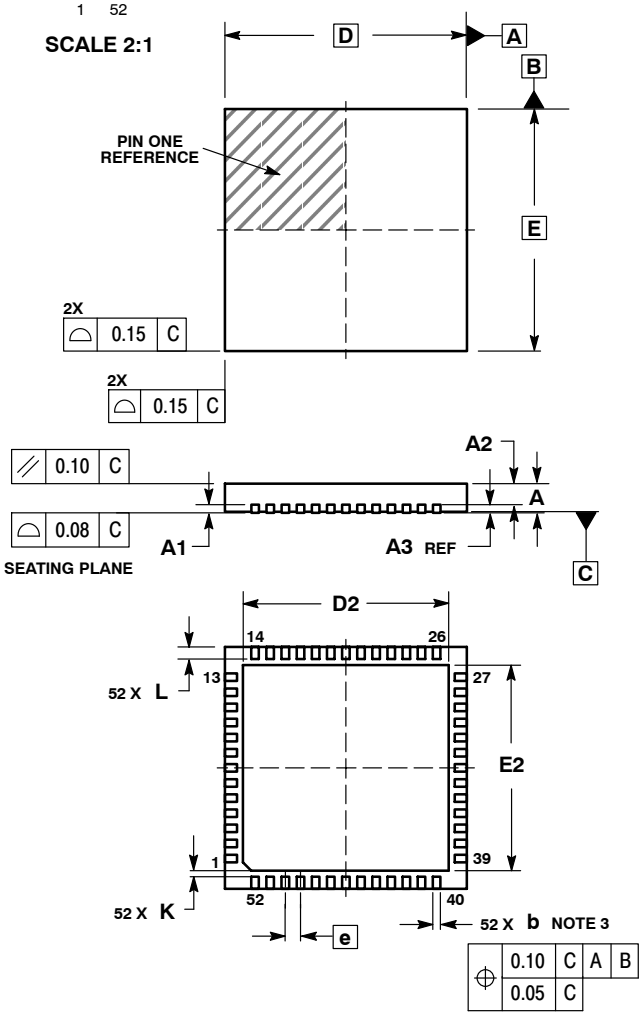
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**QFN52 8x8, 0.5P**
CASE 485M
ISSUE C

DATE 16 FEB 2010



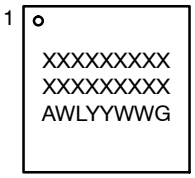

SCALE 2:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

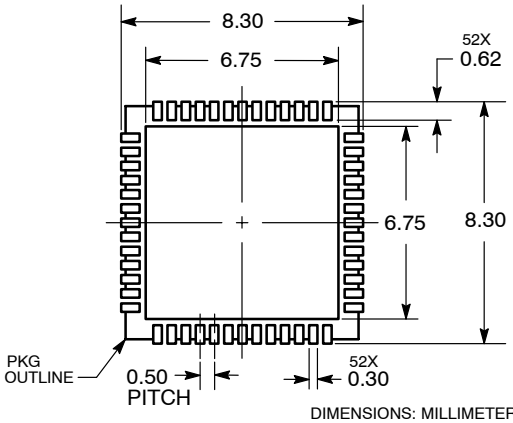
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.60 | 0.80 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 8.00 BSC | |
| D2 | 6.50 | 6.80 |
| E | 8.00 BSC | |
| E2 | 6.50 | 6.80 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |

### GENERIC MARKING DIAGRAM




| | |
|---|---|
| XXXXXXXXX | = Device Code |
| A | = Assembly Site |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

### RECOMMENDED SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

| | | |
|---|---|---|
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| **DESCRIPTION:** | **52 PIN QFN, 8X8, 0.5P** | **PAGE 1 OF 1** |

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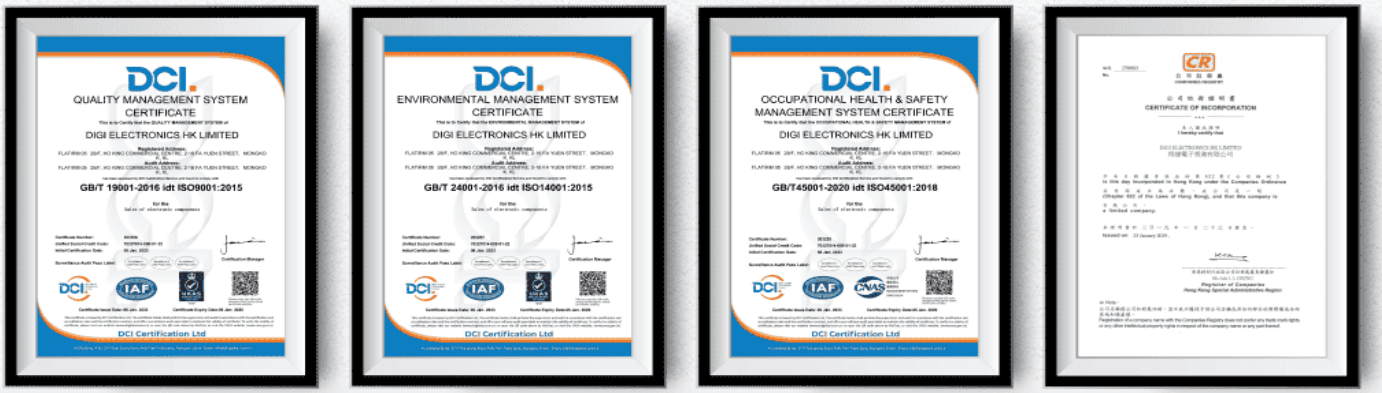



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