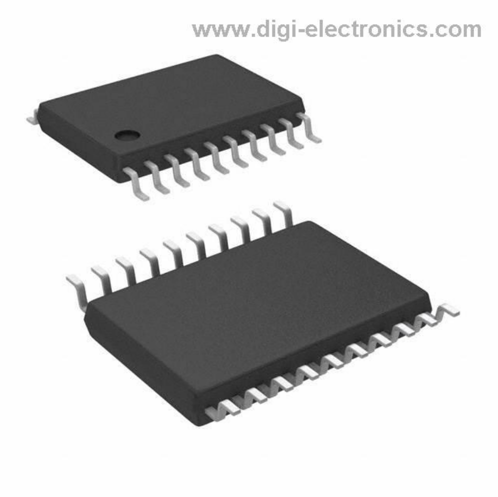
NB3N853531EDTR2G Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	NB3N853531EDTR2G-DG
Manufacturer	onsemi
Manufacturer Product Number	NB3N853531EDTR2G
Description	IC CLK BUFFER 2:4 266MHZ 20TSSOP
Detailed Description	Clock Fanout Buffer (Distribution), Multiplexer IC 2:4 266 MHz 20-TSSOP (0.173", 4.40mm Width)

Purchase and inquiry

Manufacturer Product Number:	NB3N853531EDTR2G	Manufacturer:	onsemi
Series:	-	Product Status:	Active
Type:	Fanout Buffer (Distribution), Multiplexer	Number of Circuits:	1
Ratio - Input:Output:	2:4	Differential - Input:Output:	No/Yes
Input:	LVCMOS, LVTTL, Crystal	Output:	LVPECL
Frequency - Max:	266 MHz	Voltage - Supply:	3.135V ~ 3.465V
Operating Temperature:	-40°C ~ 85°C	Mounting Type:	Surface Mount
Package / Case:	20-TSSOP (0.173", 4.40mm Width)	Supplier Device Package:	20-TSSOP
Base Product Number:	NB3N853531		

Environmental & Export classification

RoHS Status:	ROHS3 Compliant	Moisture Sensitivity Level (MSL):	1 (Unlimited)
REACH Status:	REACH Unaffected	ECCN:	EAR99
HTSUS:	8542.39.0001		

DATA SHEET
www.onsemi.com

3.3 V Xtal or LVTTL/LVCMOS Input 2:1 MUX to 1:4 LVPECL Fanout Buffer

NB3N853531E

Description

The NB3N853531E is a low skew 3.3 V supply 1:4 clock distribution fanout buffer. An input MUX selects either a Fundamental Parallel Mode Crystal or a LVCMOS/LVTTL Clock by using the CLK_SEL pin (HIGH for Crystal, LOW for Clock) with LVCMOS / LVTTL levels.

The single ended CLK input is translated to four LVPECL Outputs. Using the crystal input, the NB3N853531E can be a Clock Generator. A CLK_EN pin can enable or disable the outputs synchronously to eliminate runt pulses using LVCMOS/LVTTL levels (HIGH to enable outputs, LOW to disable outputs).

Features

- Four Differential 3.3 V LVPECL Outputs
- Selectable Crystal or LVCMOS/LVTTL CLOCK Inputs
- Up to 266 MHz Clock Operation
- Output to Output Skew: 30 ps (Max)
- Device to Device Skew 200 ps (Max)
- Propagation Delay 1.8 ns (Max)
- Operating Range: V_{CC} = 3.3 ±5% V(3.135 to 3.465 V)
- Additive Phase Jitter, RMS: 0.053 ps (Typ)
- Synchronous Clock Enable Control
- Industrial Temp. Range (−40°C to 85°C)
- Pb−Free TSSOP−20 Package
- Ambient Operating Temperature Range −40°C to +85°C
- These Devices are Pb−Free and are RoHs Compliant

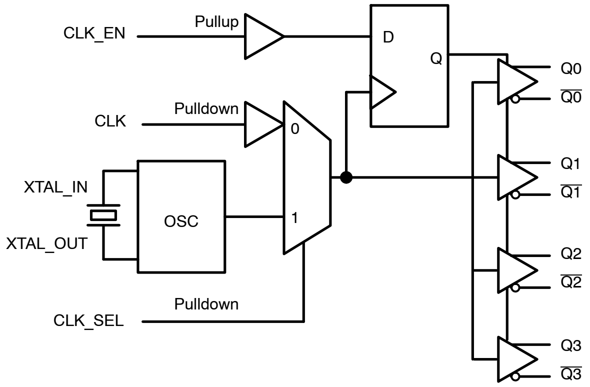
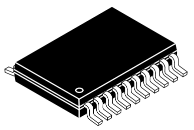
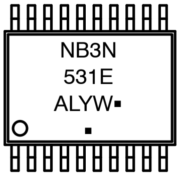


Figure 1. Simplified Logic Diagram



TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NB3N853531EDTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

January, 2024 − Rev. 8

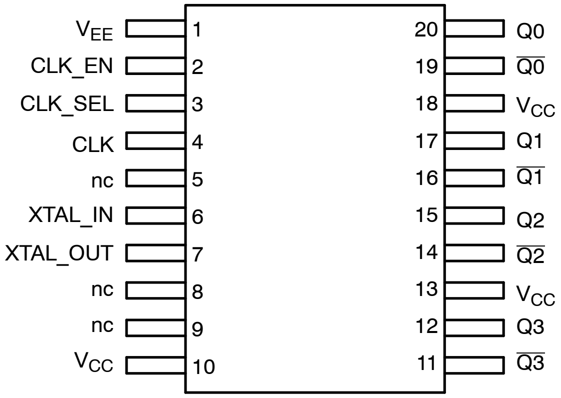


Figure 2. Pinout Diagram (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Open Default	Description
1	V_{EE}			Negative (Ground) Power Supply pin must be externally connected to power supply to guarantee proper operation.
2	CLK_EN	LVCMOS / LVTTL	Pullup	Synchronized Clock Enable when HIGH. When LOW, outputs are disabled (Qx HIGH, $\overline{Qx}$ LOW)
3	CLK_SEL	LVCMOS / LVTTL	Pulldown	Clock Input Select (HIGH selects crystal, LOW selects CLK input)
4	CLK	LVCMOS / LVTTL	Pulldown	Clock Input. Float open when unused.
5, 8, 9	nc			No Connect
6	XTAL_IN	Crystal		Crystal Oscillator Input (used with pin 7). Float open when unused.
7	XTAL_OUT	Crystal		Crystal Oscillator Output (used with pin 6). Float open when unused.
10, 13, 18	V_{CC}			Positive Power Supply pins must be externally connected to power supply to guarantee proper operation.
11, 14, 16, 19	$\overline{Q[3:0]}$	LVPECL		Complement Differential Outputs (See AND8002/D for termination)
12, 15, 17, 20	Q[3:0]	LVPECL		True Differential Outputs (See AND8002/D for termination)

Table 2. FUNCTIONS

Inputs			Outputs		
CLK_EN	CLK_SEL	Input Function	Output Function	Qx	$\overline{Qx}$
0	0	CLK input selected	Disabled	LOW	HIGH
0	1	Crystal Inputs Selected	Disabled	LOW	HIGH
1	0	CLK input selected	Enabled	CLK0	Invert of CLK1
1	1	Crystal Inputs Selected	Enabled	CLK1	Invert of CLK1

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in Figure 3.

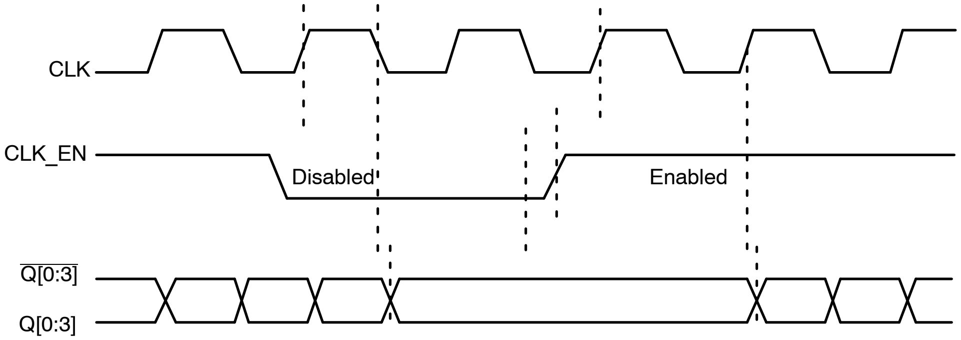


Figure 3. CLK_EN Timing Diagram

Table 3. ATTRIBUTES (Note 2)

Characteristics	Value
Internal Input Pullup Resistor	50 kΩ
Internal Input Pulldown Resistor	50 kΩ
C_{in} Input Capacitance	4 pF
ESD Protection Human Body Model Machine Model	 > 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)	Level 1
Flammability Rating Oxygen Index	UL 94 V−0 @ 0.125 in 28 to 34
Transistor Count	333 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Supply Voltage			4.6	V
V_{in}	Input Voltage			$-0.5 \le V_I \le VCC + 0.5$	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range, Industrial			−40 to ≤ +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm	Single−Layer PCB (700 mm^2, 2 oz)	128	°C/W
		200 lfpm	Multi−Layer PCB (700 mm^2, 2 oz)	94	
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 4)	TSSOP−20	23 to 41	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. CRYSTAL CHARACTERISTICS AND CONNECTIONS

Parameter	Min	Typ	Max	Unit
Mode of Oscillation	Fundamental Parallel			
Frequency	12		40	MHz
Equivalent Series Resistance (ESR)			50	Ω
Shunt Capacitance			7	pF
Drive Level			1	mW

Table 6. DC CHARACTERISTICS V_{CC} = 3.3 ±5% V (3.135 to 3.465 V), V_{EE} = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
I_{EE}	Power Supply Current				60	mA
V_{IH}	Input HIGH Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3		0.8	V
I_{IH}	Input High Current (V_{CC} = 3.456 V)	CLK, CLK_SEL = 3.456 V CLK_EN = 3.456 V			150 5	µA
I_{IL}	Input LOW Current (V_{CC} = 3.456 V)	CLK, CLK_SEL = 3.456 V CLK_EN = 3.456 V	−5 −150			µA
V_{OH}	Output HIGH Voltage		V_{CC} − 1.4		V_{CC} − 0.9	V
V_{OL}	Output LOW Voltage		V_{CC} − 2.0		V_{CC} − 1.7	V
$VOUT_{SWING}$	Output Voltage Swing (peak−to−peak)		0.6		1.0	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Outputs terminated 50 Ω to V_{CC} − 2.0 V, see Figure 4.

Table 7. AC CHARACTERISTICS V_{CC} = 3.3 ±5% V (3.135 to 3.465 V), V_{EE} = 0 V, TA = −40°C to +85°C (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
F_{MAX}	Maximum Operating Frequency	0		266	MHz
t_{PD}	Propagation Delay (Notes 7 and 9)	1.1		1.8	ns
$tSKEW_{DC}$	Duty Cycle Skew same path similar conditions at 50 MHz (Notes 7, 8 and 9)	46		54	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (Notes 7, 8 and 9)			30	ps
$tSKEW_{D-D}$	Device to Device Skew similar path and conditions (Notes 7, 8 and 9)			200	ps
t_{JIT}	Additive Phase Noise Jitter (RMS) @ 155.52 MHz (Integrated from 12 kHz to 20 MHz) See Figure 6. (Note 9)		0.053		ps
t_r/t_f	Output rise and fall times (20% and 80% points) (Note 9)	225		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Outputs terminated 50 Ω to V_{CC} − 2.0 V, see Figure 4.
7. Measured under the same supply voltage, output loading, and input conditions.
8. Similar conditions.
9. Limits do not apply to overdriving XTAL_IN.

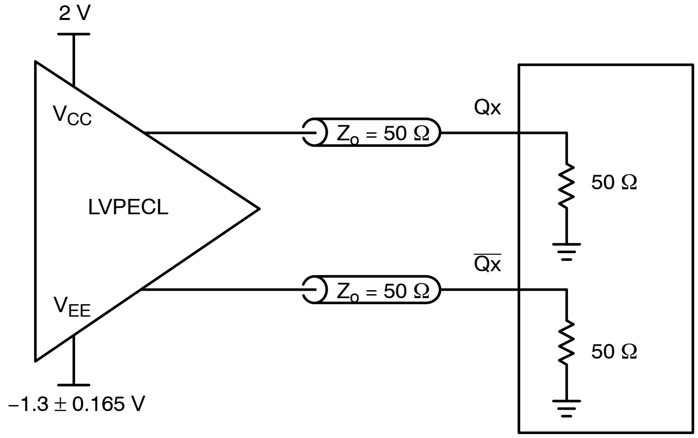
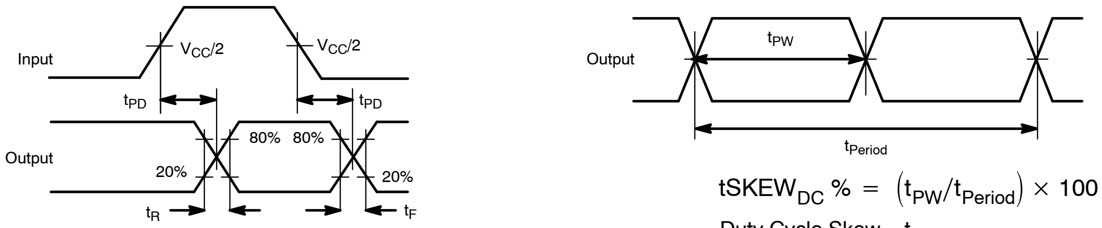


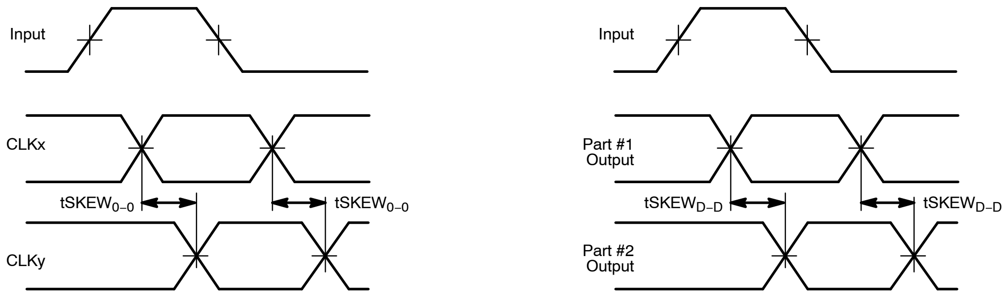
Figure 4. Typical Test Setup and Termination for Evaluation. A split supply of V_{CC} = 2.0 V and V_{EE} = −1.3 ±0.165 V allows a convenient direct connection termination into typical oscilloscope 50 Ω to GND impedance modules. For Application termination schemes see AND8020.



$$\text{tSKEW}_{DC}\ \% = \left(t_{PW}/t_{Period}\right) \times 100$$

Propagation Delay t_{PD}

Duty Cycle Skew − t_{SKEWDC}



Output−to−Output Skew tSKEW_{0-0}

Device−to−Device Skew, tSKEW_{D-D}

Figure 5. AC Measurement Reference

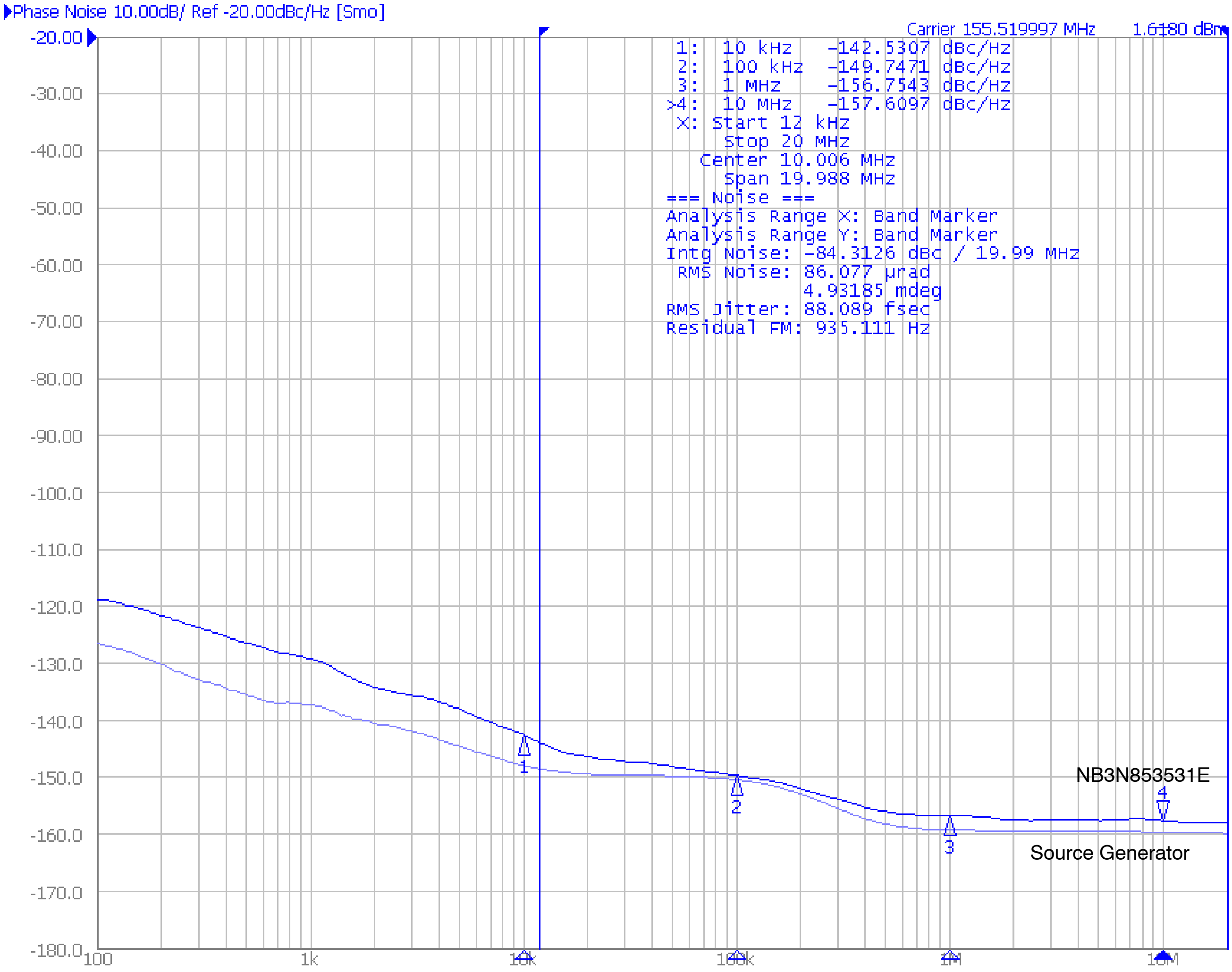


Figure 6. For 155.52 MHz Carrier, the NB3N853531E Additive Phase Noise (dBc/Hz) verses SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 88.1 fs RMS. The E8663B Source Generator Additive Phase Noise (Lower Light Line) is 70.1 fs RMS. Where $t_{JIT} = \sqrt{(t_{JIToutput})^2 - (t_{JITinput})^2} = 53$ fs

Application – Crystal Input Interface

Figure 7 shows the NB3N853531E device crystal oscillator interface using a typical parallel resonant crystal. A parallel crystal with loading capacitance C_L = 18 pF could use Series Load Caps C1 = 32 pF and C2 = 32 pF as nominal values, after subtracting a typical 4 pF of stray cap per line. The frequency accuracy and duty cycle skew can be fine tuned by adjusting the C1 and C2 values. For example, increasing the C1 and C2 values will reduce the operational frequency. Note R1 is optional and may be 0 Ω.

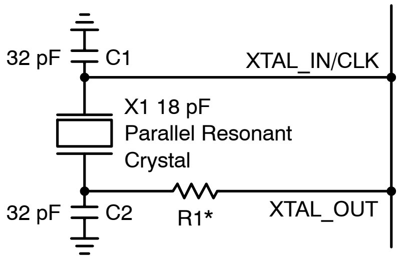


Figure 7. NB3N853531E Crystal Oscillator Interface

*R1 is optional. Assuming 4 pF stray cap per pin.

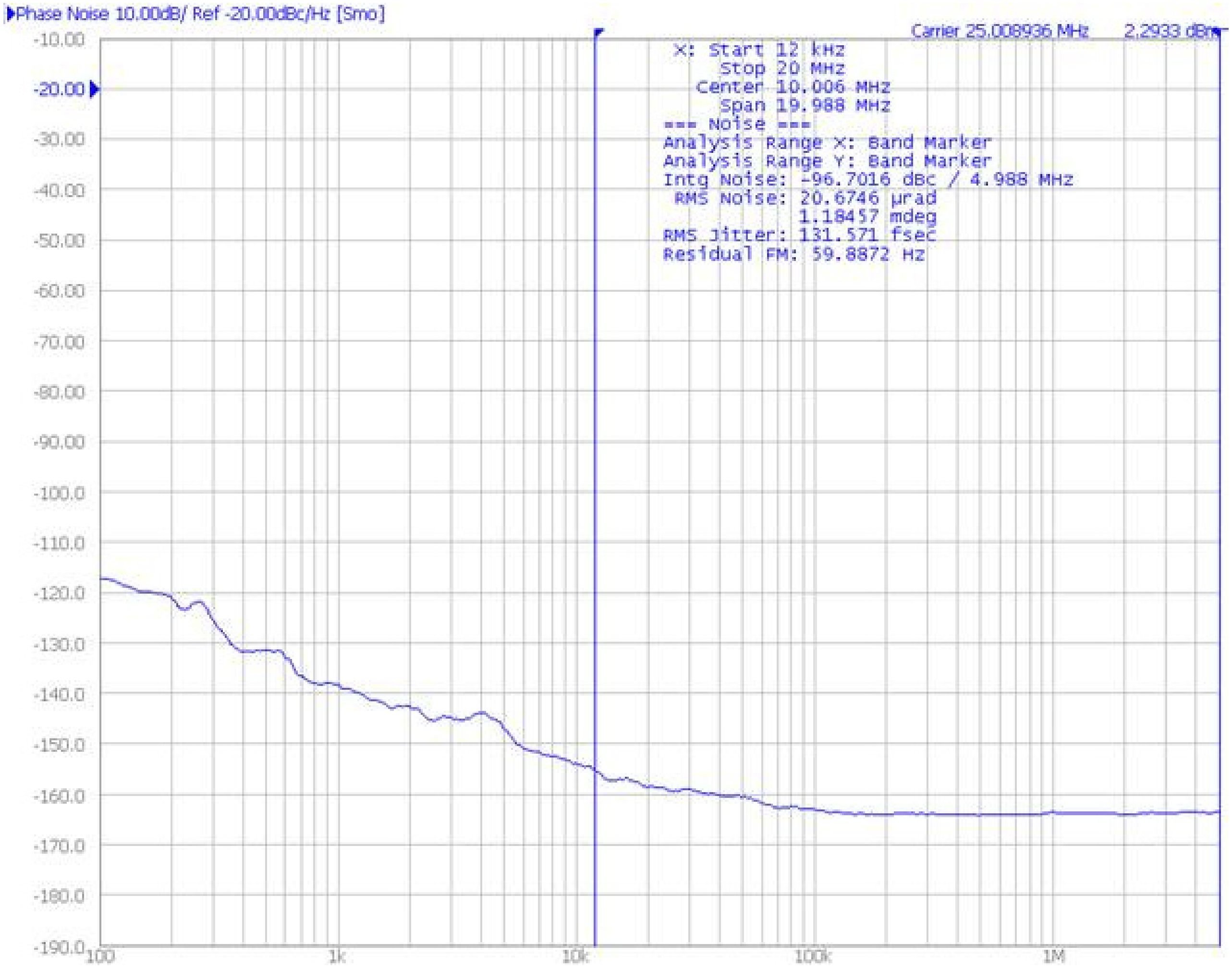
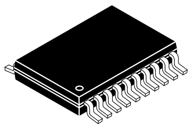


Figure 8. NB3N853531E Phase Noise with 25 MHz Crystal

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

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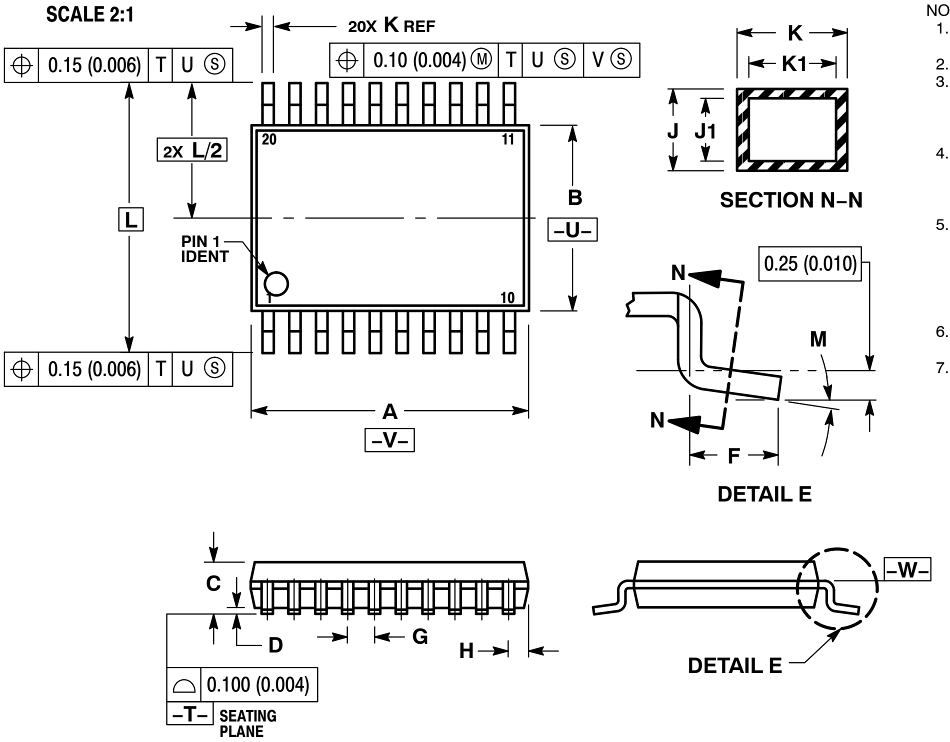
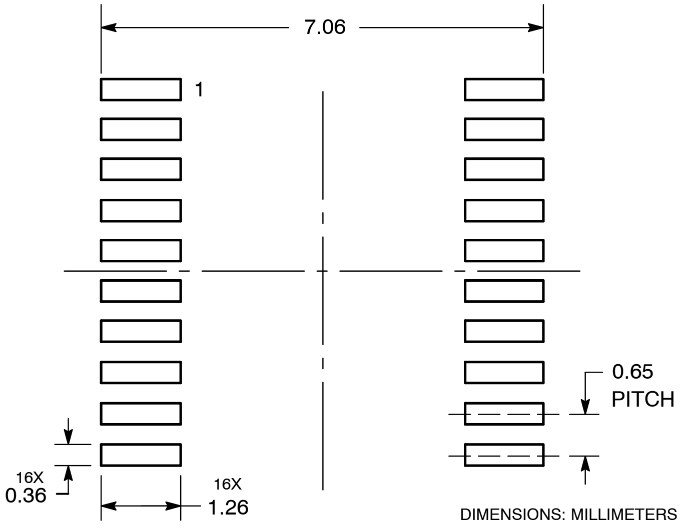


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

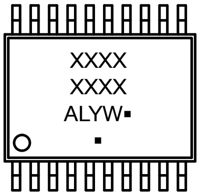
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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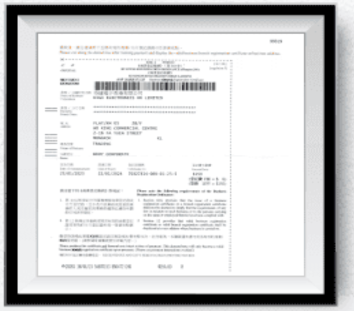

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