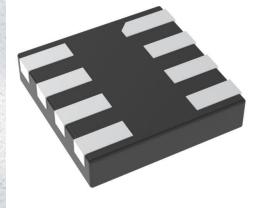


# **NB3V1102CMTTBG Datasheet**

www.digi-electronics.com



DiGi Electronics Part Number

Manufacturer

Manufacturer Product Number

Description

**Detailed Description** 

NB3V1102CMTTBG-DG

onsemi

NB3V1102CMTTBG

IC CLK BUFFER 1:2 250MHZ 8WDFN

Clock Fanout Buffer (Distribution) IC 1:2 250 MHz 8-WFDFN

https://www.DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



# Purchase and inquiry

NB3V1102CMTTBG         onsemi           Series:         Product Status:           Active         Active           Type:         Number of Circuits:           Fanout Buffer (Distribution)         1           Ratio - Input:Output:         Differential - Input:Output:           Input:         No/No           Input:         Output:           LVCMOS         LVCMOS           Frequency - Max:         VCMOS           Operating Temperature:         Voltage - Supply:           -400C ~ 105°C (TA)         Surface Mount           Package / Case:         Supplier Device Package:           B-WFDFN         Supplier Device Package:		
Series:Product Status:ActiveType:Number of Circuits:Fanout Buffer (Distribution)1Ratio - Input: Output:Differential - Input:Output:Input:No/NoLVCMOSUtput:Frequency - Max:Voltage - Supply:250 MHzNorting Type:Operating Temperature:Surface Mount40°C ~ 105°C (TA)Surface MountPackage / Case:Supplier Device Package:B-WFDFNB-WEDFN (2x2)	Manufacturer Product Number:	Manufacturer:
A         Ative           Type:         Number of Circuits:           Fanout Buffer (Distribution)         1           Ratio - Input: Output:         Differential - Input: Output:           1:2         No/No           Input:         Output:           LVCMOS         UCMOS           Frequency - Max:         VCMOS           250 MHz         No/No           Operating Temperature:         Mounting Type:           -40°C ~ 10°C (TA)         Surface Mount           Package / Case:         Surplice Package:           BYPEPN         BoxPEPN	NB3V1102CMTTBG	onsemi
Type:Number of Circuits:Fanout Buffer (Distribution)1Ratio - Input: Output:Differential - Input:Output:1:2No/NoInput:Output:LVCMOSLVCMOSFrequency - Max:Voltage - Supply:250 MHzNo/NoOperating Temperature:Mounting Type:-40°C ~ 105°C (TA)Supplier Device Package:B-WFDFNSwDFN (2x2)	Series:	Product Status:
Fanout Buffer (Distribution) 1 Ratio - Input: Output: Differential - Input: Output: Control C		Active
Ratio - Input:Output:Differential - Input:Output:1:2No/NoInput:Output:LVCMOSVCMOSFrequency - Max:VOROS250 MHzNo/NoOperating Temperature:No/No-40°C ~ 105°C (TA)Surface MountPackage / Case:Surple: Case:B-WFDFNB-WDFN (2x2)Base Product Number:Surple: Case:	Туре:	Number of Circuits:
1:2No/NoInput:Output:LVCMOSVCMOSFrequency - Max:Voltage - Supply:250 MHz1.71V ~ 3.6VOperating Temperature:Mounting Type:-40°C ~ 105°C (TA)Surface MountPackage / Case:Supplier Device Package:B-WFDFN8-WDFN (2x2)	Fanout Buffer (Distribution)	1
Input:Output:LVCMOSLVCMOSFrequency - Max:Voltage - Supply:250 MHz1.71V ~ 3.6VOperating Temperature:Mounting Type:-40°C ~ 105°C (TA)Surface MountPackage / Case:Supplier Device Package:B-WFDFN8-WDFN (2x2)	Ratio - Input:Output:	Differential - Input:Output:
LVCMOSLVCMOSFrequency - Max:Voltage - Supply:250 MHz1.71V ~ 3.6VOperating Temperature:Mounting Type:-40°C ~ 105°C (TA)Surface MountPackage / Case:Supplier Device Package:B-WFDFNB-WDFN (2x2)	1:2	No/No
Frequency - Max:Voltage - Supply:250 MHz1.71V ~ 3.6VOperating Temperature:Mounting Type:-40°C ~ 105°C (TA)Surface MountPackage / Case:Supplier Device Package:8-WFDFN8-WDFN (2x2)	Input:	Output:
250 MHz 1.71V ~ 3.6V Dperating Temperature: Mounting Type: Mounting Type: Surface Mount -40°C ~ 105°C (TA) Surface Mount Package / Case: Supplier Device Package: Suppli	LVCMOS	LVCMOS
Operating Temperature:     Mounting Type:       -40°C ~ 105°C (TA)     Surface Mount       Package / Case:     Supplier Device Package:       B-WFDFN     8-WDFN (2x2)	Frequency - Max:	Voltage - Supply:
-40°C ~ 105°C (TA) Surface Mount Package / Case: Supplier Device Package: Supplier Device Packag	250 MHz	1.71V ~ 3.6V
Package / Case:     Supplier Device Package:       B-WFDFN     8-WDFN (2x2)	Operating Temperature:	Mounting Type:
8-WFDFN 8-WDFN (2x2)	-40°C ~ 105°C (TA)	Surface Mount
Base Product Number:	Package / Case:	Supplier Device Package:
	8-WFDFN	8-WDFN (2x2)
NB3V1102	Base Product Number:	
	NB3V1102	

# **Environmental & Export classification**

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

# onsemi

# **3.3 V / 2.5 V / 1.8 V LVCMOS Low Skew Fanout Buffer Family**



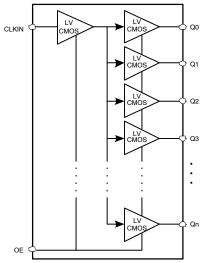
# Description

The NB3V110xC are a modular, high-performance, low-skew, general purpose LVCMOS clock buffer family. The family of devices is designed with a modular approach. Four different fan-out variations, 1:2, 1:3, 1:4, 1:6 and 1:8, are available. All of the devices are pin compatible to each other for easy handling. All family members share the same high performing characteristics like low additive jitter, low skew, and wide operating temperature range. The NB3V110xC supports an asynchronous output enable control (OE) which switches the outputs into a low state when OE is low. The NB3V110xC devices operate in a 3.3 V, 2.5 V and 1.8 V environment and are characterized for operation from  $-40^{\circ}$ C to  $105^{\circ}$ C.

### Features

- Operating Temperature Range: -40°C to 105°C
- High-Performance 1:2, 1:3, 1:4, 1:6, 1:8 LVCMOS Clock Buffer
- Available in 8–, 14–, 16–Pin TSSOP and WDFN8 Packages
- Very Low Output–to–Output Skew < 50 ps
- Very Low Additive Jitter < 200 fs
- Supply Voltage: 3.3 V, 2.5 V or 1.8 V
- f<sub>max</sub> = 250 MHz for 3.3 V; f<sub>max</sub> = 180 MHz for 2.5 V; f<sub>max</sub> = 133 MHz for 1.8 V
- These Devices are Pb-Free and are RoHS Compliant

# BLOCK DIAGRAM







TSSOP-8 DT SUFFIX CASE 948S

TSSOP-16 DT SUFFIX CASE 948F

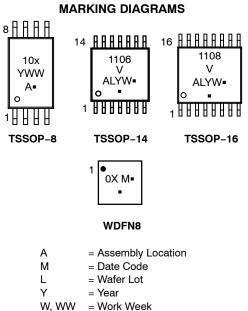


TSSOP-14

DT SUFFIX

CASE 948G

WDFN8, 2x2 MT SUFFIX CASE 511AT

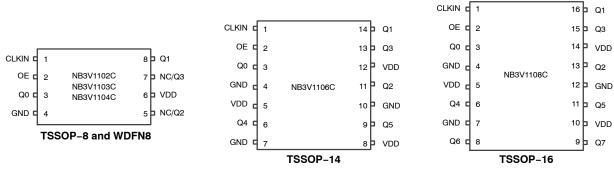


= Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 9 of this data sheet.





# Table 1. PIN DESCRIPTION

	LVCMOS Clock Input	LVCMOS Clock Output Enable	LVCMOS Clock Output	Device Supply Voltage	Device Ground
Devices	CLKIN	OE	Q0, Q1, Q7	Vdd	GND
NB3V1102C	1	2	3, 8	6	4
NB3V1103C	1	2	3, 8, 5	6	4
NB3V1104C	1	2	3, 8, 5, 7	6	4
NB3V1106C	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
NB3V1108C	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12

NOTE: Pins not mentioned in the table are NC.

# Table 2. OUTPUT LOGIC TABLE

INP	UTS	OUTPUTS
CLKIN	OE	Qn
Х	L	L
L	Н	L
Н	Н	Н

# Table 3. ATTRIBUTES

	Characteristic	Value	Unit
ESD Protection	Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001-2014 Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS-002-2014		V V
Moisture Sensitivity, Ir	definite Time Out of Dry Pack (Note 1)	Level 1	-
Meets or exceeds JEE	DEC Spec JESD78D (LU) IC Latchup Test		

1. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm<sup>2</sup>, 2 oz.)

# Table 4. ABSOLUTE MAXIMUM RATINGS (Note 2) Over operating free-air temperature range (unless otherwise noted)

Symbol	Condition		Value	Unit
$V_{DD}$	Supply Voltage Range		–0.5 to 4.6	V
V <sub>IN</sub>	Input Voltage Range (Note 3)		–0.5 to V <sub>DD</sub> + 0.5	V
Vo	Output Voltage Range (Note 3)		–0.5 to V <sub>DD</sub> + 0.5	V
I <sub>IN</sub>	Input Current		±20	mA
Ι <sub>Ο</sub>	Continuous Output Current		±50	mA
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	TSSOP-8	151.2*	°C/W
		TSSOP-14	104*	
		T000D 40	32*	
		TSSOP-16	110**	
		WDFN8	190**	
θJC	Thermal Resistance (Junction-to-Case top)	TSSOP-8	35	°C/W
		TSSOP-14	8.6	
		TSSOP-16	10	
		WDFN8	10	1
TJ	Maximum Junction Temperature	•	125	°C
T <sub>STG</sub>	Storage Temperature Range		-65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with a large copper heat spreader (20 mm<sup>2</sup>, 2 oz.)
3. For additional information, see Application Note AND8003/D.
\*JEDEC51.7 four layer PCB with 100 sqmm, 2 oz with two 80x80x1oz ground planes.

\*\*JEDEC51.3 two layer PCB with 100 sqmm, 2 oz.

### Table 5. RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Conditio	on	Min	Тур	Max	Unit
$V_{\text{DD}}$	Supply voltage range	3.3 V supply	3.0	3.3	3.6	V
		2.5 V supply	2.3	2.5	2.7	
		1.8 V supply	1.71	1.8	1.89	
V <sub>IL</sub>	Low-level input voltage	$V_{DD}$ = 3.0 V to 3.6 V			$V_{DD}/2 - 600$	mV
		$V_{DD}$ = 2.3 V to 2.7 V			$\frac{V_{\text{DD}}/2}{400} -$	
		V <sub>DD</sub> = 1.71 V to 1.89 V			$0.3 \mathrm{xV}_{\mathrm{DD}}$	V
V <sub>IH</sub>	High-level input voltage	$V_{DD}$ = 3.0 V to 3.6 V	V <sub>DD</sub> /2 + 600			mV
		$V_{DD}$ = 2.3 V to 2.7 V	V <sub>DD</sub> /2 + 400			
		V <sub>DD</sub> = 1.71 V to 1.89 V	$0.7 \mathrm{xV}_{\mathrm{DD}}$			V
$V_{\text{th}}$	Input threshold voltage	V <sub>DD</sub> = 2.3 V to 3.6 V		$V_{DD}/2$	1	V
		V <sub>DD</sub> = 1.71 V to 1.89 V		$V_{DD}/2$		V
t <sub>r</sub> / t <sub>f</sub>	Input slew rate (Note 4)		1		4	V/n
t <sub>w</sub>	Minimum pulse width at CLKIN	V <sub>DD</sub> = 3.0 V to 3.6 V	1.8			ns
		V <sub>DD</sub> = 2.3 V to 2.7 V	2.75			
		V <sub>DD</sub> = 1.71 V to 1.89 V	3.75			
fclk	LVCMOS clock Input Frequency	V <sub>DD</sub> = 3.0 V to 3.6 V	DC		250	MH
		V <sub>DD</sub> = 2.3 V to 2.7 V	DC		180	
		V <sub>DD</sub> = 1.71 V to 1.89 V	DC		133	
T <sub>A</sub>	Operating free-air temperature	•	-40		105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Guaranteed by Design.

Table 6. DEVICE CHARACTERISTICS Over recommended operating free-air temperature range (unless otherwise noted) (I
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Symbol	Parameter	Condition	Min	Тур	Max	Unit
VERALL F	PARAMETERS FOR ALL VERSIONS					
I <sub>DD</sub>	Static device current	OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 3.6 V			0.2	mA
		OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 2.7 V			0.2	
		OE = V <sub>DD</sub> ; CLKIN = 0 V or V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; V <sub>DD</sub> = 1.89 V			0.2	
I <sub>PD</sub>	Power down current	OE = 0 V; CLKIN = 0 V or $V_{DD}$ ; $I_0$ = 0 mA; $V_{DD}$ = 3.6 V, 2.7 V or 1.89 V (For 1102C, 1103C, 1104C)			60	μA
		OE = 0 V; CLKIN = 0 V or $V_{DD}$ ; $I_0$ = 0 mA; $V_{DD}$ = 3.6 V, 2.7 V or 1.89 V (For 1106C, 1108C)			75	
C <sub>PD</sub>	Power dissipation capacitance per out-	V <sub>DD</sub> = 3.3 V; f = 10 MHz		9		pF
	put (Note 6)	V <sub>DD</sub> = 2.5 V; f = 10 MHz		9		1
		V <sub>DD</sub> = 1.8 V; f = 10 MHz		9		
Ц	Input leakage current at OE	$V_{I} = 0 \text{ V or } V_{DD}, V_{DD} = 3.6 \text{ V or } 2.7 \text{ V}$		± 8	± 8	μA
	Input leakage current at CLKIN	1		1	± 8	
	Input leakage current at OE, CLKIN	$V_{I} = 0 \text{ V or } V_{DD}, V_{DD} = 1.89 \text{ V}$			± 8	
R <sub>OUT</sub>	Output impedance	V <sub>DD</sub> = 3.3 V		40		Ω
		V <sub>DD</sub> = 2.5 V		45		
		V <sub>DD</sub> = 1.8 V		60		
f <sub>OUT</sub>	Output frequency	V <sub>DD</sub> = 3.0 V to 3.6 V	DC		250	MH
		V <sub>DD</sub> = 2.3 V to 2.7 V	DC		180	
		V <sub>DD</sub> = 1.71 V to 1.89 V	DC		133	
	RAMETERS FOR $V_{DD}$ = 3.3 V ± 0.3 V					
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -0.1 mA	2.9			V
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -8 mA	2.5			
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -12 mA	2.2			
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 0.1 mA			0.1	V
		V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 8 mA			0.5	
				1	1	1

		$v_{DD} = 3 v, i_{OL} = 0 i_{DA}$		0.5	
		V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 12 mA		0.8	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay (Note 7)	CLKIN to Qn	0.8	2.0	ns
t <sub>sk(o)</sub>	Output skew (Note 7)	Equal load of each output 85°C		50	ps
		Equal load of each output 105°C		60	
t <sub>r</sub> /t <sub>f</sub>	Rise and fall time	20%–80% (V <sub>OH</sub> – V <sub>OL</sub> )	0.12	0.8	ns
t <sub>DIS</sub>	Output disable time (Note 7)	OE to Qn		6	ns
t <sub>EN</sub>	Output enable time (Note 7)	OE to Qn		6	ns
t <sub>sk(p)</sub>	Pulse skew; tPLH(Qn) - tPHL(Qn) (Note 8)	To be measured with input duty cycle of 50%		180	ps
t <sub>sk(pp)</sub>	Part-to-part skew	Under equal operating conditions for two parts		0.5	ns
Τ <sub>jit(φ)</sub>	Additive jitter rms	12 kHz20 MHz f <sub>OUT</sub> = 100 MHz		100	fs
		12 kHz20 MHz f <sub>OUT</sub> = 156.25 MHz			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. All typical values are at respective nominal  $V_{DD}$ . For switching characteristics, outputs are terminated to 50  $\Omega$  to  $V_{DD}/2$  (see Figure 2). 6. This is the formula for the power dissipation calculation. Ptot = Pstat + Pdyn + PCload [W] P<sub>stat</sub> = V<sub>DD</sub> x I<sub>DD</sub> [W] P<sub>dyn</sub> = C<sub>PD</sub> x V<sub>DD</sub>2 x f x n [W] P<sub>Cload</sub> = C<sub>load</sub> x V<sub>DD</sub>2 x f x n [W] n = Number of switching output pins 7. With rail to rail input clock

7. With rail to rail input clock.

8.  $t_{sk(p)}$  depends on output rise- and fall-time ( $t_{r}/t_{f}$ ). The output duty-cycle can be calculated: odc = ( $t_{w(OUT)} \pm t_{sk(p)}$ )/ $t_{period}$ ;  $t_{w(OUT)}$  is pulse-width of ideal output waveform and tperiod is 1/ $f_{OUT}$ .

### NB3V1102CMTTBG onsemi IC CLK BUFFER 1:2 250MHZ 8WDFN

# NB3V110xC Series

#### Table 7. DEVICE CHARACTERISTICS (continued)

Over recommended operating free-air temperature range (unless otherwise noted) (Note 5)

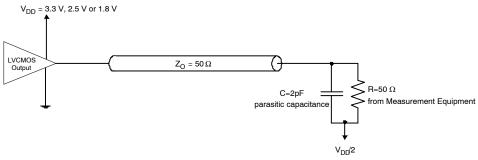
OR V <sub>DD</sub> = 2.5 V ± 0.2 tput voltage put voltage lelay (Note 10) Note 10) ime	$\frac{2 V}{V_{DD} = 2.3 V, I_{OH} = -0.1 mA}$ $\frac{V_{DD} = 2.3 V, I_{OH} = -8 mA}{V_{DD} = 2.3 V, I_{OL} = 0.1 mA}$ $\frac{V_{DD} = 2.3 V, I_{OL} = 8 mA}{V_{DD} = 2.3 V, I_{OL} = 8 mA}$ CLKIN to Qn Equal load of each output 85°C Equal load of each output 105°C 20%-80% (V_{OH} - V_{OL})	0.12	1.8	0.1 0.5 50 60	V V ns ps
put voltage lelay (Note 10) Note 10)	$V_{DD} = 2.3 \text{ V}, I_{OH} = -8 \text{ mA}$ $V_{DD} = 2.3 \text{ V}, I_{OL} = 0.1 \text{ mA}$ $V_{DD} = 2.3 \text{ V}, I_{OL} = 8 \text{ mA}$ $CLKIN \text{ to } Qn$ Equal load of each output 85°C Equal load of each output 105°C	1.7	1.8	0.5 50 60	V
ielay (Note 10) Note 10)	$V_{DD} = 2.3 \text{ V}, I_{OL} = 0.1 \text{ mA}$ $V_{DD} = 2.3 \text{ V}, I_{OL} = 8 \text{ mA}$ $CLKIN \text{ to } Qn$ Equal load of each output 85°C Equal load of each output 105°C		1.8	0.5 50 60	ns
ielay (Note 10) Note 10)	$V_{DD} = 2.3 \text{ V}, I_{OL} = 8 \text{ mA}$ CLKIN to Qn Equal load of each output 85°C Equal load of each output 105°C	0.12	1.8	0.5 50 60	ns
Note 10)	CLKIN to Qn Equal load of each output 85°C Equal load of each output 105°C	0.12	1.8	50 60	
Note 10)	Equal load of each output 85°C Equal load of each output 105°C	0.12	1.8	60	
ime	Equal load of each output 105°C	0.12		60	ps
		0.12			
	20%–80% (V <sub>OH</sub> – V <sub>OL</sub> )	0.12			
e time (Note 10)				1.2	ns
( /	OE to Qn			10	ns
e time (Note 10)	OE to Qn			10	ns
PLH(Qn) — tPHL(Qn)	To be measured with input duty cycle of 50%			220	ps
kew	Under equal operating conditions for two parts			1.2	ns
rms	12 kHz20 MHz f <sub>OUT</sub> = 100 MHz			150	fs
	12 kHz20 MHz f <sub>OUT</sub> = 156.25 MHz		1	100	1
s	skew	skew Under equal operating conditions for two parts rms 12 kHz20 MHz f <sub>OUT</sub> = 100 MHz 12 kHz20 MHz f <sub>OUT</sub> = 156.25 MHz	skew Under equal operating conditions for two parts rms 12 kHz20 MHz f <sub>OUT</sub> = 100 MHz 12 kHz20 MHz f <sub>OUT</sub> = 156.25 MHz	skew     Under equal operating conditions for two parts       rms     12 kHz20 MHz f <sub>OUT</sub> = 100 MHz	skewUnder equal operating conditions for two parts1.2rms12 kHz20 MHz f <sub>OUT</sub> = 100 MHz15012 kHz20 MHz f <sub>OUT</sub> = 156.25 MHz100

V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 1.71 V, I <sub>OH</sub> = -0.1 mA	1.6		V
		$V_{DD} = 1.71 \text{ V}, I_{OH} = -4 \text{ mA}$	0.75xV <sub>DD</sub>		
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 1.71 V, I <sub>OL</sub> = 0.1 mA		0.1	V
		V <sub>DD</sub> = 1.71 V, I <sub>OL</sub> = 4 mA		0.25xV <sub>DD</sub>	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay (Note 10)	CLKIN to Qn	1.8	3.5	ns
t <sub>sk(o)</sub>	Output skew (Note 10)	Equal load of each output		75	ps
t <sub>r</sub> /t <sub>f</sub>	Rise and fall time	20%–80% (V <sub>OH</sub> – V <sub>OL</sub> )	0.17	1.2	ns
t <sub>DIS</sub>	Output disable time (Note 10)	OE to Qn		10	ns
t <sub>EN</sub>	Output enable time (Note 10)	OE to Qn		10	ns
t <sub>sk(p)</sub>	Pulse skew ; <sup>t</sup> PLH(Qn) - tPHL(Qn) (Note 9)	To be measured with input duty cycle of 50%		450	ps
t <sub>sk(pp)</sub>	Part-to-part skew	Under equal operating conditions for two parts		1.2	ns
tjit <sub>(φ)</sub>	Additive jitter rms	12 kHz20 MHz, f <sub>OUT</sub> = 100 MHz		200	fs

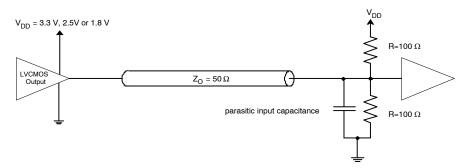
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 9.  $t_{sk(p)}$  depends on output rise- and fall-time ( $t_r/t_f$ ). The output duty-cycle can be calculated: odc = ( $t_{w(OUT)} \pm t_{sk(p)}$ )/ $t_{period}$ ;  $t_{w(OUT)}$  is

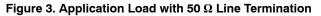
pulse-width of ideal output waveform and tperiod is 1/f<sub>OUT</sub>. 10. With rail to rail input clock.

# PARAMETERS MEASUREMENT INFORMATION









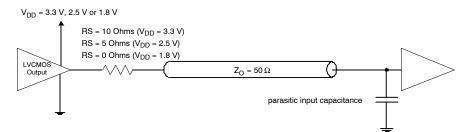


Figure 4. Application Load with Series Line Termination

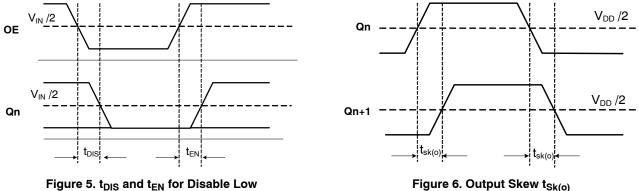
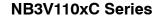
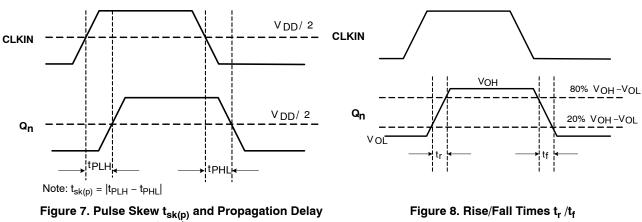
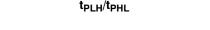
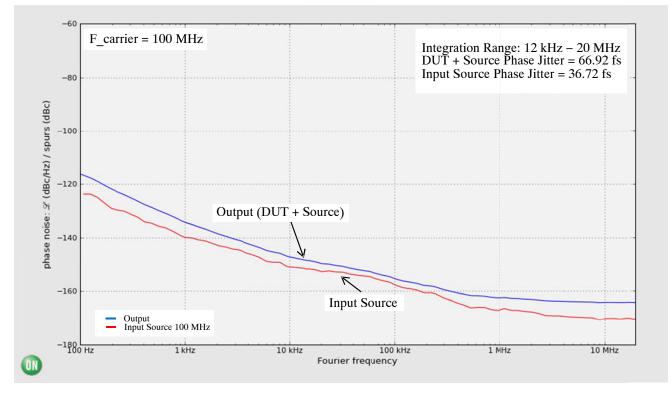


Figure 6. Output Skew t<sub>Sk(o)</sub>









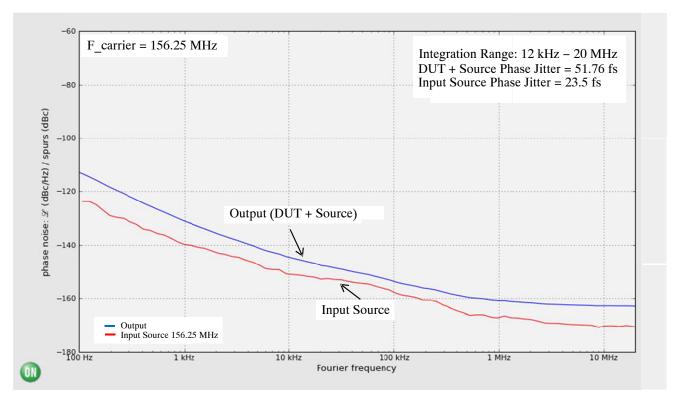


The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 55.94 fs. The additive RMS phase jitter performance of the fan out buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB3V110xC source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 55.94 fs.

Additive RMS phase jitter =  $\sqrt{\text{RMS}}$  phase jitter of output<sup>2</sup> – RMS phase jitter of input<sup>2</sup>

55.94 fs =  $\sqrt{66.92 \text{ fs}^2 - 36.72 \text{ fs}^2}$ 



# Figure 10. Typical NB3V110xC Phase Noise Plot at f<sub>Carrier</sub> = 156.25 MHz, V<sub>CC</sub> = 3.3 V V, 25°C

The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 46.11 fs.

Additive RMS phase jitter =  $\sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$ 

46.11 fs = 
$$\sqrt{51.76 \text{ fs}^2 - 23.5 \text{ fs}^2}$$

Figures 9 and 10 were created with measured data from Agilent–E5052A/B Signal Source Analyzer using **onsemi** Phase Noise Explorer web tool. This free application enables an interactive environment for advanced phase noise and jitter analysis of timing devices and clock tree designs. To see the performance of NB3V110xC beyond conditions outlined in this datasheet, please visit the **onsemi** Green Point Design Tools homepage.

Device	Marking	Package	Shipping <sup>†</sup>
NB3V1102CDTR2G	102	TSSOP-8 (Pb-Free) 2500 / Tape & Reel	
NB3V1103CDTR2G	103		2500 / Tape & Reel
NB3V1104CDTR2G	104		
NB3V1102CMTTBG	02	WDFN8	
NB3V1104CMTTBG	04	(Pb-Free) 30	3000 / Tape & Reel
NB3V1106CDTR2G	1106 V	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NB3V1108CDTR2G	1108 V	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

# Table 8. ORDERING INFORMATION

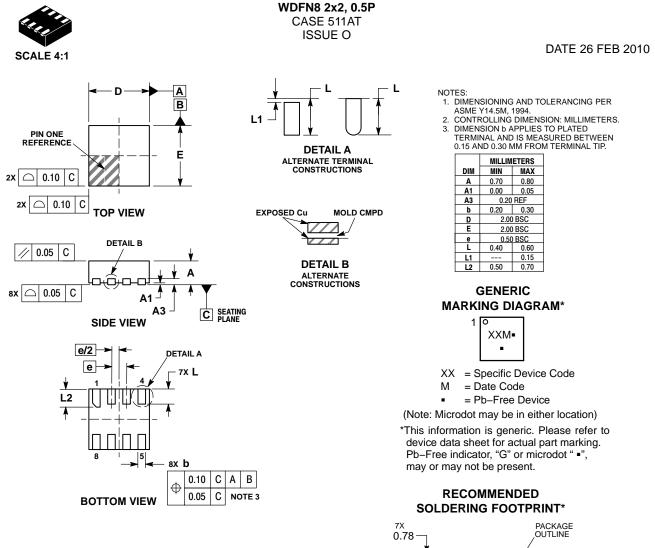
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.

NOTE: Please contact your onsemi sales representative for availability of parts in tube.



# **MECHANICAL CASE OUTLINE**

PACKAGE DIMENSIONS



2.30 0.88 0.50 8X 0.30 PITCH DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WDFN8, 2X2, 0.5 P		PAGE 1 OF 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

**TSSOP-16 WB** CASE 948F **ISSUE B** DATE 19 OCT 2006 SCALE 2:1 16X K REF NOTES  $\oplus$ 0.10 (0.004) 🔘 T U 🕥 V 🕥 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER. υs 0.15 (0.006) T κ 2 З. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. **K1** MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. 2X L/2 J1 4. INTERLEAD FLASH OR PROTRUSION SHALL INTERLEAD FLASH OF PHOTHOSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. TERMINAL INTIMEER ADE OLIVINI ECO. SECTION N-N В 5. L -U-PIN 1 IDENT. N TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 0.25 (0.010) 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-. 7. ○ 0.15 (0.006) υs Т MILLIMETERS INCHES Α DIN MIN MAX MIN MAX -V-Α 4.90 5.10 0.193 0.200 F в 4.30 4.50 0.169 0.177 С 1.20 0.047 0.15 0.002 D 0.05 0.006 DETAIL E F 0.50 0.75 0.020 0.030 G 0.65 BSC 0.026 BSC н 0.18 0.28 0.007 0.011 -W– 0.09 0.20 0.004 0.008 J С J1 K 
 0.09
 0.16
 0.004
 0.006

 0.19
 0.30
 0.007
 0.012
 ○ 0.10 (0.004) K1 0.19 0.25 0.007 0.010 DETAIL E 6.40 BSC н L 0.252 BSC SEATING -T-D 0 ° 8 0 ° G 8 GENERIC RECOMMENDED **MARKING DIAGRAM\*** SOLDERING FOOTPRINT\* 16AAAAAAAA 7.06 XXXX XXXX ٦ 1 o ALYW 1 888888888 = Specific Device Code XXXX = Assembly Location A = Wafer Lot L Υ = Year W = Work Week 0.65

G or = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

16X

1.26

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DIMENSIONS: MILLIMETERS

PITCH

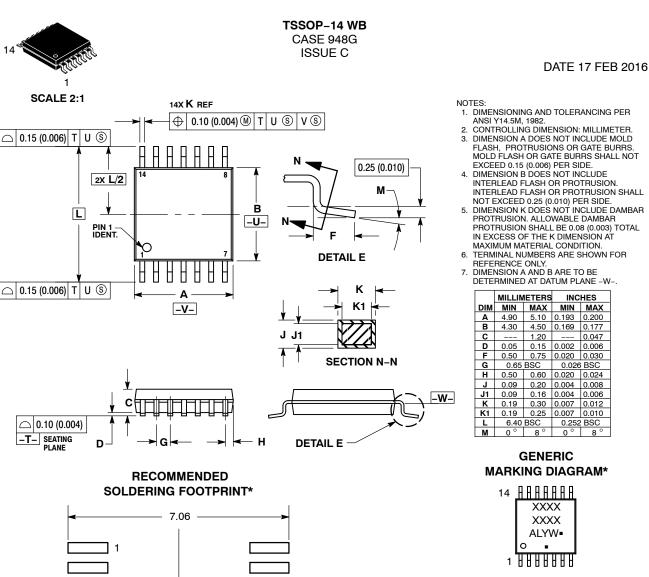
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16X

0.36



**MECHANICAL CASE OUTLINE** PACKAGE DIMENSIONS



= Assembly Location Α = Wafer Lot L Υ = Year = Work Week w/

= Pb-Free Package

(Note: Microdot may be in either location) \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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0.65

DIMENSIONS: MILLIMETERS

PITCH

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1 14X 0.36

14X

1.26

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**MECHANICAL CASE OUTLINE** 

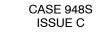
PACKAGE DIMENSIONS



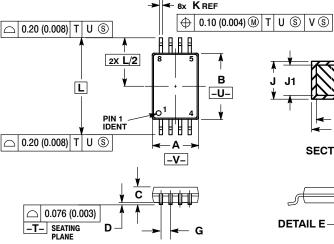
TSSOP-8 3.0x4.4x1.1 CASE 948S **ISSUE C** 

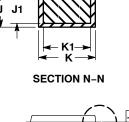
**DATE 20 JUN 2008** 

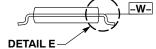


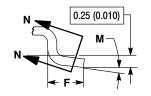












DETAIL E

NOTES:

- IOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE. 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
- PER SIDE. 5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY. DIMENSION A AND B ARE TO BE DETERMINED 6.
- AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
С		1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0°	8°	0°	8 °

#### GENERIC **MARKING DIAGRAM\***

0	XXX
	YWW
	A •
	•

XXX	= Specific Device Code
Α	= Assembly Location
Y	= Year
WW	= Work Week
	= Pb-Free Package

= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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