NC7SV58L6X Datasheet

DiGi Electronics Part Number	NC7SV58L6X-DG
Manufacturer	onsemi
Manufacturer Product Number	NC7SV58L6X
Description	IC GATE ULP-A UNIV 2INP 6-MCRPAK
Detailed Description	Configurable Multiple Function Configurable 1 Circuit 3 Input 6-MicroPak

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NC7SV58L6X	onsemi
Series:	Product Status:
7SV	Obsolete
Logic Type:	Number of Circuits:
Configurable Multiple Function	1
Number of Inputs:	Schmitt Trigger Input:
3	No
Output Type:	Current - Output High, Low:
Single-Ended	24mA, 24mA
Voltage - Supply:	Operating Temperature:
0.9V ~ 3.6V	-40°C ~ 85°C
Mounting Type:	Package / Case:
Surface Mount	6-UFDFN
Supplier Device Package:	Base Product Number:
6-MicroPak	7SV58

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

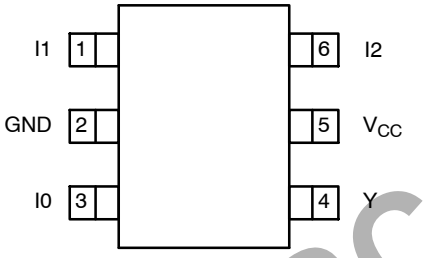
TinyLogic ULP-A Universal Configurable Logic Gates

NC7SV57, NC7SV58

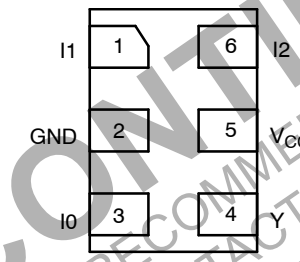
The NC7SV57 and NC7SV58 are universal configurable logic gates in tiny footprint packages. The devices are designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 2.4 ns t_{PD} at 3.3 V (Typ)
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.3 V
- Available in SC−88 and MicroPak™ Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



SC−88



MicroPak

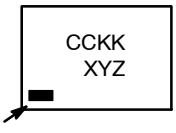
Figure 1. Pinout Diagrams (Top Views)

PIN ASSIGNMENT

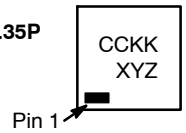
Pin	SC−88	MicroPak
1	I1	I1
2	GND	GND
3	I0	I0
4	Y	Y
5	V_{CC}	V_{CC}
6	I2	I2

MARKING DIAGRAM

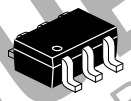
SIP6 1.45X1.0 MicroPak CASE 127EB



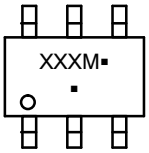
UDFN6 1.0X1.0, 0.35P MicroPak2™ CASE 517DP



CC = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code
Z = Assembly Plant Code



SC−88 CASE 419AD



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

FUNCTION TABLE

Inputs			NC7SV57	NC7SV58
I2	I1	I0	$Y = (\overline{I0}) \bullet (\overline{I2}) + (I1) \bullet (I2)$	$Y = (I0) \bullet (\overline{I2}) + (\overline{I1}) \bullet (I2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

FUNCTION SELECTION TABLE

2−Input Logic Function	Device Selection	Connection Configuration
2−Input AND	NC7SV57	Figure 2
2−Input AND with inverted input	NC7SV58	Figure 8, 9
2−Input AND with both inputs inverted	NC7SV57	Figure 5
2−Input NAND	NC7SV58	Figure 7
2−Input NAND with inverted input	NC7SV57	Figure 3, 4
2−Input NAND with both inputs inverted	NC7SV58	Figure 10
2−Input OR	NC7SV58	Figure 10
2−Input OR with inverted input	NC7SV57	Figure 3, 4
2−Input OR with both inputs inverted	NC7SV58	Figure 7
2−Input NOR	NC7SV57	Figure 5
2−Input NOR with inverted input	NC7SV58	Figure 8, 9
2−Input NOR with both inputs inverted	NC7SV57	Figure 2
2−Input XOR	NC7SV58	Figure 11
2−Input XNOR	NC7SV57	Figure 6

Logic Configurations NC7SV57

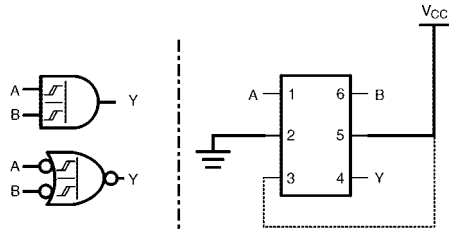


Figure 2. 2−Input AND Gate

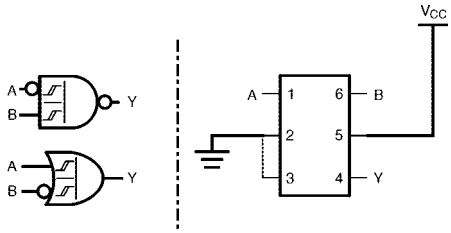


Figure 3. 2−Input NAND with Inverted A Input

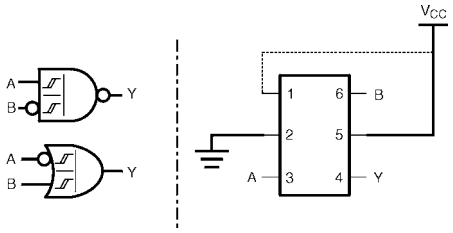


Figure 4. 2−Input NAND with Inverted B Input

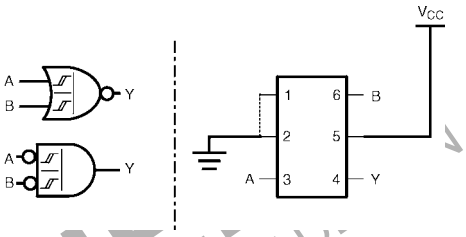


Figure 5. 2−Input NOR Gate

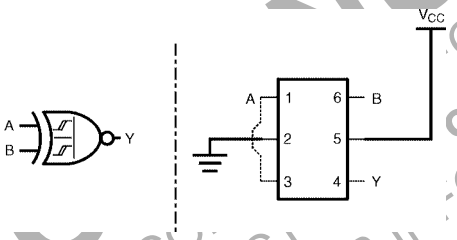


Figure 6. 2−Input XNOR Gate

NOTE: Figure 2 through Figure 6 show the logical functions that can be implemented using the NC7SV57. The diagrams show the DeMorgan's equivalent logic duals for a given 2−input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

Logic Configurations NC7SV58

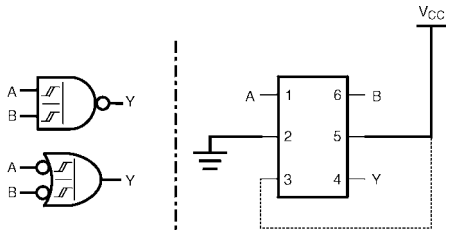


Figure 7. 2−Input NAND Gate

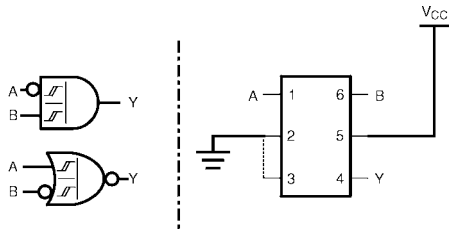


Figure 8. 2−Input AND with Inverted A Input

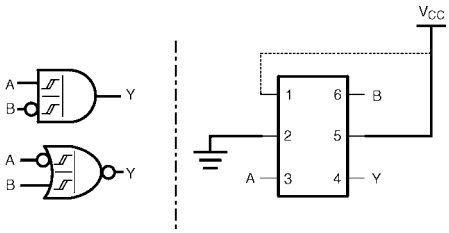


Figure 9. 2−Input AND with Inverted B Input

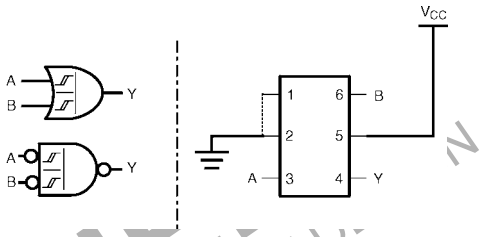


Figure 10. 2−Input OR Gate

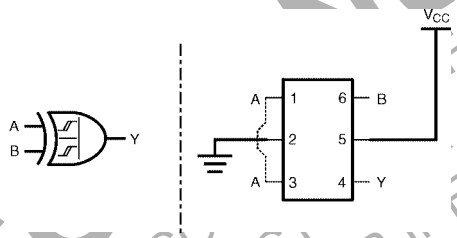


Figure 11. 2−Input XOR Gate

NOTE: Figure 7 through Figure 11 show the logical functions that can be implemented using the NC7SV58. The diagrams show the DeMorgan's equivalent logic duals for a given 2−input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +4.3	V
V_{IN}	DC Input Voltage	−0.5 to +4.3	V
V_{OUT}	DC Output Voltage Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current	±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SC−88 MicroPak	377 154	°C/W
P_D	Power Dissipation in Still Air SC−88 MicroPak	332 812	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	0.9	3.6	V
V_{IN}	DC Input Voltage	0	3.6	V
V_{OUT}	DC Output Voltage Active−Mode (High or Low State) Tri−State Mode (Note 5) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	V
T_A	Operating Temperature Range	−40	+85	°C
t_r , t_f	Input Transition Rise and Fall Time	0	No Limit	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Applicable to devices with outputs that may be tri−stated.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_P	Positive Threshold Voltage		0.9	–	0.62	–	–	–	V
			1.1	–	–	1.0	–	1.0	
			1.4	–	–	1.25	–	1.25	
			1.65	–	–	1.5	–	1.5	
			2.3	–	–	1.8	–	1.8	
			2.7	–	–	2.2	–	2.2	
V_N	Negative Threshold Voltage		0.9	–	0.34	–	–	–	V
			1.1	0.15	–	–	0.15	–	
			1.4	0.2	–	–	0.2	–	
			1.65	0.25	–	–	0.25	–	
			2.3	0.4	–	–	0.4	–	
			2.7	0.6	–	–	0.6	–	
V_H	Hysteresis Voltage		0.9	–	0.29	–	–	–	V
			1.1	0.08	–	0.6	0.08	0.6	
			1.4	0.09	–	0.8	0.09	0.8	
			1.65	0.15	–	1.0	0.15	1.0	
			2.3	0.25	–	1.1	0.25	1.1	
			2.7	0.6	–	1.2	0.6	1.2	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −100 μA	0.9		V_{CC} − 0.1	–	–	–	
			1.1 to 1.3	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.4 to 1.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.65 to 1.95	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
			2.3 to <2.7	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
			2.7 to 3.6	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
		I_{OH} = −2 mA	1.1 o 1.3	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −4 mA	1.4 to 1.6	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −6 mA	1.65 to 1.95	1.25	–	–	1.25	–	
			2.3 to <2.7	2.0	–	–	2.0	–	
		I_{OH} = −12 mA	2.3 to <2.7	1.8	–	–	1.8	–	
			2.7 to 3.6	2.2	–	–	2.2	–	
		I_{OH} = −18 mA	2.3 to <2.7	1.7	–	–	1.7	–	
			2.7 to 3.6	2.4	–	–	2.4	–	
		I_{OH} = −24 mA	2.7 to 3.6	2.2	–	–	2.2	–	

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OL} = 100 μA	0.9	–	0.1	–	–	–	
			1.1 to 1.3	–	–	0.1	–	0.1	
			1.4 to 1.6	–	–	0.1	–	0.1	
			1.65 to 1.95	–	–	0.2	–	0.2	
			2.3 to < 2.7	–	–	0.2	–	0.2	
			2.7 to 3.6	–	–	0.2	–	0.2	
		I_{OL} = 2 mA	1.1 o 1.3	–	–	0.25 x V_{CC}	–	0.25 x V_{CC}	
		I_{OL} = 4 mA	1.4 to 1.6	–	–	0.25 x V_{CC}	–	0.25 x V_{CC}	
		I_{OL} = 6 mA	1.65 to 1.95	–	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.3 to <2.7	–	–	0.4	–	0.4	
			2.7 to 3.6	–	–	0.4	–	0.4	
		I_{OL} = 18 mA	2.3 to <2.7	–	–	0.6	–	0.6	
			2.7 to 3.6	–	–	0.4	–	0.4	
		I_{OL} = 24 mA	2.7 to 3.6	–	–	0.55	–	0.55	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±0.5	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V or V_{OUT} = 0 V to 3.6 V	0	–	–	0.5	–	0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	0.9 to 3.6	–	–	0.9	–	0.9	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

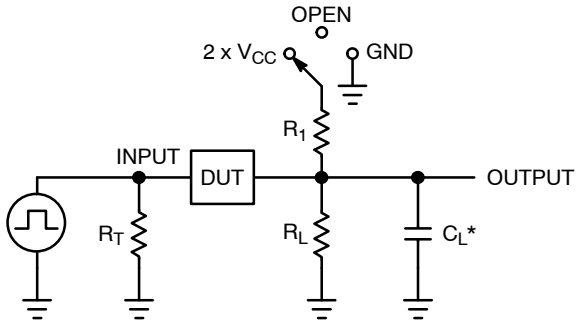
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (I0 or I1 or I2) to Y (Figures 12 and 13)	R_L = 1 MΩ, C_L = 15 pF	0.9	–	22.2	–	–	–	ns
		R_L = 2 kΩ, C_L = 15 pF	1.10 to 1.30	–	7.1	16.5	–	31.0	
			1.40 to 1.60	–	4.4	10.0	–	12.0	
		R_L = 500 Ω, C_L = 30 pF	1.65 to 1.95	–	3.7	9.1	–	10.0	
			2.3 to 2.7	–	2.9	6.2	–	6.7	
			3.0 to 3.6	–	2.4	5.4	–	6.1	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	8.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V	12	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	f = 10 MHz, V_{CC} = 0.9 to 3.6 V, V_{IN} = 0 V or V_{CC}	10	pF

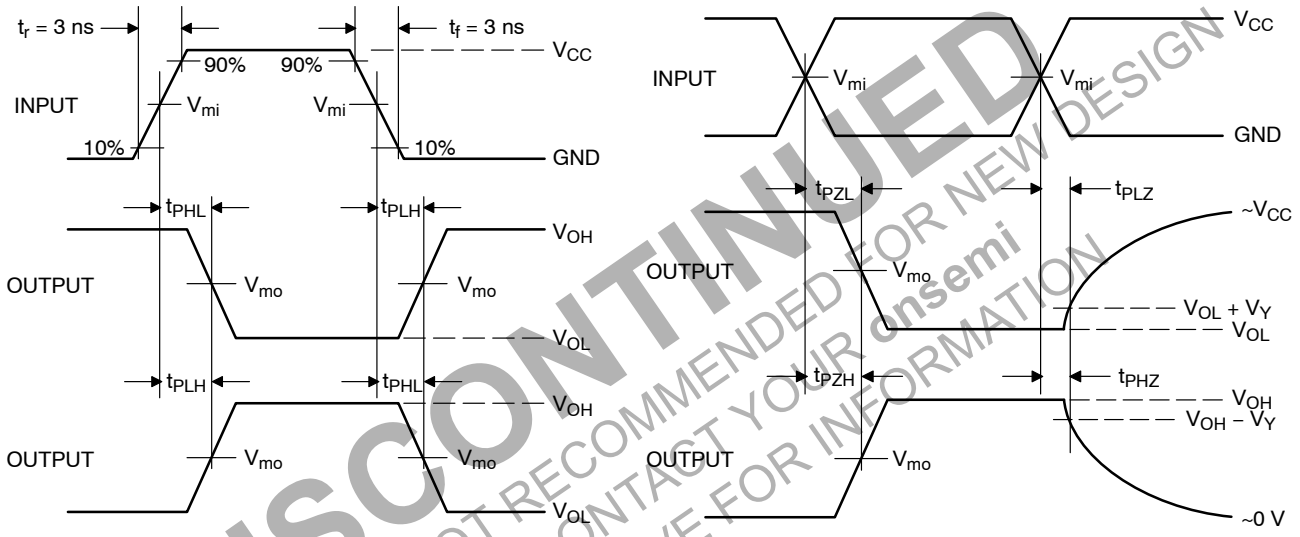
6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

Figure 12. Test Circuit



V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	V_{CC} / 2	V_{CC} / 2	0.1
1.1 to 1.3	V_{CC} / 2	V_{CC} / 2	0.1
1.4 to 1.6	V_{CC} / 2	V_{CC} / 2	0.1
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	1.5	1.5	0.3

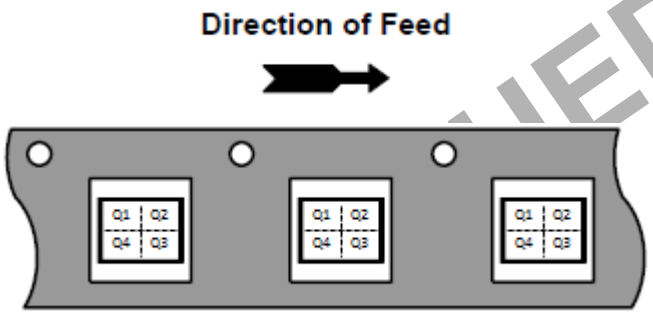
Figure 13. Switching Waveforms

ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NC7SV57P6X	SC−88	V57	Q4	3000 / Tape & Reel
NC7SV57L6X	MicroPak	H3	Q4	5000 / Tape & Reel
NC7SV57FHX	MicroPak2	H3	Q4	5000 / Tape & Reel
NC7SV57FHX−L22780	MicroPak2	H3	Q4	5000 / Tape & Reel
NC7SV58P6X	SC−88	V58	Q4	3000 / Tape & Reel
NC7SV58L6X	MicroPak	H4	Q4	5000 / Tape & Reel
NC7SV58FHX	MicroPak2	H4	Q4	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN 1 ORIENTATION IN TAPE AND REEL

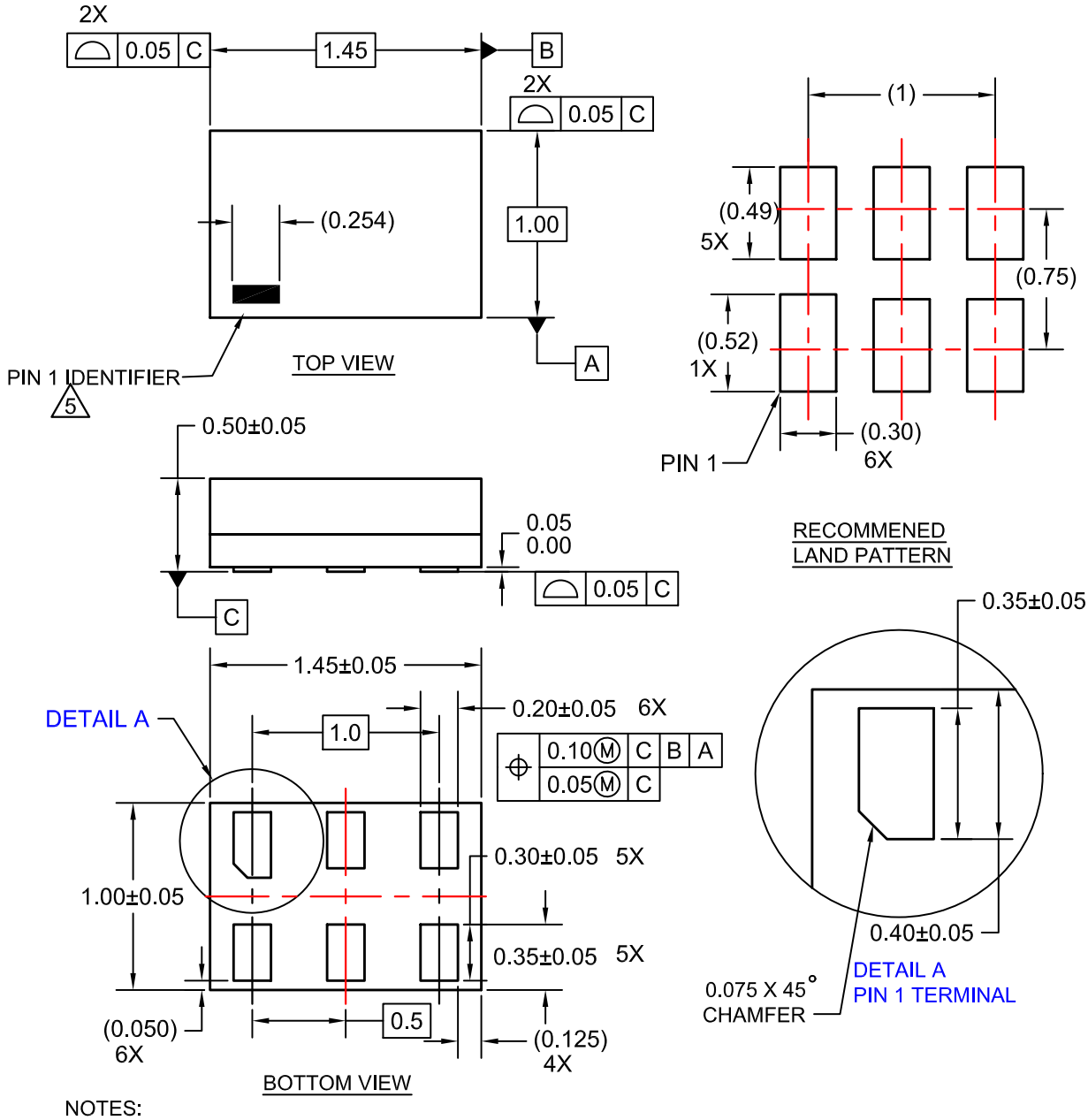


onsemi

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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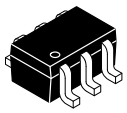
DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**

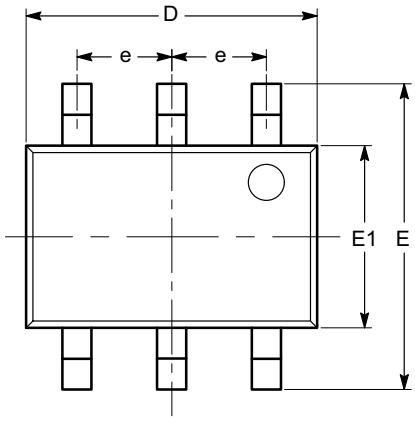
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



1

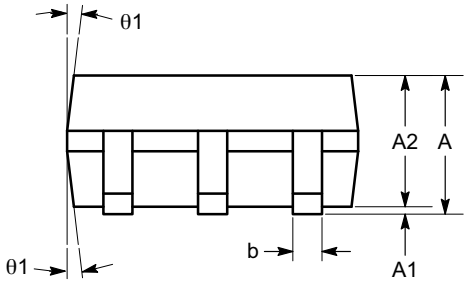
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

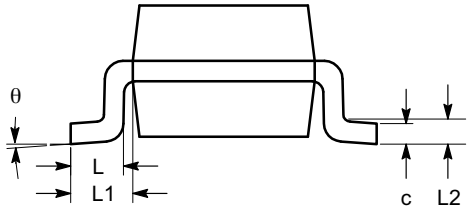


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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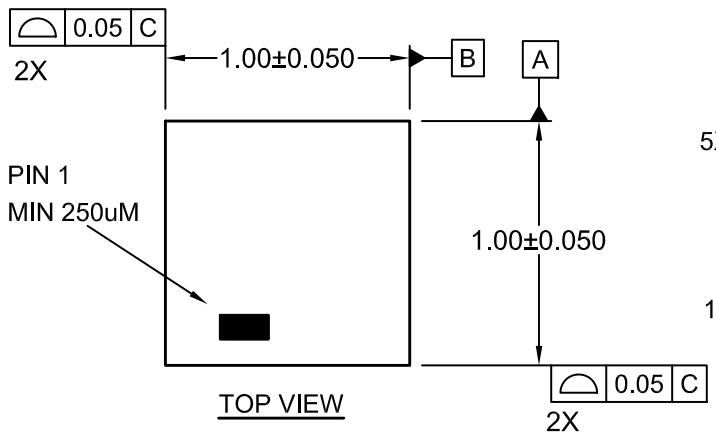
DESCRIPTION:	**SC−88 (SC−70 6 LEAD), 1.25X2**		**PAGE 1 OF 1**

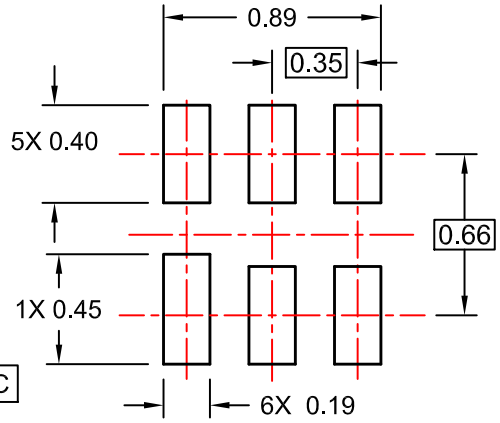
onsemi

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

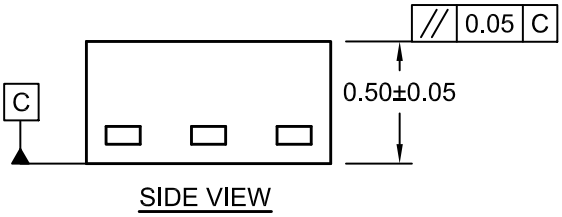
UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

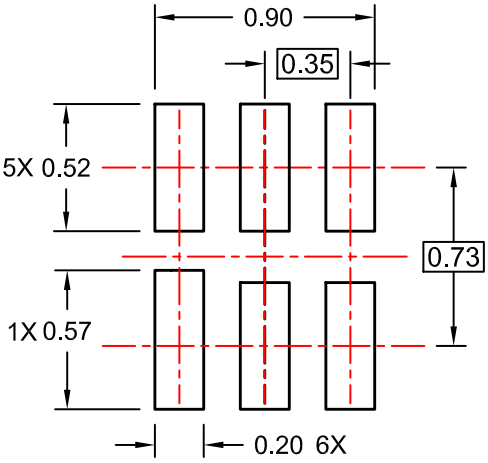
DATE 31 AUG 2016



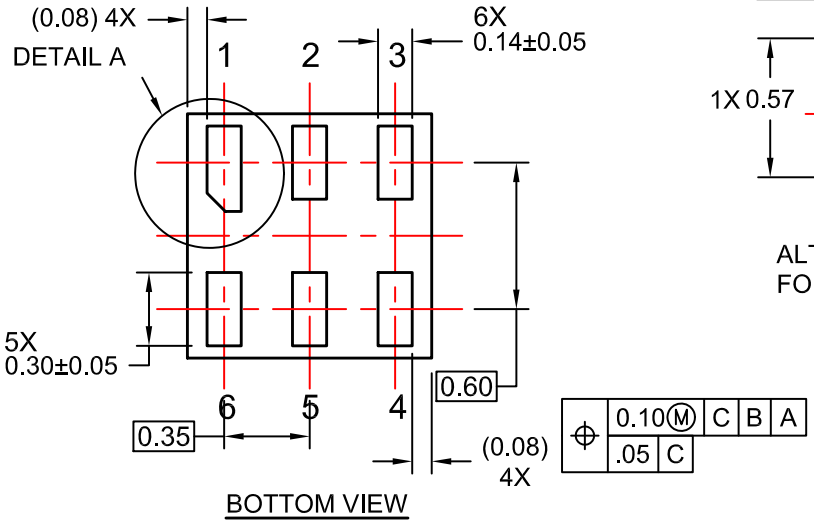


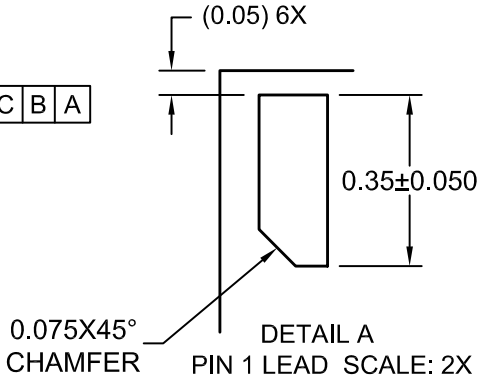
RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB





ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION





NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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DESCRIPTION:	**UDFN6 1.0X1.0, 0.35P**	**PAGE 1 OF 1**

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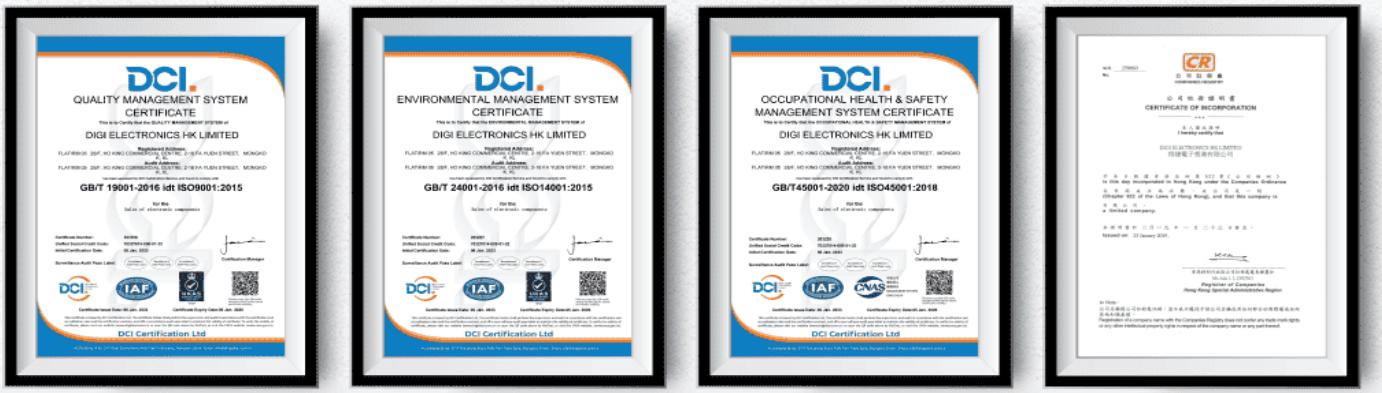

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