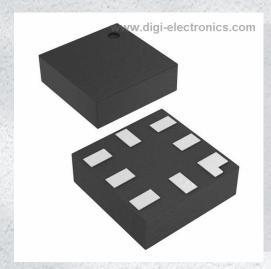


NC7WP02L8X Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number NC7WP02L8X-DG

Manufacturer onsemi

Manufacturer Product Number NC7WP02L8X

Description IC GATE NOR 2CH 2-INP 8MICROPAK

Detailed Description NOR Gate IC 2 Channel 8-MicroPak™



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NC7WP02L8X	onsemi
Series:	Product Status:
7WP	Obsolete
Logic Type:	Number of Circuits:
NOR Gate	2
Number of Inputs:	Features:
2	
Voltage - Supply:	Current - Quiescent (Max):
0.9V ~ 3.6V	900 nA
Current - Output High, Low:	Input Logic Level - Low:
2.6mA, 2.6mA	0.7V ~ 0.9V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.6V ~ 2V	7ns @ 3.3V, 30pF
Operating Temperature:	Mounting Type:
-40°C ~ 85°C	Surface Mount
Supplier Device Package:	Package / Case:
8-MicroPak™	8-UFQFN
Base Product Number:	
7WP02	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

8542.39.0001





To It are more about QV Semiconductor, please visit our website at www.onsemi.com

Please note. As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild questions@onsemi.com.

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October 2003 Revised August 2024

NC7WP02

TinyLogic® ULP Dual 2-Input NOR Gate

General Description

The NC7WP02 is a dual 2-Input NOR Gate from Fairchild's Ultra Low Power (ULP) series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V V_{CC} .

The internal circuit is composed of a minimum of inverter stages, including the output buffer, to enable ultra low static and dynamic power.

The NC7WP02 is designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining extremely low CMOS power dissipation.

Features

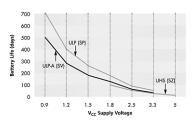
- Space saving US8 package
- Ultra small MicroPak™ Pb-Free package
- 0.9V to 3.6V V_{CC} supply operation
- 3.6V overvoltage tolerant I/O's √_{CC} fr 0.9
- 3 ns typ for 3.0V tr 3.6V V_{Cu} 4 ns typ for 2 V to VV_{CC} 5 ns tvn for 1.6 to 1. V V 1.60v V_{CC} typ 1 1.10v30V V_{CC} 24 n. o fo. 90V V_{CC}
- Power- high impedar or inputs and nor
- 'tatic Drive ('OH/IOL) 2.6 mA ⊋ 3.0℃ V_{CC} ±2.11:A @ 2.30V V_C 1.4 mA @ 1.35V V₃₀ 1.0 m ¼ @ 1.40V V_C ±0.5 mA @ 1.10\/ v cc 20 μA @ 1.9V V_{CC}
- Low note switching using design techniques of Quiet Series™ noise/EMI reduction circuitry
- Ultra low dynamic power

de..ng Code:

	Order Number	Packinge Number	Fro duct Code Top Nark	Package Description	Supplied As
	VC7WP02K8X	MAB08A	WP02	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
Ļ	NC7WP02L8X	MAC08A	Y4	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per IEP EC IS ID-020B.

Battery Life vs. V_{CC} Supply Voltage



TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly. Battery Life = $(V_{battery} *I_{battery} *.9)/(P_{device})/24hrs/day$

Where, $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$

Assumes ideal 3.6V Lithium lon battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with $C_{\rm L}$ = 15 pF load

TinyLogic® is a registered trademark, and Quiet Series™ and MicroPak™ are trademarks of Fairchild Semiconductor Corporation

C7WP02

Logic Symbol

IEEE/IEC

≥1

Y₁

Y₂

Pin Descriptions

Pin Names	Description				
A _n , B _n	Input				
Y _n	Output				

Function Table

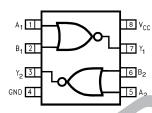
 $\boldsymbol{Y} = \overline{\boldsymbol{A} + \boldsymbol{B}}$

Inp	uts	Output
Α	В	Y
L	L	Н
L	Н	L
Н	L	L
Н	Н	

H = HIGH Logic Level

Connection Diagrams

Pin Assignments for US8



(Top View)

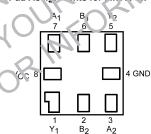
Pin One Orie ...on Dir aran.



AAA reset s Product ode fop Mark - see orsett foode

Note: Intation of rop Mark determines Product code mail: (e. to right, Pin One in this lower left pin is a diagram).

Pad Assignments for MicroPak



(Top Through View)

0.9V to 3.6V

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions (Note 3)

Supply Voltage

Supply Voltage (V _{CC})	-0.5V to $+4.6V$
DC Input Voltage (V _{IN})	-0.5V to +4.6V
DC Output Voltage (V _{OUT})	
HIGH or LOW State (Note 2)	$-0.5V$ to V_{CC} +0.5V
$V_{CC} = 0V$	-0.5V to 4.6V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	±50 mA
DC Output Diode Current (I _{OK})	
$V_{OUT} > 0V$	−50 mA
$V_{OUT} < V_{CC}$	+50 mA

 $V_{OUT} < V_{CC}$ +50 mA

DC Output Source/Sink Current (I_{OH}/I_{OL}) ± 50 mA

DC V_{CC} or Ground Current per

Supply Pin (I_{CC} or Ground) ± 50 mA

Storage Temperature Range (T_{STG}) -65°C to +150°C

Free Air Operating Temperatur (T_A) J°C to +85°C

Minimum Inpu' \bar{dg} te ($\Delta t/\Delta$ V_{IN} = 0.8V to . V, V_L = 3.0'

V, V_C = 3.0'

Note 1: A. The property of the safe of the set of the s

9 2: I_O Absolute Maximum Rating must be ob encod

No : Unused in, un must be held HIGH o. 10W. They may not float.

DC Electrical Characteric

Symbol	Parameter	V _{CC}	T _A = +25	Max	T _A = -40°C	` ₁o +85°C N'aλ	Units	Conditions
,	HIGH Level	(V)	C.65 x V		0.35 x V _C (II ay		
/ _{IH}		140 (1)	1 1 11	_ \		人 ·		
	Input Voltage	1.10 ≤ V _{CC} ≤ 1. ·0			0.65 \ V _C (
		1.40 ≤ V _{CC} ≤ 1 60			1.65 x 1/50		V	
		1.65 - V _{CC} ≤ 1.95	/ / / / / /		0.05 x V _{CC}			
		$2.3c \le V_{CC} \le 2.70$		$\langle V \rangle$	1.6			
		$3.00 \le V_{CO} \le 3.30$		10	2.1			
B 7	OW revel	0.90	/ 12 '	.35 x V _{CC}		$0.35 \times V_{CC}$		
	ut Voltage, بار	$1.10 \le v_{CC} \le 1.30$	0.	.35 x V _{CC}		$0.35 \times V_{CC}$		
		$1 + 3 \le V_{CC} \le 1.00$	0.	.35 x V _{CC}		$0.35 \times V_{\rm CC}$	V	
	(GV, X)	$1.65 \le V_{CC} \le 1.95$	0.	.35 x V _{CC}		$0.35 \times V_{\rm CC}$	ľ	
\		$2.25 \le V_{CC} \le 2.70$		0.7		0.7		
		$3.70 \le V_{CC} \le 3.60$		0.9		0.9		
/C+/	HIGH Level	0.90	V _{CC} - 0.1		V _{CC} - 0.1			
,	Output Voltage	1.10 ≤ V _{CC} ≤ 1.30	V _{CC} - 0.1		$V_{CC} - 0.1$			
	OV.	$1.40 \le V_{CC} \le 1.60$	V _{CC} - 0.1		$V_{CC} - 0.1$			
		$1.65 \le V_{CC} \le 1.95$	V _{CC} - 0.1		$V_{CC} - 0.1$			$I_{OH} = -20 \mu A$
	•	$2.30 \le V_{CC} \le 2.70$	V _{CC} - 0.1		V _{CC} - 0.1			
		$3.00 \le V_{CC} \le 3.60$	V _{CC} - 0.1		V _{CC} - 0.1		V	
		1.10 ≤ V _{CC} ≤ 1.30	0.75 x V _{CC}		0.70 x V _{CC}			$I_{OH} = -0.5 \text{ mA}$
		1.40 ≤ V _{CC} ≤ 1.60	1.07		0.99			I _{OH} = -1.0 mA
		1.65 ≤ V _{CC} ≤ 1.95	1.24		1.22			I _{OH} = -1.5 mA
		2.30 ≤ V _{CC} ≤ 2.70			1.87			I _{OH} = -2.1 mA
		3.00 ≤ V _{CC} ≤ 3.60	2.61		2.55		1	$I_{OH} = -2.6 \text{ mA}$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A =	= +25°C	$T_A = -40^{\circ}$	°C to +85°C	Units	Conditions
Symbol	Farameter	(V)	Min	Max	Min	Max	Units	Conditions
V _{OL}	LOW Level	0.90		0.1		0.1		
	Output Voltage	$1.10 \leq V_{CC} \leq 1.30$		0.1		0.1		
		$1.40 \le V_{CC} \le 1.60$		0.1		0.1		I _{OL} = 20 μA
		$1.65 \leq V_{CC} \leq 1.95$		0.1		0.1		I _{OL} = 20 μA
		$2.30 \leq V_{CC} \leq 2.70$		0.1		0.1		
		$3.00 \le V_{CC} \le 3.60$		0.1		0.1	V	
		1.10 ≤ V _{CC} ≤ 1.30		0.30 x V _{CC}		0.30 x V _{CC}		U.5
		1.40 ≤ V _{CC} ≤ 1.60		0.31		0.37		= 1.0 m/
		$1.65 \le V_{CC} \le 1.95$		0.31		0.35		I _C 1.5 mA
		$2.30 \le V_{CC} \le 2.70$		0.31		0.3		I _{OL} 1-
		$3.00 \le V_{CC} \le 3.60$		0.31		7.33		I _{OI} = 2 mA
I _{IN}	Input Leakage Current	0.90 to 3.60		±0.1		5	чA	_ V _I ≤ 3.6\
I _{OFF}	Power Off Leakage Current	0		0.5		0.		$0 \le (V_1, V_0) \le 3.6 V$
I _{CC}	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	μA	$V_1 = V_{C}$, or GND

AC Electrical Characteristics

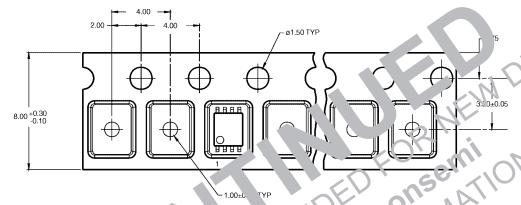
Symbol	Parameter	V _{cc}		T _A = C		= -40°C 10 +85°C		Units	Conditions	Figure
Syllibol	Parameter	(V)	Min	7	W	in	ivia.	Ullits	Constants	N umber
t _{PHL}	Propagation Delay	0.90						-	79 77	7
t _{PLH}		$1.10 \le V_{CC} \le 1.30$	4	9.0	20.7	3.5	30.9			Ì
		1.40 ≤ V _{CC} ≤	2.0	6.0	12.4	1.5	13 9	ns	$C_1 = 10.01$	Figures
		1.65 < `` ≤ 1.\	1.	5.0	9.6	1.0	12.1	115	$\Gamma_{1} = 1 M\Omega$	1, 2
		7	1.0	4.0	7.0	3.0	\$.0	/() \	
		$0.0 \le V_{CC} \le 0$	0	3.0	5.7	0.5	6.9	~	ĺ	
t _{PHL}	Propagatic	0.90	_ (5), 0			7/2			
t _{PLH}		130		10.0	22.2	4.5	33.9			
	1	.40 ≤ V _{CC} ≤ 1.6	3.0	7.0	10.3	2.5	16.0	ns	C _L = 15 pF	Figures
		.65 ≤ V _{CC} ≤ 1 /J5		5.9	10.3	50	12.6	110	$R_L = 1 M\Omega$	1, 2
		2.30 ⊆ 1 _{CC} ≤ 2 70	1.5	4.0	1.4	1.0	8.2			
		$5.00 \le V_{CC} \le 3.60$	1.0	3.0	6.1	0.5	7.0			
	Pror ation Delay	0.90		34.0	6					
t _{PL}	G			1.2.0	26.0	5.0	43.0			
	12			8.0	16.0	3.0	18.0	ns	C _L = 30 pF	Figures
				6.0	12.0	2.0	14.0		$R_L = 1 M\Omega$	1, 2
[(C	/ · · · · · · · · · · · · · · · · · · ·	$2.30 \le V_{00} \le 2.70$	1.0	5.0	9.0	1.0	10.0			
777		$3.00 \le V_{CC} \le 3.60$	0.8	4.0	7.0	0.5	8.9			
		0		2.0				pF		
	Output Capacitan วย	0		4.0	, and the second			pF		
C _{PD}	Power Dissipation Capacitance	0.9 to 3.60		6.0				pF	$V_I = 0V \text{ or } V_{CC},$ f = 10 MHz	
C _{IIN}	Power Dissipation	0.90 $1.10 \le V_{C,T} \le 1.30$ $1.40 \le V_{C,T} \le 1.60$ $1.60 \le V_{C,C} \le 1.9$ $2.30 \le V_{C,C} \le 2.70$ 0 0	6.0 4.7 2.0 1.0	34.\\ 12.0 8.0 6.0 5.0 4.0 2.0	26.0 16.0 12.0 9.0	5.0 3.0 2.0 1.0	43.0 18.0 14.0 10.0	pF	$R_L = 1 \text{ M}\Omega$ $V_i = 0 \text{V or } V_{CC}$	

AC Loading and Waveforms TEST O SIGNAL O FIGURE 1. AC Test Circuit $t_r = 3 \text{ ns}$ $t_f = 3 \text{ ns}$ INPUT 10% OUTPUT FIGURE 2. A 3 V/aveforms Symbol 1.8V ± 0.15V 1.2V ± 0.10V 0.9V V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC}/2 V_{CC}/2

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Tape and Reel Specification TAPE FORMAT for US8 Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed K8X Carrier 3000 Filled Sealed Trailer (Hub End) Sealed 75 (typ) Empty

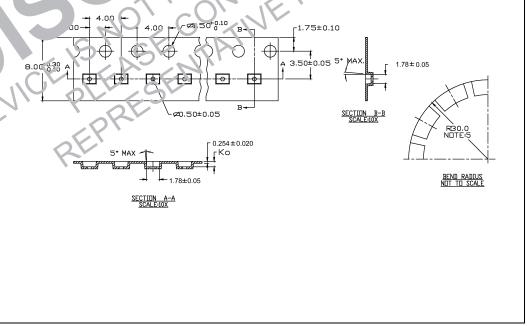
TAPE DIMENSIONS inches (millimeters)

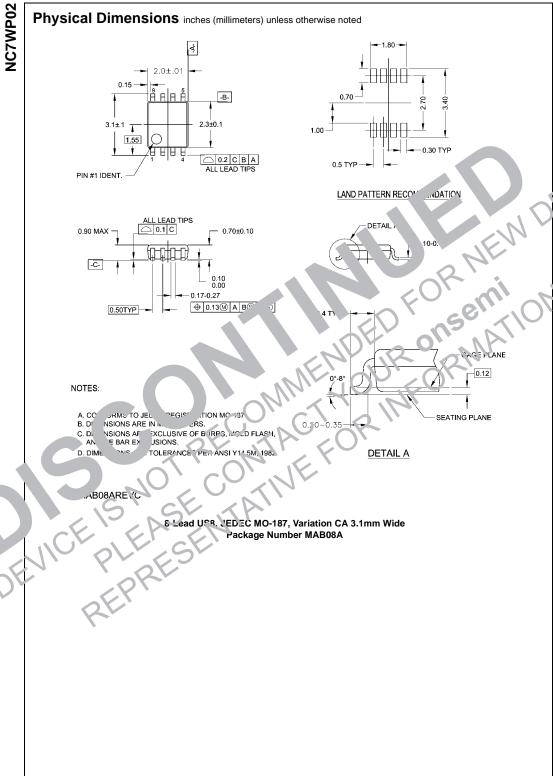


TAPE FORMAT for MicroPak

Package	Tape	Number	Cavity	Cover Tape
Designator	on on	Cavitiss	Status	Status
	_eader (5 t Er.	1∠5 (typ)	Empty	Sealed
L8X	Car	3000	Fii.ed	Sealed
	ub End)	75 (typ)	Empty	Sealed

'S inch (millimetras)





Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 2X _____ 0.10 C 1.6 (0.805)(0.41) 1.6 (0.125)INDEX AREA 0.10 C (0.4)8X TOP VIEW 0.55 MAX 0.05 C Recommended La batt. 0.05 0.05 C 1.0 8X(0.09) \4/(0.1 8X 0.35 0.10M C A E 0.05M C 3X(0.2) TTOM V Not 1. F CKAGE CONFORMS TO JEDEC MO-255 VARIATION L'AND NSION ARE IN MILLIMFTERS 2. D. ONFORMS TO ASME 1, 14, 1-1994 ORA 1 FLAG, FIND OF PACKAGE OFFSET. MAC08AREVC

Package Number MAC08A

-Free 8-Lean MicroPak, 1.6 mm Wide

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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