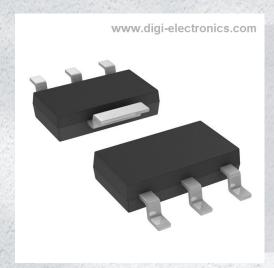


NCV8402STT1G Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number NCV8402STT1G-DG

Manufacturer onsemi

Manufacturer Product Number NCV8402STT1G

Description IC PWR DRIVER N-CHAN 1:1 SOT223

Detailed Description Power Switch/Driver 1:1 N-Channel 2A SOT-223 (TO

-261)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NCV8402STT1G	onsemi
Series:	Product Status:
	Obsolete
Switch Type:	Number of Outputs:
General Purpose	1
Ratio - Input:Output:	Output Configuration:
1:1	Low Side
Output Type:	Interface:
N-Channel	On/Off
Voltage - Load:	Voltage - Supply (Vcc/Vdd):
42V (Max)	Not Required
Current - Output (Max):	Rds On (Typ):
2A	165mOhm
Input Type:	Features:
Non-Inverting	Auto Restart
Fault Protection:	Operating Temperature:
Current Limiting (Fixed), Over Temperature, Over Voltage	-40°C ~ 150°C (TJ)
Grade:	Qualification:
Automotive	AEC-Q100
Mounting Type:	Supplier Device Package:
Surface Mount	SOT-223 (TO-261)
Package / Case:	Base Product Number:
TO-261-4, TO-261AA	NCV8402

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001



Self-Protected Low Side Driver with Temperature and Current Limit

NCV8402, NCV8402A

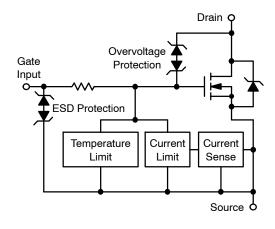
NCV8402/A is a three terminal protected Low–Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain–to–Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- NCV8402AMNWT1G Wettable Flanks Product
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

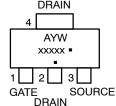


V _{(BR)DSS} (Clamped)	R _{DS(ON)} TYP	I _D MAX
42 V	165 mΩ @ 10 V	2.0 A*

^{*}Max current limit value is dependent on input condition.

MARKING DIAGRAMS







DFN6 CASE 506AX





DFN6 (WF) CASE 506DK



A = Assembly Location

Y = Year

W or WW = Work Week xxxxx = V8402 or 8402A

■ = Pb-Free Package

(Note: Microdot may be in either location)

DFN6 PACKAGE PIN DESCRIPTION

	G	NC	NC
ſ	1	2	3
		7 EPAI)
	6	5	4
	S	S	S

Pin#	Symbol	Description
1	G	Gate Input
2	NC	No Connect
3	NC	No Connect
4	S*	Source
5	S*	Source
6	S*	Source
7	EPAD	Drain

*Pins 4, 5, 6 are internally shorted together. It is recommended to short these pins externally.

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

	Rating		Symbol	Value	Unit	
Drain-to-Source Voltage Internally	Clamped		V_{DSS}	42	V	
Drain-to-Gate Voltage Internally Cl	Drain-to-Gate Voltage Internally Clamped $(R_G = 1.0 MΩ)$			42	V	
Gate-to-Source Voltage			V_{GS}	±14	V	
Continuous Drain Current			I _D	Internally L	Internally Limited	
Total Power Dissipation – SOT-223	3 Version	@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C)	P _D	1.1 1.74 8.9	W	
@ T _A = 2		@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C)	P _D	0.76 1.78 8.9	W	
Maximum Continuous Drain Curren	@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C)	I _D	1.54 1.94 6.75	Α		
Maximum Continuous Drain Current – DFN Version 0 T _A = 25°C (Note 1) 0 T _A = 25°C (Note 2) 0 T _S = 25°C)			Ι _D	1.28 1.97 6.75	Α	
Thermal Resistance	SOT223 Junction-to-	-Ambient Steady State (Note 1) -Ambient Steady State (Note 2) o-Soldering Point Steady State	$egin{aligned} R_{ hetaJA} \ R_{ hetaJS} \end{aligned}$	114 72 14	°C/W	
	DFN Junction-to-	-Ambient Steady State (Note 1) -Ambient Steady State (Note 2) o-Soldering Point Steady State	$egin{aligned} R_{ hetaJA} \ R_{ hetaJS} \end{aligned}$	163 70 14		
Single Pulse Drain-to–Source Avalanche Energy (V _{DD} = 32 V, V _G = 5.0 V, I _{PK} = 1.0 A, L = 300 mH, R _{G(ext)} = 25 Ω)			E _{AS}	150	mJ	
Load Dump Voltage	$(V_{GS} = 0 \text{ and } 10 \text{ V}, R_I =$	2.0 Ω, $R_L = 9.0$ Ω, $t_d = 400$ ms)	V_{LD}	55	V	
Operating Junction Temperature			TJ	-40 to 150	°C	
Storage Temperature			T _{stg}	-55 to 150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).

2. Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).

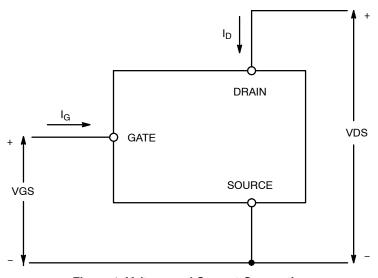


Figure 1. Voltage and Current Convention

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter Parameter	Test Condition	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS				-71		
Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C	V _{(BR)DSS}	42	46	55	V
(Note 3)	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5)	(31,920	40	45	55	1
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C	I _{DSS}		0.25	4.0	μΑ
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5)	I _{DSS}		1.1	20	μΑ
Gate Input Current	V _{DS} = 0 V, V _{GS} = 5.0 V	I _{GSSF}		50	100	μΑ
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 150 \mu A$	V _{GS(th)}	1.3	1.8	2.2	V
Gate Threshold Temperature Coefficient		V _{GS(th)} /T _J		4.0		-mV/°C
Static Drain-to-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 1.7 \text{ A}, T_J = 25^{\circ}\text{C}$	R _{DS(on)}		165	200	mΩ
	V _{GS} = 10 V, I _D = 1.7 A, T _J = 150°C (Note 5)			305	400	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 25°C			195	230	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 150°C (Note 5)			360	460	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C			190	230	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 5)			350	460	-
Source-Drain Forward On Voltage	V _{GS} = 0 V, I _S = 7.0 A	V _{SD}		1.0		V
SWITCHING CHARACTERISTICS (Note	5)			•		•
Turn-On Time (10% V _{IN} to 90% I _D)		t _{on}		25	30	μs
Turn-Off Time (90% V _{IN} to 10% I _D)		t _{off}		120	200	μs
Turn–On Rise Time (10% I_D to 90% I_D)	V _{GS} = 10 V, V _{DD} = 12 V,	t _{rise}		20	25	μs
Turn-Off Fall Time (90% I _D to 10% I _D)	$I_D = 2.5 \text{ A}, R_L = 4.7 \Omega$	t _{fall}		50	70	μs
Slew-Rate ON (70% to 50% V _{DD})		-dV _{DS} /dt _{ON}		0.8	1.2	V/μs
Slew-Rate OFF (50% to 70% V _{DD})		dV _{DS} /dt _{OFF}		0.3	0.5	V/μs
SELF PROTECTION CHARACTERISTIC	S (T _J = 25°C unless otherwise noted) (Note 4)				
Current Limit	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 25°C (Note 6)	I _{LIM}	3.7	4.3	5.0	Α
	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Notes 5, 6)		2.3	3.0	3.7	1
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C (Note 6)		4.2	4.8	5.4	1
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Notes 5, 6)		2.7	3.6	4.5	1
Temperature Limit (Turn-off)	V _{GS} = 5.0 V (Notes 5, 6)	T _{LIM(off)}	150	175	200	°C
Thermal Hysteresis	V _{GS} = 5.0 V	$\Delta T_{LIM(on)}$		15		
Temperature Limit (Turn-off)	V _{GS} = 10 V (Notes 5, 6)	T _{LIM(off)}	150	165	185	
Thermal Hysteresis	V _{GS} = 10 V	$\Delta T_{LIM(on)}$		15		<u> </u>
GATE INPUT CHARACTERISTICS (Note	5)					
Device ON Gate Input Current	V _{GS} = 5 V I _D = 1.0 A	I _{GON}		50		μΑ
	V _{GS} = 10 V I _D = 1.0 A			400		

- Pulse Test: Pulse Width ≤300 µs, Duty Cycle ≤ 2%.
 Fault conditions are viewed as beyond the normal operating range of the part.
 Not subject to production testing.
 Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

ELECTRICAL CHARACTERISTICS (T_{.I} = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Тур	Max	Unit
GATE INPUT CHARACTERISTICS (Note	5)					
Current Limit Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GCL}		0.05		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.4		
Thermal Limit Fault Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GTL}		0.15		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.7		
ESD ELECTRICAL CHARACTERISTICS	(T _J = 25°C unless otherwise noted) (Note 5)				
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)	1	400			1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: Pulse Width ≤[300 μs, Duty Cycle ≤ 2%.
 Fault conditions are viewed as beyond the normal operating range of the part.
- 5. Not subject to production testing.6. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

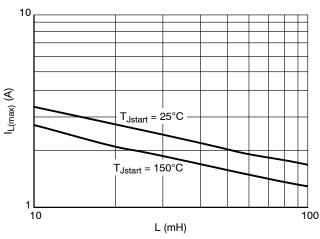


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

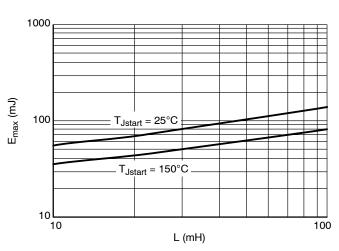


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

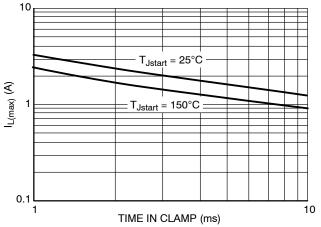


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

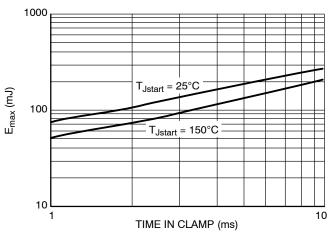


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

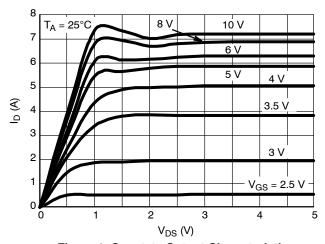


Figure 6. On-state Output Characteristics

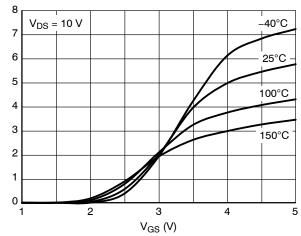


Figure 7. Transfer Characteristics

I_D (A)

TYPICAL PERFORMANCE CURVES

I⊔M (A)

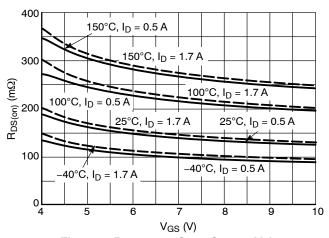


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

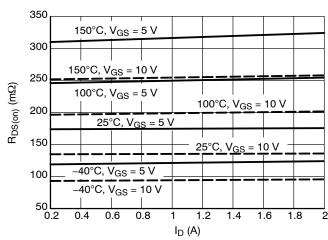


Figure 9. R_{DS(on)} vs. Drain Current

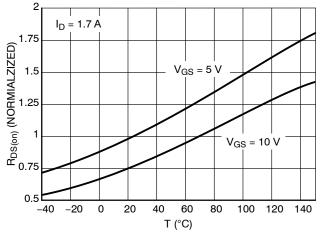


Figure 10. Normalized R_{DS(on)} vs. Temperature

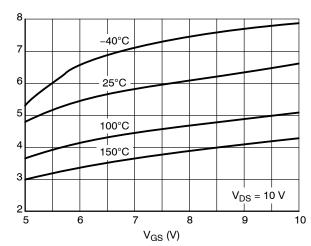


Figure 11. Current Limit vs. Gate-Source Voltage

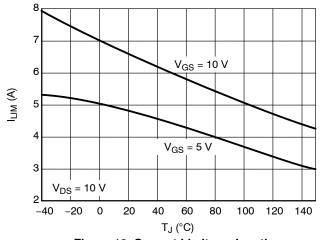


Figure 12. Current Limit vs. Junction Temperature

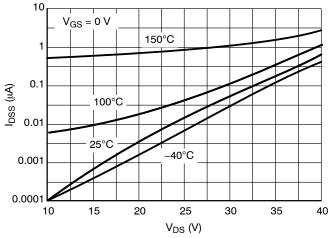


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

DRAIN-SOURCE VOLTAGE SLOPE (V/µs)

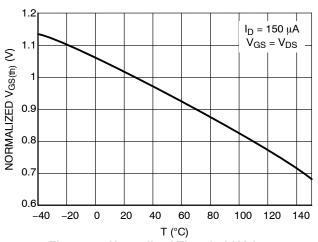


Figure 14. Normalized Threshold Voltage vs. Temperature

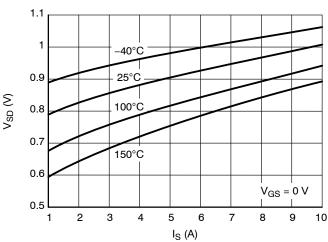


Figure 15. Source-Drain Diode Forward Characteristics

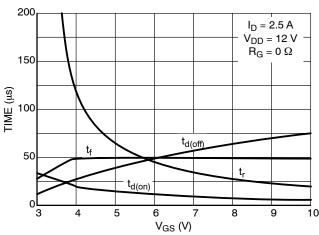


Figure 16. Resistive Load Switching Time vs.
Gate-Source Voltage

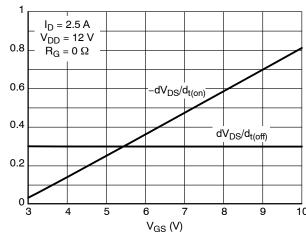


Figure 17. Resistive Load Switching
Drain-Source Voltage Slope vs. Gate-Source
Voltage

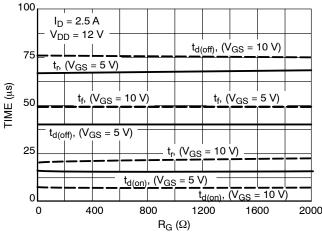


Figure 18. Resistive Load Switching Time vs.
Gate Resistance

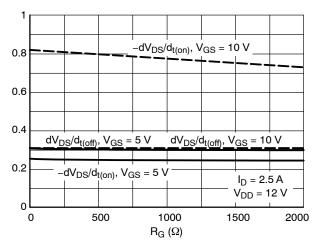


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

DRAIN-SOURCE VOLTAGE SLOPE (V/μs)

TYPICAL PERFORMANCE CURVES

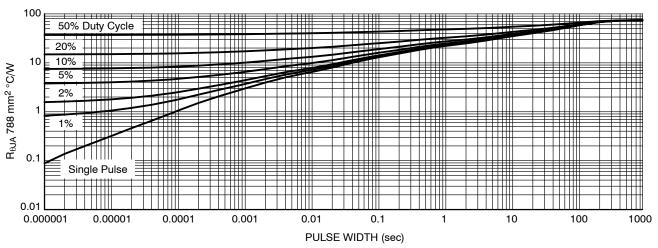


Figure 20. Transient Thermal Resistance - SOT-223 Package

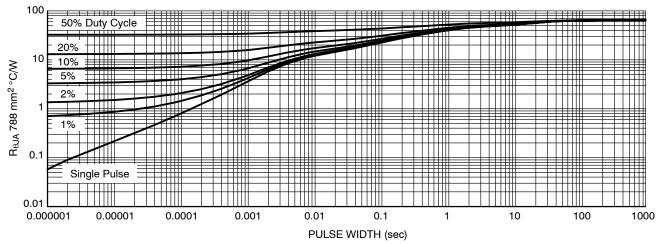


Figure 21. Transient Thermal Resistance - DFN Package

TEST CIRCUITS AND WAVEFORMS

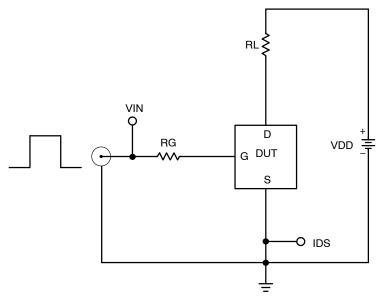


Figure 22. Resistive Load Switching Test Circuit

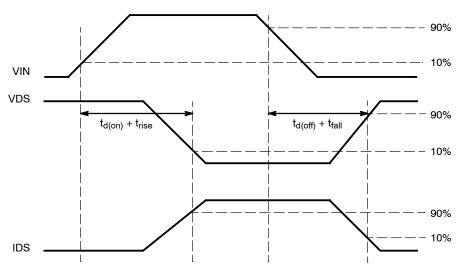


Figure 23. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

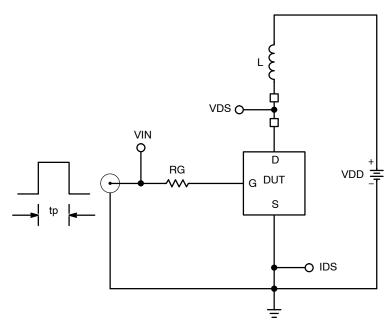


Figure 24. Inductive Load Switching Test Circuit

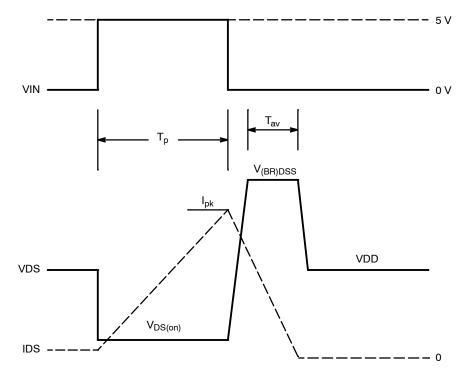


Figure 25. Inductive Load Switching Waveforms

ORDERING INFORMATION

Device*	Package	Shipping [†]
NCV8402STT1G	SOT-223	1000 / Tape & Reel
NCV8402ASTT1G	(Pb-Free)	
NCV8402STT3G	SOT-223	4000 / Tape & Reel
NCV8402ASTT3G	(Pb-Free)	
NCV8402AMNT2G	DFN6 (Pb-Free)	2000 / Tape & Reel
NCV8402AMNWT1G	DFN6 (Pb-Free, Wettable Flank)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP

Capable.

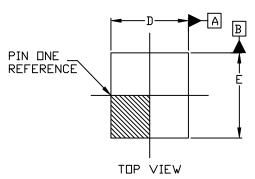
PACKAGE DIMENSIONS

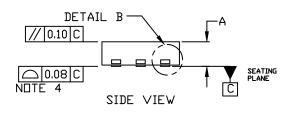
DFN6 3.0x3.3, 0.95P CASE 506AX

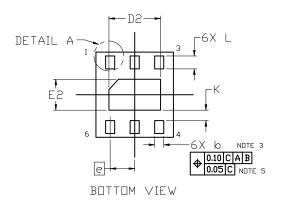
ISSUE A

DATE 22 SEP 2020



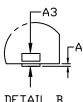






NDTES:

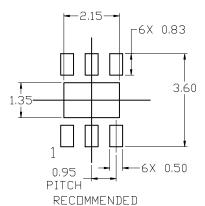
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
 DIMENSION & APPLIES TO PLATED TERMINALS AND IS
 MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
 COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL
- AS THE TERMINALS.
- POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL B



	MILLIMETERS				
DIM	MIN.	N□M.	MAX.		
Α	0.80	0.90	1.00		
A1	0.00		0.05		
b	0.30	0.35	0.40		
D	2.90	3.10			
D2	1.90	2.00	2.10		
E	3,20	3.30	3.40		
E2	1.10	1.20	1.30		
е	0.95 BSC				
К	0,40 REF				
L	0.40 0.50 0.60				
L1	0.00		0.15		



MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*

XXXXX XXXXX AYWW= XXXX = Specific Device Code = Assembly Location

= Year WW

= Work Week = Pb-Free Package

(Note: Microdot may be in either location)

For additional information on our Pb-Free strategy and soldering details, please download the IIN Semiconductor Soldering and Mounting Techniques Reference Manual, SILDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



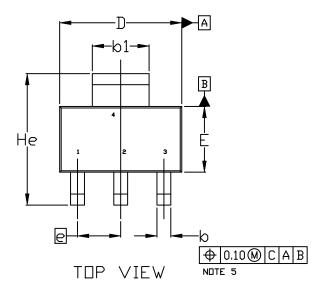
MECHANICAL CASE OUTLINE

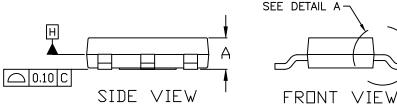
PACKAGE DIMENSIONS

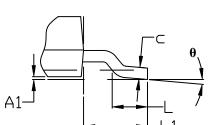


SOT-223 (TO-261) CASE 318E-04 ISSUE R

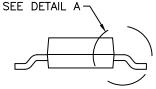
DATE 02 OCT 2018







DETAIL A

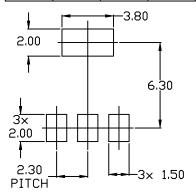




NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- POSITIONAL TOLERANCE APPLIES TO DIMENSIONS to AND tol.

	MILLIMETERS				
DIM	MIN.	N□M.	MAX.		
Α	1.50	1.63	1.75		
A1	0.02	0.06	0.10		
b	0.60	0.75	0.89		
b1	2.90	3.20			
c	0.24	0.29	0.35		
D	6.30	6.50	6.70		
E	3.30	3.70			
е		5'30 B2C	;		
L	0.20	0.20			
L1	1.50	1.75	2.00		
He	6.70	6.70 7.00			
θ	0*		10*		



RECOMMENDED MOUNTING **FOOTPRINT**

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Ī	DESCRIPTION:	SOT-223 (TO-261)		PAGE 1 OF 2	

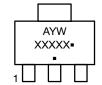
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SOT-223 (TO-261) CASE 318E-04 ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

GENERIC MARKING DIAGRAM*



A = Assembly Location

Y = Year

W = Work Week XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

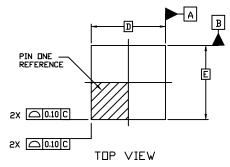
PACKAGE DIMENSIONS

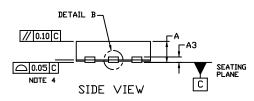
DFNW6 3x3, 0.95P

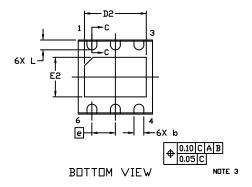
CASE 506DK ISSUE A

DATE 07 MAY 2021









GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code

A = Assembly Location

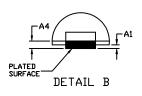
L = Wafer Lot
Y = Year
W = Work Week
• Pb-Free Package

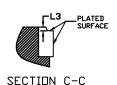
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

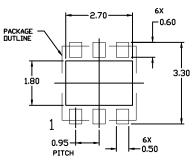
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSION 6 APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
- PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.





MIN.	MAX.	MAX.	
0.75	0.85	0.95	
0.00		0.05	
0.20 REF			
0.10			
0.35	0.40	0.45	
3.00 BSC			
2.40	2.50	2.60	
3.00 B2C			
1.50	1.60	1.70	
0.95 BSC			
0.30	0.40	0.50	
0.00	0.05	0.10	
	0.75 0.00 0.10 0.35 2.40 1.50	0.75 0.85 0.00 0.20 REF 0.10 0.35 0.40 3.00 BSC 2.40 2.50 3.00 BSC 1.50 1.60 0.95 BSC 0.30 0.40	

MILLIMETERS



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the IIN Semiconductor Soldering and Mounting Techniques Reference Manual, SILDERRM/D.

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DESCRIPTION:	DFNW6 3X3, 0.95P		PAGE 1 OF 1

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