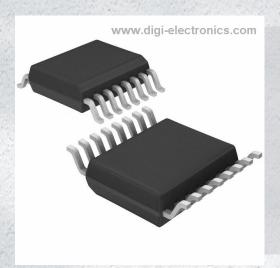


NLAS44599DTG Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number NLAS44599DTG-DG

Manufacturer onsemi

Manufacturer Product Number NLAS44599DTG

Description IC SWITCH DPDT X 2 250HM 16TSSOP

Detailed Description 2 Circuit IC Switch 2:2 250hm 16-TSSOP



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
NLAS44599DTG	onsemi
Series:	Product Status:
	Obsolete
Switch Circuit:	Multiplexer/Demultiplexer Circuit:
DPDT	2:2
Number of Circuits:	On-State Resistance (Max):
2	250hm
Channel-to-Channel Matching (ΔRon):	Voltage - Supply, Single (V+):
	2V ~ 5.5V
Voltage - Supply, Dual (V±):	Switch Time (Ton, Toff) (Max):
	14ns, 5ns
-3db Bandwidth:	Charge Injection:
175MHz	3pC
Channel Capacitance (CS(off), CD(off)):	Current - Leakage (IS(off)) (Max):
10pF, 10pF	10μΑ
Crosstalk:	Operating Temperature:
-90dB @ 100kHz	-55°C ~ 125°C (TA)
Mounting Type:	Package / Case:
Surface Mount	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package:	Base Product Number:
16-TSSOP	NLAS4

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8542.39.0001

Low Voltage Single Supply Dual DPDT Analog Switch

The NLAS44599 is an advanced dual-independent CMOS double pole-double throw (DPDT) analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This DPDT controls analog and digital voltages that may vary across the full power–supply range (from $V_{\rm CC}$ to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs. The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The NLAS44599 can also be used as a quad 2-to-1 multiplexerdemultiplexer analog switch with two Select pins that each controls two multiplexer-demultiplexers.

- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max) at $T_A = 25^{\circ}C$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 158 FETs
- Pb-Free Packages are Available



ON Semiconductor®

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MARKING DIAGRAMS



QFN-16 MN SUFFIX CASE 485G

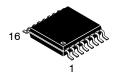


Current Part Marking

16 1 C ALYW

> Previous Part Marking*

*Previous releases of this device may be marked as shown in this diagram.



TSSOP-16 DT SUFFIX CASE 948F

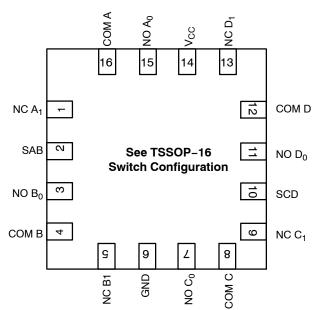
A = Assembly Location

L = Wafer Lot
 Y = Year
 W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

QFN-16 PACKAGE



FUNCTION TABLE

Select AB or CD	On Channel
L	NC to COM
Н	NO to COM

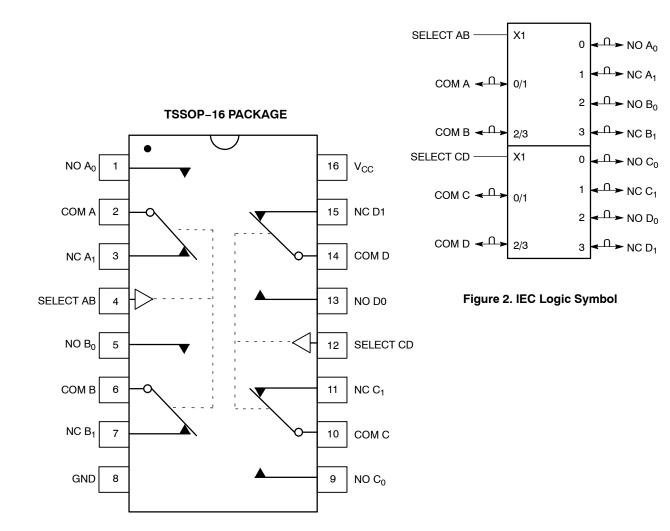


Figure 1. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	•	Value	Unit
V _{CC}	Positive DC Supply Voltage		-0.5 to +7.0	V
V _{IS}	Analog Input Voltage (V _{NO} or V _{COM})		$-0.5 \le V_{IS} \le V_{CC} + 0.5$	
V _{IN}	Digital Select Input Voltage		$-0.5 \le V_{\parallel} \le +7.0$	V
I _{IK}	DC Current, Into or Out of Any Pin		±50	mA
P _D	Power Dissipation in Still Air	800 450	mW	
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Second	260	°C	
TJ	Junction Temperature Under Bias		+150	°C
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94-V0 (0.125 in)	
V _{ESD}	ESD Withstand Voltage	2000 200 1000	V	
I _{Latch-Up}	Latch-Up Performance Above V	CC and Below GND at 125°C (Note 4)	±300	mA
θ_{JA}	Thermal Resistance	QFN-16 TSSOP-16	80 164	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Tested to EIA/JESD22-A114-A.
- 2. Tested to EIA/JESD22-A115-A.
- 3. Tested to JESD22-C101-A.
- 4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage	2.0	5.5	V	
V _{IN}	Digital Select Input Voltage	GND	5.5	V	
V _{IS}	Analog Input Voltage (NC, NO, COM)		GND	V _{CC}	V
T _A	Operating Temperature Range		-55	+125	°C
t _r , t _f	Input Rise or Fall Time, SELECT V _{CC} : V _{CC} :	= 3.3 V ± 0.3 V = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

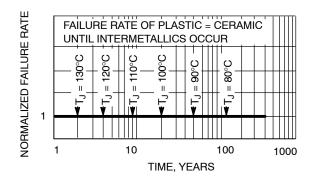


Figure 3. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS - Digital Section (Voltages Referenced to GND)

				Guaranteed Limit			
Symbol	Parameter	Condition	V _{CC}	-55°C to 25°C	<85°C	<125°C	Unit
V _{IH}	Minimum High-Level Input		2.0	1.5	1.5	1.5	V
	Voltage, Select Inputs		2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V _{IL}	Maximum Low-Level Input		2.0	0.5	0.5	0.5	V
	Voltage, Select Inputs		2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	5.5	±0.2	±2.0	±2.0	μА
l _{OFF}	Power Off Leakage Current, Select Inputs	V _{IN} = 5.5 V or GND	0	±10	±10	±10	μΑ
lcc	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	4.0	4.0	8.0	μΑ

DC ELECTRICAL CHARACTERISTICS - Analog Section

				Guaranteed Limit			
Symbol	Parameter	Condition	V _{CC}	-55°C to 25°C	<85°C	<125°C	Unit
R _{ON}	Maximum "ON" Resistance (Figures 17 – 23)	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IS} = \text{GND to } V_{CC}$	2.5 3.0	85 45	95 50	105 55	Ω
	,	$I_{\text{IN}}I \leq 10.0 \text{ mA}$	4.5 5.5	30 25	35 30	40 35	
R _{FLAT (ON)}	ON Resistance Flatness (Figures 17 – 23)	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{IN}I \le 10.0 \text{ mA}$ $V_{IS} = 1 \text{ V, 2 V, 3.5 V}$	4.5	4	4	5	Ω
I _{NC(OFF)} I _{NO(OFF)}	NO or NC Off Leakage Current (Figure 9)	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{NO} \text{ or } V_{NC} = 1.0 \text{ V}_{COM} \text{ 4.5 V}$	5.5	1	10	100	nA
I _{COM(ON)}	COM ON Leakage Current (Figure 9)	$\begin{split} &V_{IN} = V_{IL} \text{ or } V_{IH} \\ &V_{NO} \text{ 1.0 V or 4.5 V with } V_{NC} \text{ floating or } \\ &V_{NO} \text{ 1.0 V or 4.5 V with } V_{NO} \text{ floating } \\ &V_{COM} = \text{1.0 V or 4.5 V} \end{split}$	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

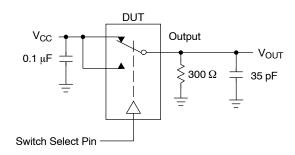
						Guaranteed Maximum Limit						
			V _{CC}	V _{IS}	- 5	5°C to 2	25°C	<8	5°C	< 12	25°C	
Symbol	Parameter	Test Conditions	(v)	(V)	Min	Тур*	Max	Min	Max	Min	Max	Unit
t _{ON}	Turn-On Time	$R_L = 300 \Omega, C_L = 35 pF$	2.5	2.0	5	23	35	5	38	5	41	ns
	(Figures 12 and 13)	(Figures 5 and 6)	3.0	2.0	5	16	24	5	27	5	30	
			4.5	3.0	2	11	16	2	19	2	22	
			5.5	3.0	2	9	14	2	17	2	20	
t _{OFF}	Turn-Off Time	$R_L = 300 \Omega, C_L = 35 pF$	2.5	2.0	1	7	12	1	15	1	18	ns
	(Figures 12 and 13)	(Figures 5 and 6)	3.0	2.0	1	5	10	1	13	1	16	
			4.5	3.0	1	4	6	1	9	1	12	
			5.5	3.0	1	3	5	1	8	1	11	
t _{BBM}	Minimum Break-Before-Make	V _{IS} = 3.0 V (Figure 4)	2.5	2.0	1	12		1		1		ns
	Time	$R_L = 300 \Omega, C_L = 35 pF$	3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

		Typical @ 25, V _{CC} = 5.0 V	~F
C _{IN}	Maximum Input Capacitance, Select Input	8	pF
C _{NO} or C _{NC}	Analog I/O (switch off)	10	
C _{COM}	Common I/O (switch off)	10	
C _(ON)	Feedthrough (switch on)	20	

^{*}Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

			V _{CC}	Typical	
Symbol	Parameter	Condition	v	25°C	Unit
BW	Maximum On-Channel -3dB	V _{IN} = 0 dBm	3.0	145	MHz
	Bandwidth or Minimum Frequency Response (Figure 11)	V _{IN} centered between V _{CC} and GND	4.5	170	
	Tresponse (Figure 11)	(Figure 7)	5.5	175	1
V _{ONL}	Maximum Feedthrough On Loss	V _{IN} = 0 dBm @ 100 kHz to 50 MHz	3.0	-3	dB
		V _{IN} centered between V _{CC} and GND	4.5	-3	1
		(Figure 7)	5.5	-3	1
V _{ISO}	Off-Channel Isolation (Figure 10)	f = 100 kHz; V _{IS} = 1 V RMS	3.0	-93	dB
		V _{IN} centered between V _{CC} and GND	4.5	-93	1
		(Figure 7)	5.5	-93	1
Q	Charge Injection Select Input to	V _{IN =} V _{CC to} GND, F _{IS} = 20 kHz			рC
	Common I/O (Figure 15)	$t_r = t_f = 3 \text{ ns}$	3.0	1.5	1
		$R_{IS} = 0 \Omega$, $C_L = 1000 pF$	5.5	3.0	1
		$Q = C_L * \Delta V_{OUT}$			
		(Figure 8)			
THD	Total Harmonic Distortion THD +	F_{IS} = 20 Hz to 100 kHz, R_L = Rgen = 600 Ω , C_L = 50 pF			%
	Noise (Figure 14)	$V_{IS} = 5.0 V_{PP}$ sine wave	5.5	0.1	1
VCT	Channel-to-Channel Crosstalk	f = 100 kHz; V _{IS} = 1 V RMS			dB
		V _{IN} centered between V _{CC} and GND	5.5	-90	
		(Figure 7)	3.0	-90	1



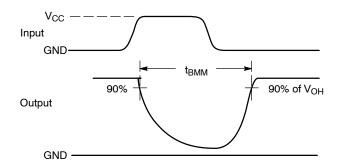
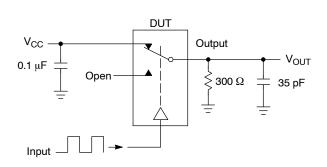


Figure 4. t_{BBM} (Time Break-Before-Make)



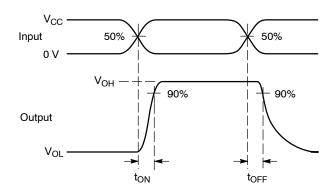
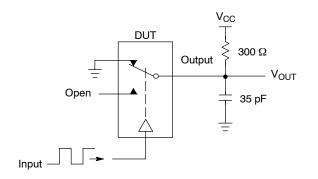


Figure 5. t_{ON}/t_{OFF}



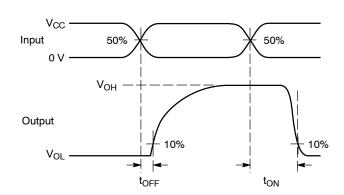
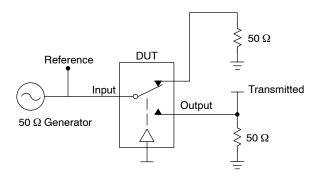


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$\begin{split} &V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at } 100 \text{ kHz} \\ &V_{ONL} = \text{On Channel Loss} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz} \end{split}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

 V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

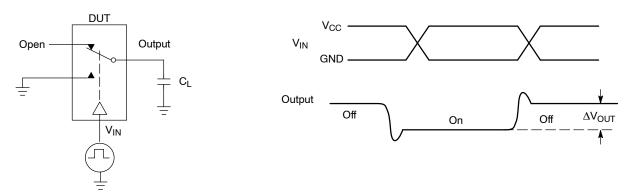


Figure 8. Charge Injection: (Q)

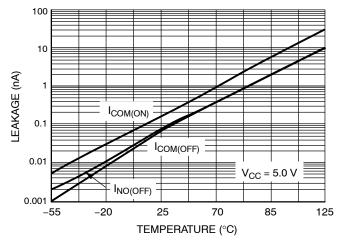
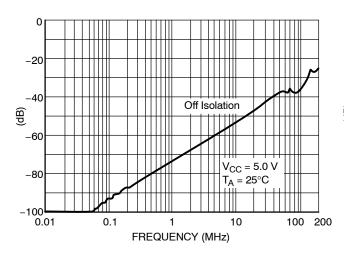


Figure 9. Switch Leakage vs. Temperature

30



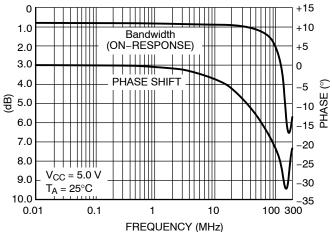
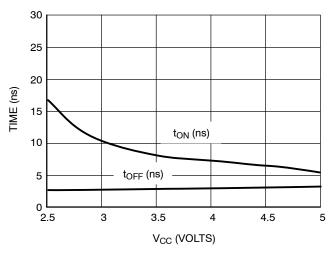


Figure 10. Off-Channel Isolation

Figure 11. Typical Bandwidth and Phase Shift



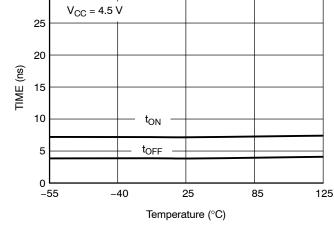
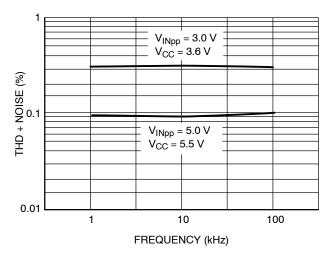


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

Figure 13. t_{ON} and t_{OFF} vs. Temp



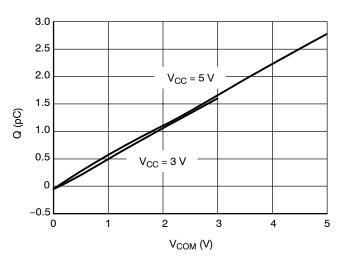
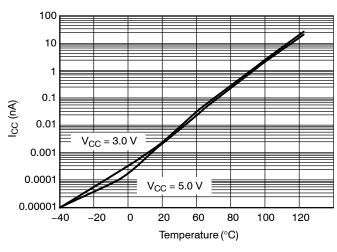


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

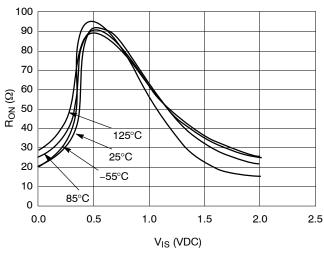
Figure 15. Charge Injection vs. COM Voltage



100 $V_{CC} = 2.0 \text{ V}$ 80 60 Ron (Q) V_{CC} = 2.5 V 40 $V_{CC} = 3.0 \text{ V}$ V_{CC} = 4.0 V 20 V_{CC} = 5.5 V 0.0 1.0 2.0 3.0 4.0 5.0 6.0 V_{IS} (VDC)

Figure 16. I_{CC} vs. Temp, V_{CC} = 3 V & 5 V

Figure 17. R_{ON} vs. V_{CC}, Temp = 25°C



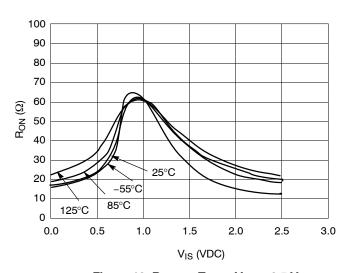
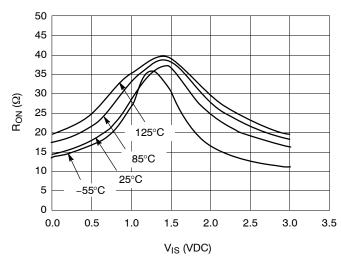


Figure 18. R_{ON} vs Temp, V_{CC} = 2.0 V

Figure 19. R_{ON} vs. Temp, V_{CC} = 2.5 V



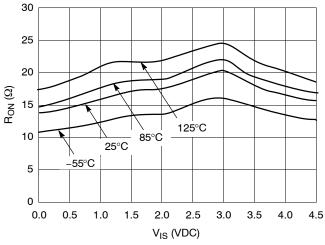
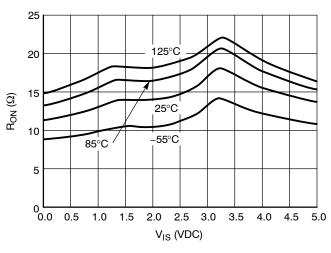


Figure 20. R_{ON} vs. Temp, V_{CC} = 3.0 V

Figure 21. R_{ON} vs. Temp, V_{CC} = 4.5 V



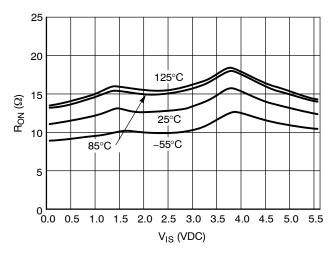


Figure 22. R_{ON} vs. Temp, V_{CC} = 5.0 V

Figure 23. R_{ON} vs. Temp, V_{CC} = 5.5 V

DEVICE ORDERING INFORMATION

		Devi	ce Nomenc				
Device	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type	Shipping [†]
NLAS44599DT	NL	AS	44599	DT		TSSOP-16*	96 / Unit Rail
NLAS44599DTR2	NL	AS	44599	DT	R2	TSSOP-16*	2500 / Tape & Reel
NLAS44599MN	NL	AS	44599	MN		QFN-16	124 Unit / Rail
NLAS44599MNG	NL	AS	44599	MN		QFN-16 (Pb-Free)	124 Unit / Rail
NLAS44599MNR2	NL	AS	44599	MN	R2	QFN-16	2500 / Tape & Reel
NLAS44599MNR2G	NL	AS	44599	MN	R2	QFN-16 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}This package is inherently Pb-Free.



SCALE 2:1

PIN ONE

LOCATION

2X 0.10 C

2X 0.10 C

// 0.05 C

□ 0.05 C

NOTE 4

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



回

TOP VIEW

DETAIL B

LEA

В

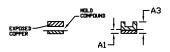
SEATING PLANE

E

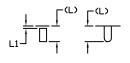
DATE 08 OCT 2021

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS.
 THE TERMINALS.



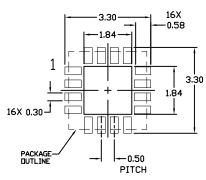
DETAIL B
ALTERNATE
CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

	MILLIMETERS		
DIM	MIN.	N□M.	MAX.
Α	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
DS	1.65	1.75	1.85
Е	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



◆ 0.10 C A B
DETAIL A S 16X L
9 0.10 CAB 9 16X b 0.10 CAB 0.05 C NOTE 3
e/2
B□TT□M VIEW

SIDE VIEW

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code A = Assembly Location

L = Wafer Lot
Y = Year
W = Work Week
Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	QFN16 3X3, 0.5P		PAGE 1 OF 1	

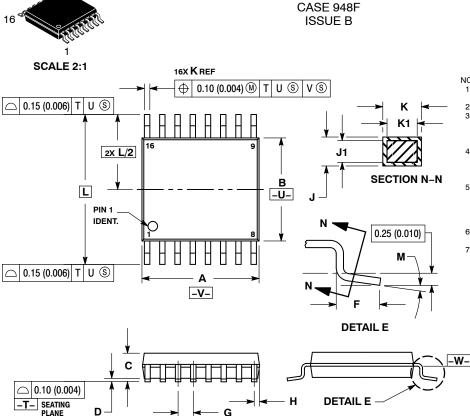
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TSSOP-16 WB



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



NOTES

DIMENSIONING AND TOLERANCING PER

DATE 19 OCT 2006

- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL
- IN TERLEAD FLASH OH PROTHOSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0 0	00	0 0	0

RECOMMENDED SOLDERING FOOTPRINT*

7.06 0.65 **PITCH** 16X 0.36 1.26 **DIMENSIONS: MILLIMETERS**

GENERIC MARKING DIAGRAM*



= Specific Device Code XXXX Α = Assembly Location

= Wafer Lot L = Year = Work Week W G or • = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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