

## **NLV17SZ08DFT2G Datasheet**



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DiGi Electronics Part Number NLV17SZ08DFT2G-DG

Manufacturer onsemi

Manufacturer Product Number NLV17SZ08DFT2G

Description IC GATE AND 1CH 2-INP SC88A

Detailed Description AND Gate IC 1 Channel SC-88A (SC-70-5/SOT-353)



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RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.



## **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:
NLV17SZ08DFT2G	onsemi
Series:	Product Status:
17SZ	Obsolete
Logic Type:	Number of Circuits:
AND Gate	1
Number of Inputs:	Features:
2	
Voltage - Supply:	Current - Quiescent (Max):
1.65V ~ 5.5V	1 μΑ
Current - Output High, Low:	Input Logic Level - Low:
32mA, 32mA	
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
	4.5ns @ 5V, 50pF
Operating Temperature:	Grade:
-55°C ~ 125°C	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Supplier Device Package:	Package / Case:
SC-88A (SC-70-5/SOT-353)	5-TSSOP, SC-70-5, SOT-353
Base Product Number:	
170700	

## **Environmental & Export classification**

8542.39.0001

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	



# Single 2-Input AND Gate NL17SZ08

The NL17SZ08 is a single 2-input AND Gate in tiny footprint packages.

SC-88A DF SUFFIX CASE 419A



MARKING DIAGRAMS

#### Features

- Designed for 1.65 V to 5.5 V V<sub>CC</sub> Operation
- 2.7 ns  $t_{PD}$  at  $V_{CC} = 5 \text{ V (typ)}$
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I<sub>OFF</sub> Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in SC-88A, SC-74A, SOT-553, SOT-953 and UDFN6 Packages
- Chip Complexity < 100 FETs
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

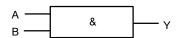


Figure 1. Logic Symbol



SC-74A DBV SUFFIX CASE 318BQ





SOT-553 XV5 SUFFIX CASE 463B





SOT-953 P5 SUFFIX CASE 527AE





UDFN6 1.45 x 1.0 CASE 517AQ





UDFN6 1.0 x 1.0 CASE 517BX

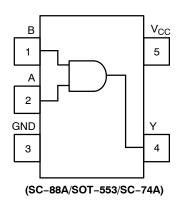


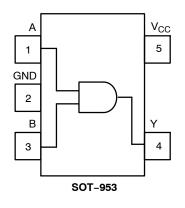
XX = Specific Device Code
M = Date Code\*
Pb-Free Package

\*Date Code orientation and/or position may vary depending upon manufacturing location. (Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.





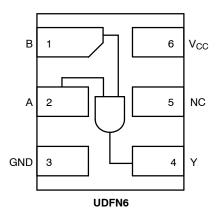


Figure 2. Pinout (Top View)

PIN ASSIGNMENT (SC-88A/SOT-553/SC-74A)

Pin	Function
1	В
2	Α
3	GND
4	Υ
5	V <sub>CC</sub>

#### PIN ASSIGNMENT (SOT-953)

Pin	Function
1	Α
2	GND
3	В
4	Y
5	V <sub>CC</sub>

#### PIN ASSIGNMENT (UDFN)

Pin	Function
1	В
2	Α
3	GND
4	Y
5	NC
6	V <sub>CC</sub>

#### **FUNCTION TABLE**

Inp	Output Y = AB	
Α	В	Υ
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

#### **MAXIMUM RATINGS**

Symbol	Characteristics		Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage		-0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage Active-Mode (Hig Tri-State Power-Down Mo	Mode (Note 1)	-0.5 to V <sub>CC</sub> + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < GND	-50	mA
lok	DC Output Diode Current	V <sub>OUT</sub> < GND	-50	mA
lout	DC Output Source/Sink Current		±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs		260	°C
TJ	Junction Temperature Under Bias		+150	°C
θJA	Thermal Resistance (Note 2)	SC-88A SC-74A SOT-553 SOT-953 UDFN6	377 320 324 254 154	°C/W
P <sub>D</sub>	Power Dissipation in Still Air	SC-88A SC-74A SOT-553 SOT-953 UDFN6	332 390 386 491 812	mW
MSL	Moisture Sensitivity		Level 1	-
F <sub>R</sub>	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V <sub>ESD</sub>		an Body Model d Device Model	2000 1000	V
I <sub>Latchup</sub>	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Applicable to devices with outputs that may be tri-stated.
   Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
   HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22–A115–A (Machine Model) be discontinued per JEDEC/JEP172A.

  4. Tested to EIA/JESD78 Class II.

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics			Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage		1.65	5.5	V
V <sub>IN</sub>	DC Input Voltage		0	5.5	V
V <sub>OUT</sub>	DC Output Voltage	Active–Mode (High or Low State) Tri–State Mode (Note 1) Power–Down Mode ( $V_{\rm CC}$ = 0 V)	0 0 0	V <sub>CC</sub> 5.5 5.5	V
T <sub>A</sub>	Operating Temperature Range		-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	$\begin{array}{c} V_{CC} = 1.65 \ V \ to \ 1.95 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 3.0 \ V \ to \ 3.6 \ V \\ V_{CC} = 4.5 \ V \ to \ 5.5 \ V \end{array}$	0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

#### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		–55°C ≤ T	<sub>A</sub> ≤ 125°C		
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Units
V <sub>IH</sub>	High-Level Input Volt	age	1.65 to 1.95	0.65 x V <sub>CC</sub>	-	-	0.65 x V <sub>CC</sub>	-	V
			2.3 to 5.5	0.70 x V <sub>CC</sub>	_	-	0.70 x V <sub>CC</sub>	-	
V <sub>IL</sub>	Low-Level Input Volta	age	1.65 to 1.95	-	_	0.35 x V <sub>CC</sub>	-	0.35 x V <sub>CC</sub>	V
			2.3 to 5.5	-	_	0.30 x V <sub>CC</sub>	-	0.30 x V <sub>CC</sub>	
V <sub>ОН</sub>	High-Level Output Voltage	$\begin{aligned} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OH} = -100  \mu\text{A} \\ &I_{OH} = -4 \text{ mA} \\ &I_{OH} = -8 \text{ mA} \\ &I_{OH} = -12 \text{ mA} \\ &I_{OH} = -16 \text{ mA} \\ &I_{OH} = -24 \text{ mA} \\ &I_{OH} = -32 \text{ mA} \end{aligned}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V <sub>CC</sub> - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V <sub>CC</sub> 1.4 2.1 2.4 2.7 2.5 4.0	- - - - -	V <sub>CC</sub> - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	- - - - -	V
V <sub>OL</sub>	Low-Level Output Voltage	$\begin{aligned} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OL} = 100  \mu\text{A} \\ &I_{OL} = 4 \text{ mA} \\ &I_{OL} = 8 \text{ mA} \\ &I_{OL} = 12 \text{ mA} \\ &I_{OL} = 16 \text{ mA} \\ &I_{OL} = 24 \text{ mA} \\ &I_{OL} = 32 \text{ mA} \end{aligned}$	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		- 0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55	111111	0.1 0.24 0.3 0.4 0.4 0.55	<b>V</b>
I <sub>IN</sub>	Input Leakage Cur- rent	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	μΑ
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	-	_	1.0	-	10	μΑ
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	-	-	1.0	-	10	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

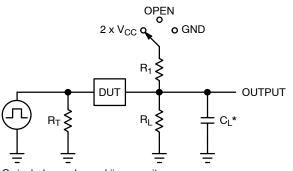
#### **AC ELECTRICAL CHARACTERISTICS**

			V <sub>CC</sub>		<sub>A</sub> = 25°	С	-55°C ≤ T	<sub>A</sub> ≤ 125°C	
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Units
t <sub>PLH</sub> ,	t <sub>PLH</sub> , Propagation Delay, A to Y (Figures 3 and 4)	$R_L = 1 M\Omega$ , $C_L = 15 pF$	1.65 to 1.95	_	6.3	12	_	12.7	ns
₹PHL		$R_L = 1 M\Omega$ , $C_L = 15 pF$	2.3 to 2.7	-	3.4	7.0	=	7.5	
		$R_L = 1 M\Omega$ , $C_L = 15 pF$	3.0 to 3.6	-	2.6	4.7	=	5.0	
		$R_L = 500 \Omega$ , $C_L = 50 pF$		-	3.3	5.2	=	5.5	
		$R_L = 1 M\Omega$ , $C_L = 15 pF$	4.5 to 5.5	-	2.2	4.1	=	4.4	
		$R_L = 500 \Omega$ , $C_L = 50 pF$		_	2.7	4.5	_	4.8	1

#### **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$	2.5	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$	2.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	10 MHz, $V_{CC}$ = 3.3 V, $V_{IN}$ = 0 V or $V_{CC}$ 10 MHz, $V_{CC}$ = 5.5 V, $V_{IN}$ = 0 V or $V_{CC}$	9 11	pF

<sup>5.</sup>  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$ .



Test	Switch Position	C <sub>L</sub> , pF	$R_L, \Omega$	R <sub>1</sub> , Ω			
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	See AC Character	See AC Characteristics Table				
t <sub>PLZ</sub> / t <sub>PZL</sub>	2 x V <sub>CC</sub>	50	500	500			
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND	50	500	500			

X = Don't Care

C<sub>L</sub> includes probe and jig capacitance

 $R_{T}$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega)$ 

f = 1 MHz

Figure 3. Test Circuit



Figure 4. Switching Waveforms

		V <sub>m</sub>		
V <sub>CC</sub> , V	V <sub>mi</sub> , V	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> , t <sub>PZH</sub> , t <sub>PHZ</sub>	V <sub>Y</sub> , V
1.65 to 1.95	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
2.3 to 2.7	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
3.0 to 3.6	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.3
4.5 to 5.5	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.3

#### **DEVICE ORDERING INFORMATION**

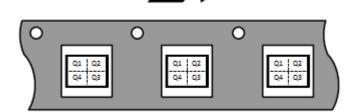
Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL17SZ08DFT2G	SC-88A	L2	Q4	3000 / Tape & Reel
NL17SZ08DFT2G-Q*	SC-88A	L2	Q4	3000 / Tape & Reel
NL17SZ08DBVT1G	SC-74A	AH	Q4	3000 / Tape & Reel
NL17SZ08DBVT1G-Q*	SC-74A	AH	Q4	3000 / Tape & Reel
NL17SZ08XV5T2G	SOT-553	L2	Q4	4000 / Tape & Reel
NL17SZ08P5T5G	SOT-953	E (Rotated 180° CW)	Q2	8000 / Tape & Reel
NL17SZ08MU1TCG	UDFN6, 1.45 x 1.0, 0.5P	D (Rotated 180° CW)	Q4	3000 / Tape & Reel
NL17SZ08MU3TCG	UDFN6, 1.0 x 1.0, 0.35P	P (Rotated 180° CW)	Q4	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP

#### Pin 1 Orientation in Tape and Reel

#### Direction of Feed



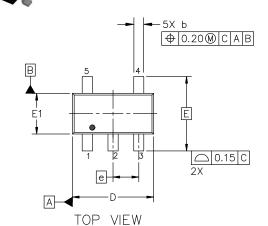
Capable.

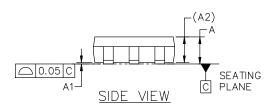


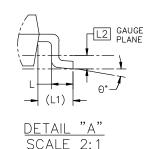
PACKAGE DIMENSIONS



**DATE 26 FEB 2024** 







#### **GENERIC MARKING DIAGRAM\***



XXX = Specific Device Code

= Date Code M

= Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

#### NOTES:

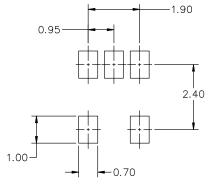
- DIMENSIONING AND TOLERANCING CONFORM TO ASME 1. Y14.5-2018.
- ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM

DETAIL	A —
C _	
+	
END	VIEW

DIM	MIN.	NOM.	MAX.	
Α	0.90	1.00	1.10	
A1	0.01	0.18	0.10	
A2	(	0.95 REF		
b	0.25	0.37	0.50	
С	0.10	0.18	0.26	
D	2.85	3.00	3.15	
Е		2.75 BSC	)	
E1	1.35	1.50	1.65	
e		0.95 BSC	)	
٦	0.20	0.40	0.60	
L1	0.62 REF.			
L2	0.25 BSC			
Θ	0,	5*	10°	

**MILLIMETERS** 



#### RECOMMENDED MOUNTING FOOTPRINT\*

FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly fron Printed versions are uncontrolled except when stamped "CONTROLLET	
DESCRIPTION:	SC-74A-5 3.00x1.50x0.95, 0.95P		PAGE 1 OF 1

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#### PACKAGE DIMENSIONS



#### SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

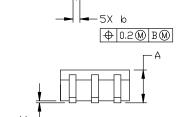
**DATE 11 APR 2023** 

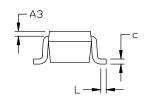
#### NOTES:

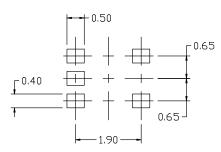
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETERS
- 419A-01 DBSDLETE, NEW STANDARD 419A-02
- 4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MI	LLIMETE	RS
INITU	MIN.	N□M.	MAX.
А	0.80	0.95	1.10
A1			0.10
A3	0.20 REF		
b	0.10	0.20	0.30
C	0.10		0.25
D	1.80	2.00	2,20
Е	2.00	2.10	2.20
E1	1.15	1.25	1.35
е	0.65 BSC		
L	0.10	0.15	0.30

## SCALE 2:1







#### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

#### **GENERIC MARKING DIAGRAM\***



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

= Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:
PIN 1. BASE	PIN 1. ANODE	PIN 1. ANODE 1	PIN 1. SOURCE 1	PIN 1. CATHODE
2. EMITTER	<ol><li>EMITTER</li></ol>	2. N/C	2. DRAIN 1/2	2. COMMON ANODE
3. BASE	3. BASE	3. ANODE 2	<ol><li>SOURCE 1</li></ol>	3. CATHODE 2
4. COLLECTOR	<ol><li>COLLECTOR</li></ol>	<ol><li>CATHODE 2</li></ol>	4. GATE 1	4. CATHODE 3
<ol><li>COLLECTOR</li></ol>	<ol><li>CATHODE</li></ol>	<ol><li>CATHODE 1</li></ol>	5. GATE 2	<ol><li>CATHODE 4</li></ol>
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

DOCUMENT NUMBER:	98ASB42984B Electronic versions are uncontrolled except when accessed directly from Printed versions are uncontrolled except when stamped "CONTROLLED		
DESCRIPTION:	SC-88A (SC-70-5/SOT-353)		PAGE 1 OF 1

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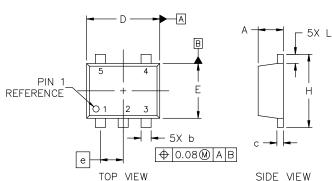


PACKAGE DIMENSIONS



#### SOT-553-5 1.60x1.20x0.55, 0.50P CASE 463B ISSUE D

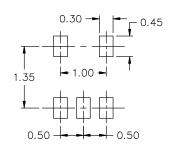
**DATE 21 FEB 2024** 



#### NOTES:

- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
- ALL DIMENSION ARE IN MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	М	MILLIMETERS			
I DIIVI	MIN.	NOM.	MAX.		
А	0.50	0.55	0.60		
b	0.17	0.22	0.27		
С	0.08	0.13	0.18		
D	1.55	1.60	1.65		
E	1.15	1.20	1.25		
е	0.50 BSC				
Н	1.55	1.60	1.65		
Ĺ	0.10	0.20	0.30		



#### RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

#### **GENERIC MARKING DIAGRAM\***



XX = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:	STYLE 2: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4	STYLE 3:	STYLE 4:	STYLE 5:
PIN 1. BASE		PIN 1. ANODE 1	PIN 1. SOURCE 1	PIN 1. ANODE
2. EMITTER		2. N/C	2. DRAIN 1/2	2. EMITTER
3. BASE		3. ANODE 2	3. SOURCE 1	3. BASE
4. COLLECTOR		4. CATHODE 2	4. GATE 1	4. COLLECTOR
5. COLLECTOR		5. CATHODE 1	5. GATE 2	5. CATHODE
STYLE 6:	STYLE 7:	STYLE 8:	STYLE 9:	
PIN 1. EMITTER 2	PIN 1. BASE	PIN 1. CATHODE	PIN 1. ANODE	
2. BASE 2	2. EMITTER	2. COLLECTOR	2. CATHODE	

PIN 1. EMITTER 2	PIN 1. BASE	PIN 1. CATHODE	PIN 1. ANODE
2. BASE 2	2. EMITTER	2. COLLECTOR	2. CATHODE
3. EMITTER 1	3. BASE	3. N/C	<ol><li>ANODE</li></ol>
4. COLLECTOR 1	<ol><li>COLLECTOR</li></ol>	4. BASE	4. ANODE
<ol><li>COLLECTOR 2/BASE 1</li></ol>	<ol><li>COLLECTOR</li></ol>	5. EMITTER	5. ANODE

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SOT-553-5 1.60x1.20x0.55, 0.50P **DESCRIPTION:** 

PAGE 1 OF 1

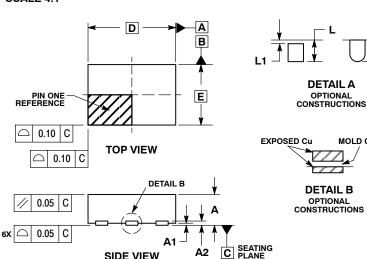
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## PACKAGE DIMENSIONS



**DATE 15 MAY 2008** 



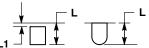
6X L

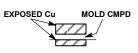
6X b

Ф

0.10 | C | A | B

0.05 C NOTE 3

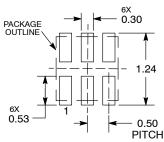




- NOTES:
  1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS			
DIM	MIN	MAX		
Α	0.45	0.55		
A1	0.00	0.05		
A2	0.07 REF			
b	0.20	0.30		
D	1.45 BSC			
Е	1.00 BSC			
е	0.50 BSC			
Ĺ	0.30	0.40		
L1		0.15		

#### **MOUNTING FOOTPRINT**



**DIMENSIONS: MILLIMETERS** 

#### **GENERIC MARKING DIAGRAM\***

**BOTTOM VIEW** 

SIDE VIEW

е



Χ = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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DESCRIPTION:	UDFN6, 1.45x1.0, 0.5P		PAGE 1 OF 1

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<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

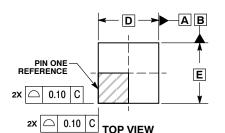


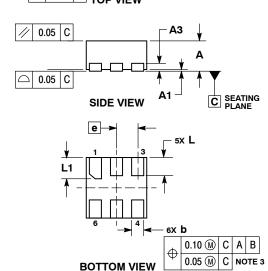
PACKAGE DIMENSIONS



UDFN6, 1x1, 0.35P CASE 517BX **ISSUE O** 

**DATE 18 MAY 2011** 



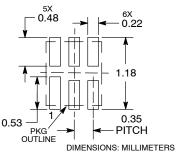


#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN
- 0.15 AND 0.20 MM FROM TERMINAL TIP.
  4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.45	0.55	
A1	0.00 0.05		
A3	0.13 REF		
b	0.12	0.22	
D	1.00 BSC		
E	1.00 BSC		
е	0.35 BSC		
L	0.25	0.35	
L1	0.30	0.40	

#### RECOMMENDED **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### **GENERIC MARKING DIAGRAM\***



X = Specific Device Code

M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	UDFN6, 1x1, 0.35P		PAGE 1 OF 1

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MILLIMETERS

 $N\square M$ 

0.37

0.15

0.12

1.00

0.80

0.35 BSC

1.00

0.175

0.10

(REF)

0.075

MIN

0.34

0.10

0.07

0.95

0.75

0.95

0.125

0.05

DIM

Α

b

C

 $\mathbb{D}$ 

E

9 Н

L2

L3

PACKAGE DIMENSIONS



#### SOT-953 1.00x0.80x0.37, 0.35P CASE 527AE **ISSUE F**

**DATE 17 JAN 2024** 

MAX

0.40

0.20

0.17

1.05

0.85

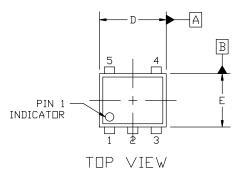
1.05

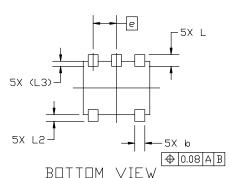
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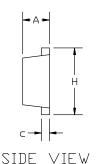
0.15

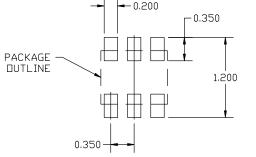
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.









#### RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

#### **GENERIC MARKING DIAGRAM\***



= Specific Device Code

= Month Code

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